```vhdl
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
--                       University of Hawaii at Manoa                        --
--              Instrumentation Development Lab / GARY S. VARNER              --
--                         Watanabe Hall Room 214                            --
--                            2505 Correa Road                               --
--                           Honolulu, HI 96822                              --
--                           Lab: (808) 956-2920                             --
--                           Fax: (808) 956-2930                             --
--                    E-mail: idlab@phys.hawaii.edu                          --
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------


-- Design by: Gary S. Varner                                                 --
-- DATE : 14 JUL 2010                                                        --
-- Project name: CREAMTEA Sequencer                                          --
-- FPGA chip : Xilinx's SPARTAN3 xc3s200-208                                 --
-- USB chip : CYPRESS CY7C68013                                              --
-- Module name: CREAMTEA_SEQ                                                 --
-- Description :                                                             --
--    Do all of the crap needed to ensure proper Trigger sequencing         --
--                                                                          --
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;


--------------------------------------------------------------------------------
--                          I/O Definitions                                  --
--------------------------------------------------------------------------------


entity CREAMTEA_SEQ is
    Port (  CLK       :    in std_logic;      -- CLOCK 60MHz global
            EXT_TRIG  :    in std_logic;      -- Active High External Trigger
            DONE      :    in std_logic;      -- Active High xDONE
            CT_TRIG   :    out std_logic);    -- Trigger output signal
end CREAMTEA_SEQ;


--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------


architecture Behavioral of CREAMTEA_SEQ is
    type State_type is(IDLE, TRIGGERED, CLEAR);
    signal state: State_type;

begin

    process(EXT_TRIG,DONE)
    begin
--      state <= IDLE;
        if falling_edge(CLK) then
            case  state is
--------------------------------------------------------------------------------
                when IDLE =>
                    CT_TRIG  <= '0';
                    if EXT_TRIG = '1' then
                        state <= TRIGGERED;
```

```
61                         end if;
62         --------------------------------------------------------------------------------
63                 when TRIGGERED =>
64                     CT_TRIG  <= '1';
65                     if DONE = '1' then
66                         state <= CLEAR;
67                     end if;
68         --------------------------------------------------------------------------------
69                 when CLEAR =>
70                     CT_TRIG  <= '0';
71                     state <= IDLE;
72         --------------------------------------------------------------------------------
73                 when others =>
74                     state <= IDLE;
75             end case;
76         --------------------------------------------------------------------------------
77         end if;
78      end process;
79   end Behavioral;
80
81   --------------------------------------------------------------------------------
82   --                              The End                                        --
83   --------------------------------------------------------------------------------
84
```