Timing Issues

• We tried several sets of timing value to solve the problem but failed.
• Finally, we found the reason while we observed the TSA_OUT waveform.
• The problem occurs on board 1 and 4.
TSA_OUT waveform on board 0 (taken from UH)
TSA_OUT waveform on board 2
TSA_OUT waveform on board 1 and 4
Sampling Speed

- We set the same VadjN1, VadjN2, VadjP1 and VadjP2 on boards but we achieve faster sampling speed on board 1 and 4.
- TSA from input to output only takes 122ns on board 1 and 4. (High sampling speed)
- Solution:
  - Short TSA value, but limited by FPGA timing constraints and strobe time of IRS.
  - Adjust Vadj values → adjust Sampling speed
After adjust VadjN1

Previous: \((V_{adj1}, V_{adj2}, V_{adj1}, V_{adj2}) = (990, 990, 0, 0)\)

After: \((V_{adj1}, V_{adj2}, V_{adj1}, V_{adj2}) = (1024, 990, 0, 0)\)
Waveform (after Adjust VadjN1)