ANITA-III Coherent Waveform Trigger

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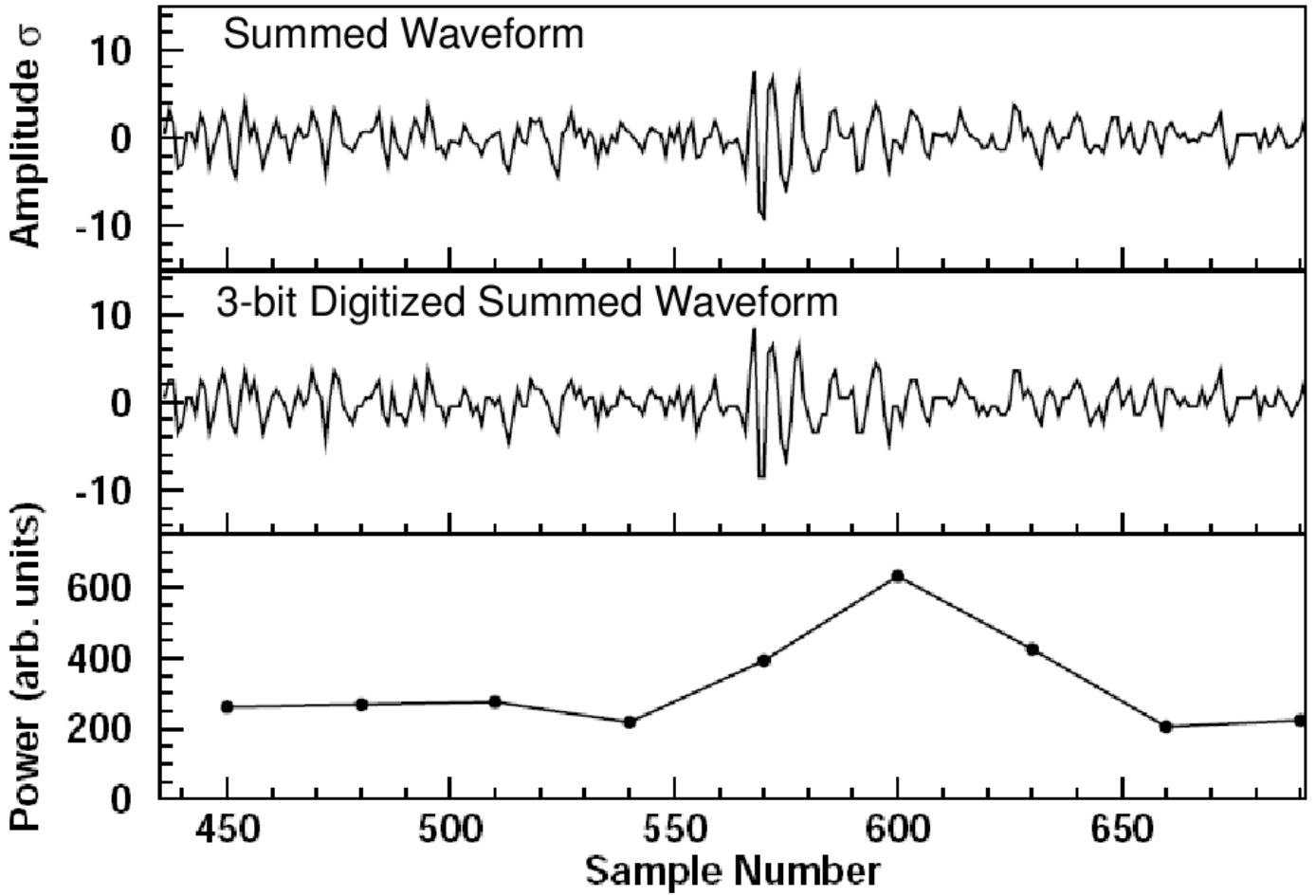
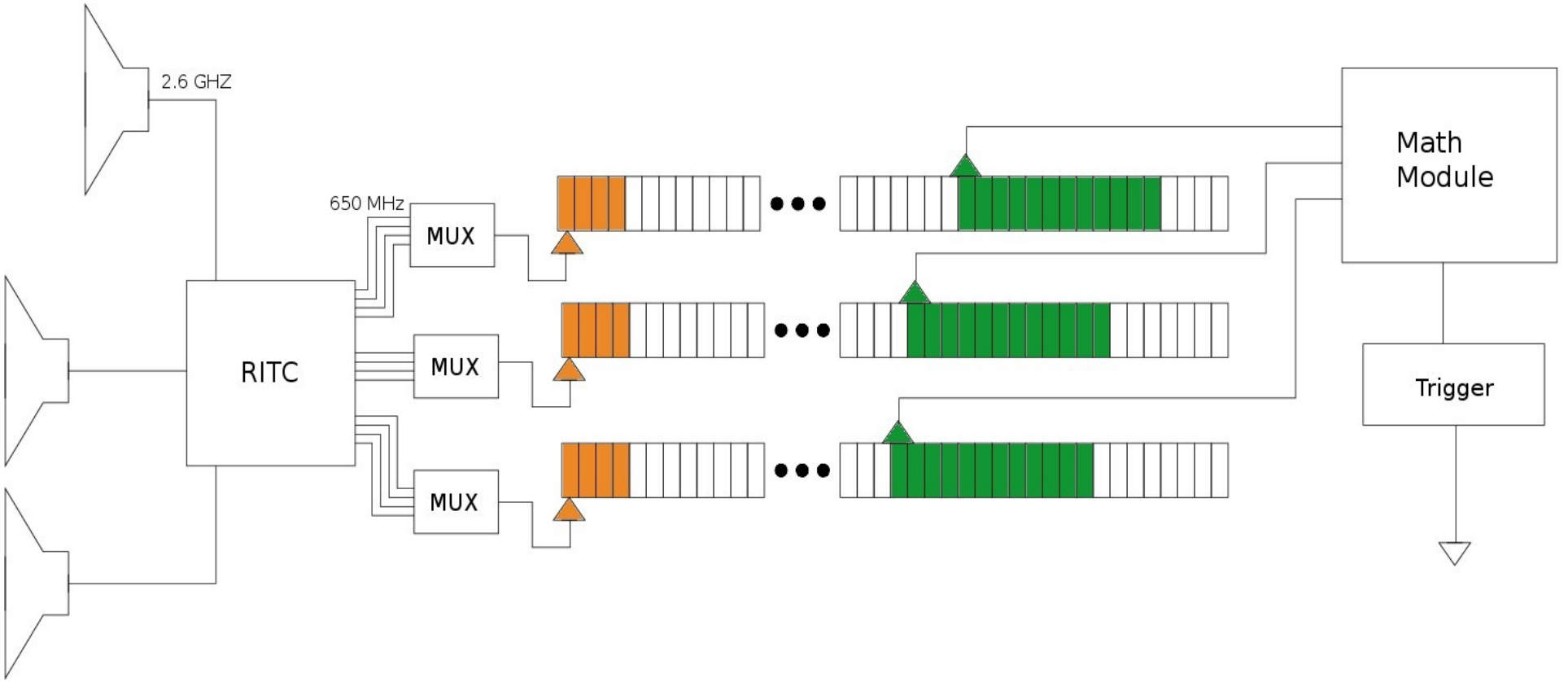
Correlation Trigger

- Phase align 3-bit waveforms of a phi sector according to various angles
- Sum waveform and take a power over 32 samples
- Repeat every 16 samples
- Trigger at a threshold power level



Basic Outline



- Multiplexor feeds digitized waveforms to a shift register of length 128.
- The math module sums, takes the square and sums again, 67 are needed.

RITC

- Reads in data from the antennas at 2.6 GHz
- Outputs digitized data in parallel at 650MHz
- Also outputs a LVDS clock
- Submitted May 9, chip expected in August

Current FPGA

- Top: input is LVDS from RITC, outputs a trigger
  - Mux2Reg: Serializes RITC data into a shift register
  - SPIM (Sum, power, integral module)
    - LUT for sum and power
    - Trigger threshold
  - Trigger -OR- gate
  - Clock multiplier

Space Concerns

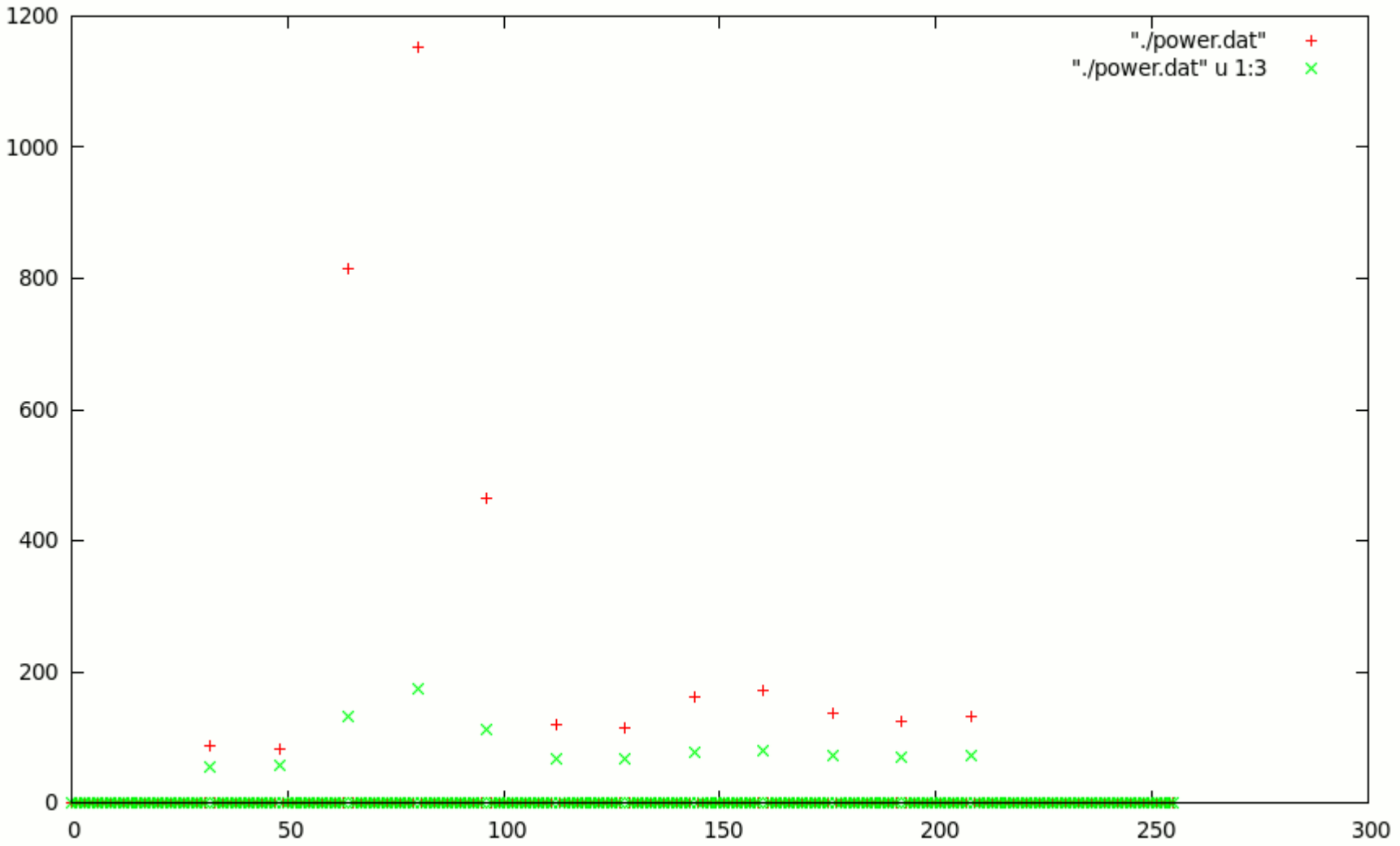
Amount of logic needed is substantial. Currently all needed logic doesn't fit onto the FPGA. A method to combat this that is being explored is compressing the sum and square of the waveforms.

Digitized waveform has 8 possible values (-3.5,-2.5,-1.5,-0.5,0.5,1.5,2.5,3.5)
Thus a sum of 3 of these has 22 possible values.
But the square of the sum has only 11.
So the sum and square can be done with one look-up table and give an answer of only 4 bits instead of 5.

However, if we wish to take best advantage of this, the horizontal sum over the 32 windows will add the 4 bit numbers. Translating back to 5 bit is do-able, but would add more logic back!

So the question is, can we use the compressed data for the power threshold?

Possibly?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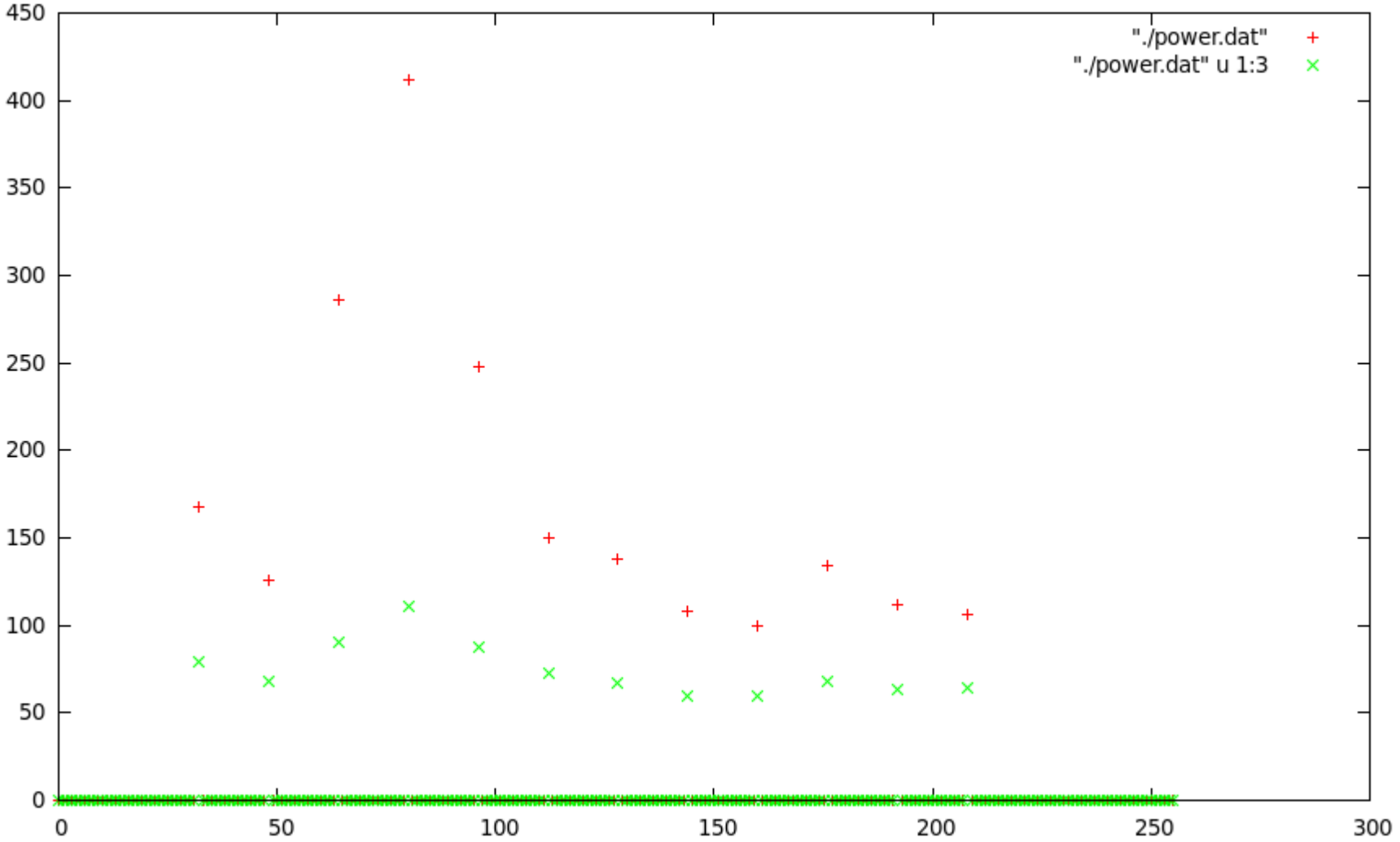
SNR 2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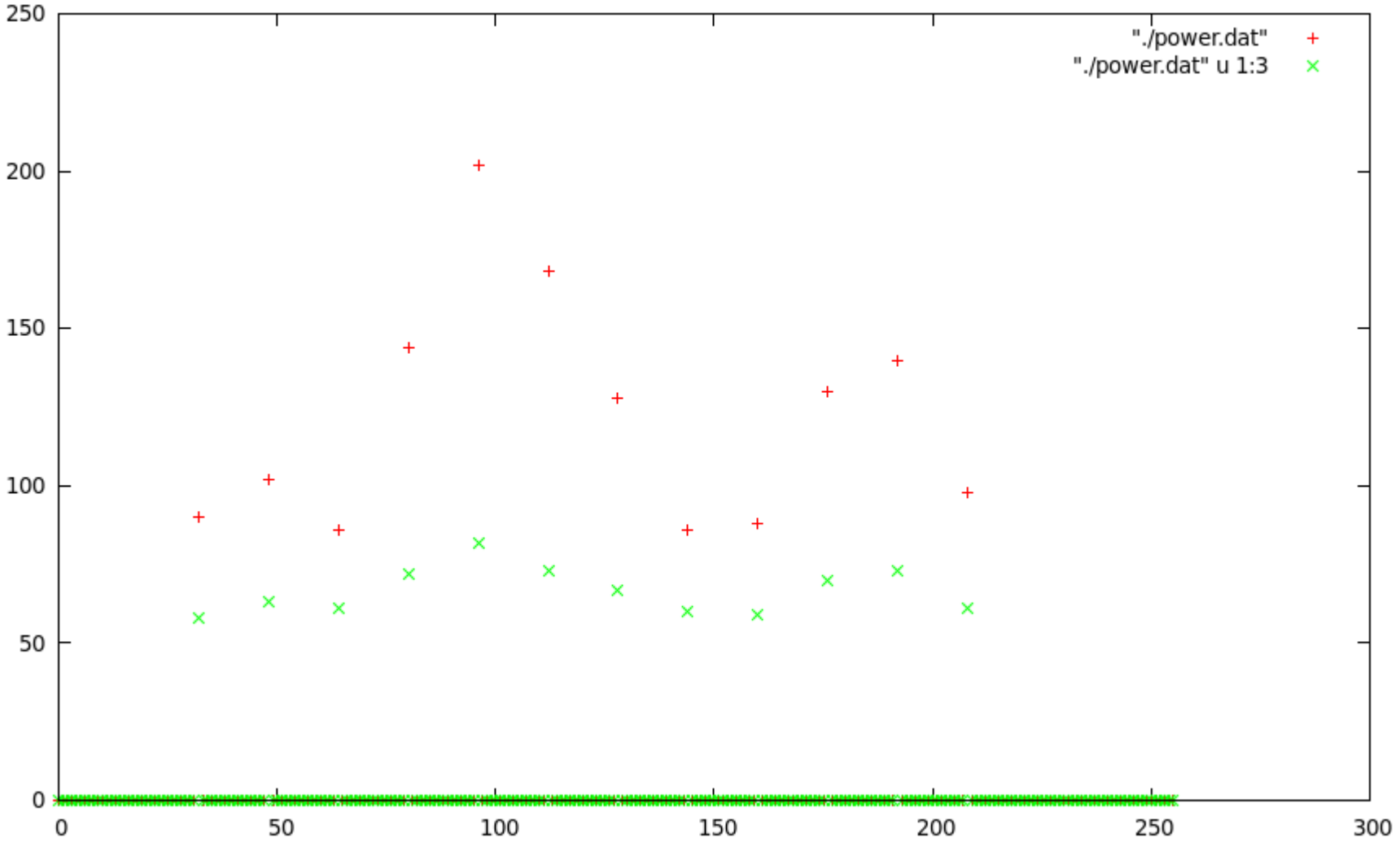
SNR 1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