OSU ATRI operational status

PSA, 8/24/11

Firmware tested and working

- USB control packet data path (all destinations)
- Daughterboard detect/power on
- All daughter interfaces (I^2C, trigger, IRS)
- PPS counter, clock counter
- Scalers, stuck bit detection
- Wilkinson monitor
- irs_block_manager operation (both pedestal and normal mode)
- TSAOUT inputs seen (but no phase detect)

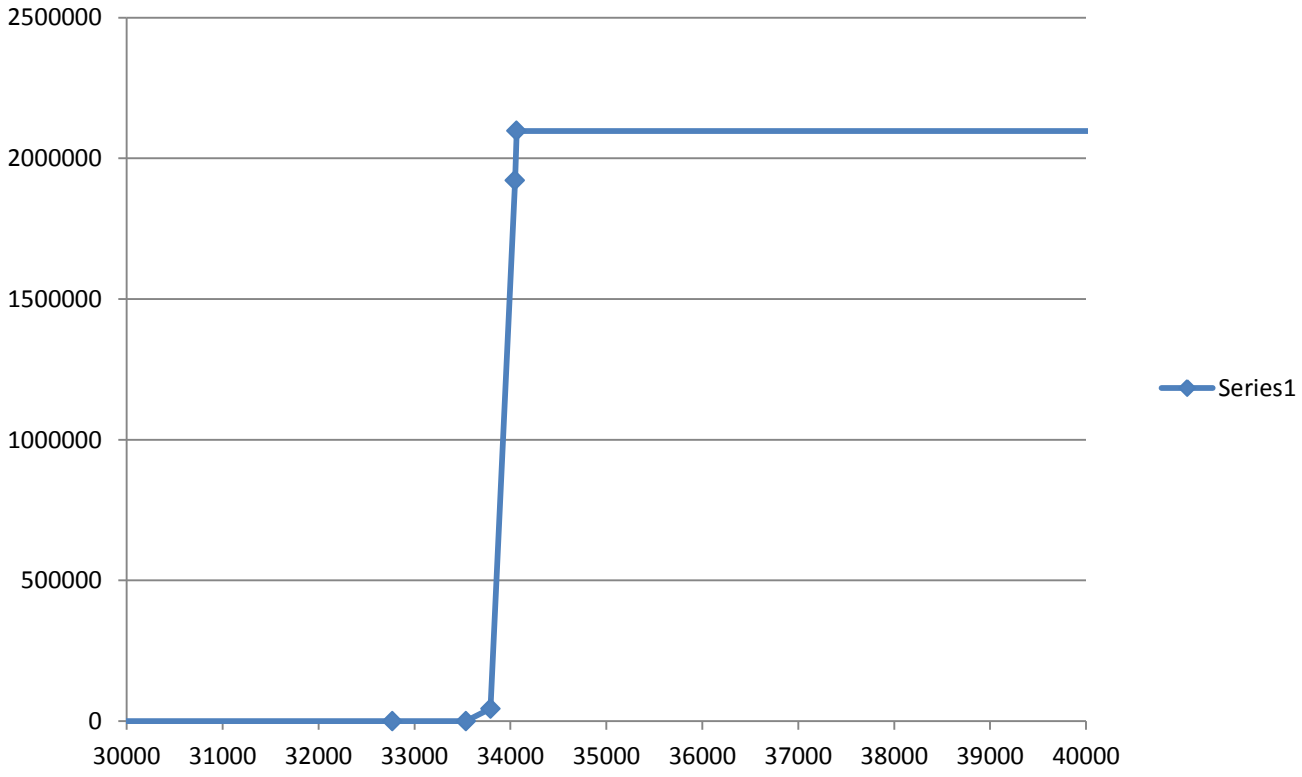
Still to do…

- Event path, obviously
  - Not sure how to do it: ARAAcqd doesn't seem to dump event endpoint, so endpoint is reported as full and PHY doesn't try to write to it
- Trigger path, using Thomas's readout module
  - Haven't heard from Kael et al. regarding any attempts to integrate it into irs2_top : this is critical path
- TSA phase detection
  - Need global phase shifter: 4 independently shiftable DCMs requires using all clocks (which then don't place correctly)
  - Working on it now along with event readout

Documentation…

- All I^2C devices on daughterboards documented in a message on ara-firm (DocDB and ELOG both were acting bizarre)
- All WISHBONE registers documented in doc 314 on DocDB
- Control packets documented in doc 267
- ATRI, DDA, TDA BOMs, schematics, gerbers all on DocDB

Simple first threshold scan



Transition from no triggers to greater than 2 MHz is ~2000 DAC counts

Notes

- DDA likely needs 2 component value changes
  - R10 (Isel) 20K -> 33K (for 6.2 us 0->2.5V RAMP)
  - R15 (Vbias) 100K->250K (might have some other value on there due to miscommunication) – for lower power
- With 4X TDAs and 4X DDAs, current is ~2.4 A with everything on and running (8 W)