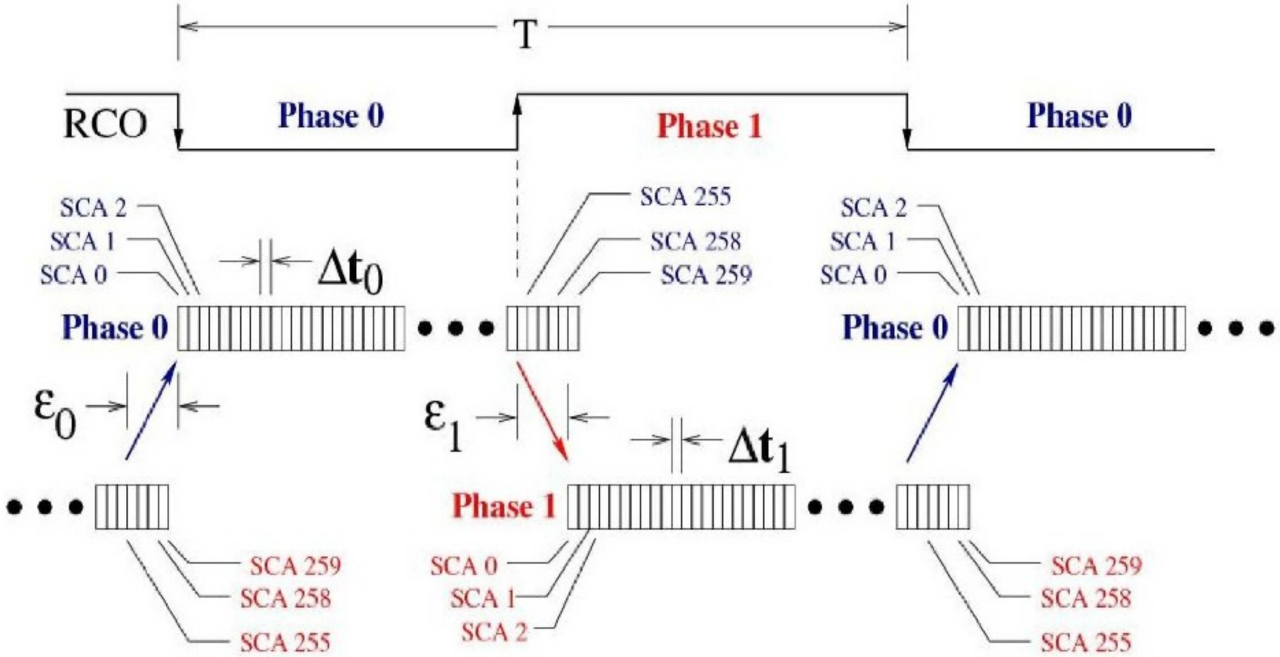
ARA Timing Calibration

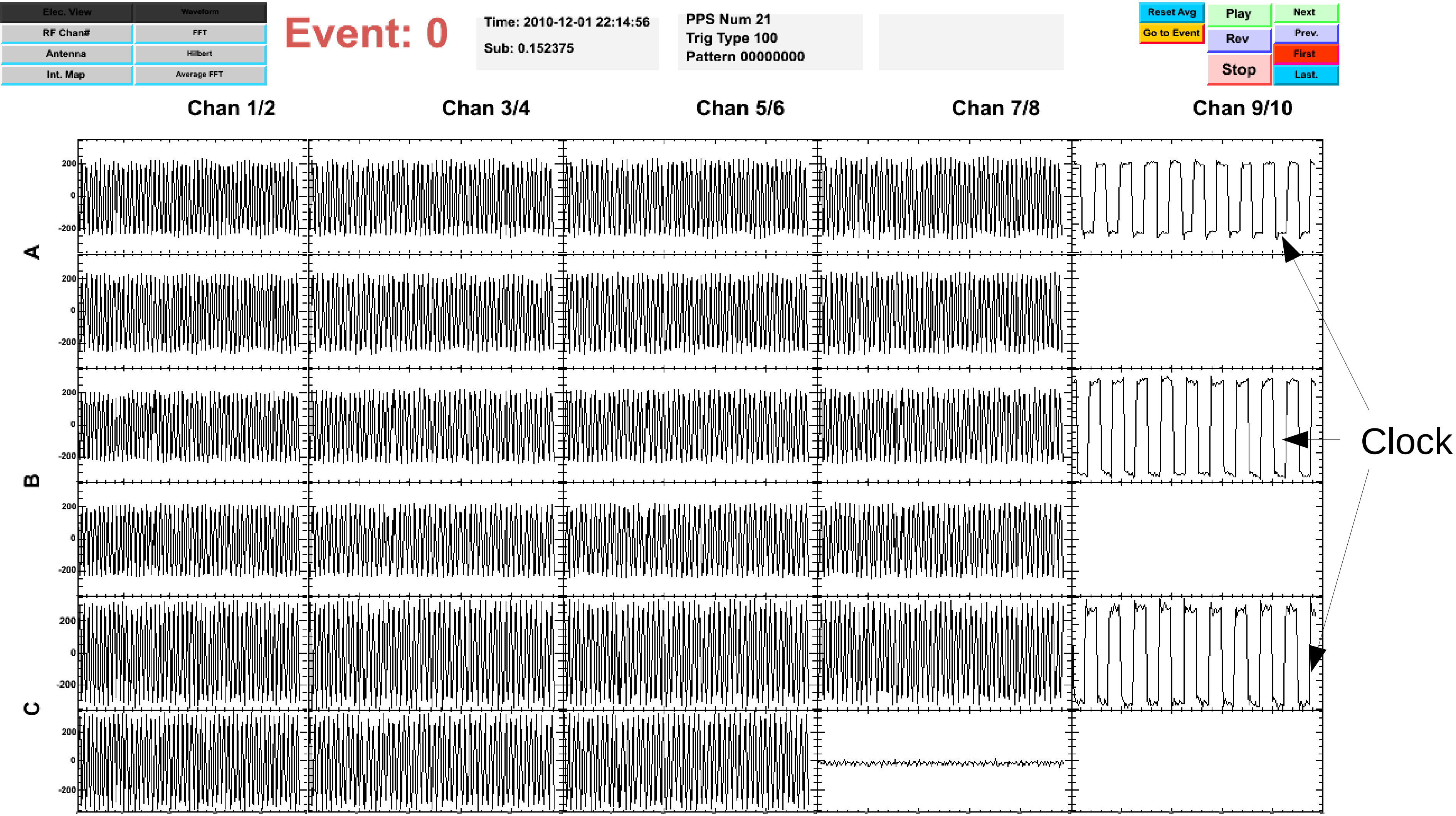
Jonathan Davies UCL

ARA Timing Calibration



Δt – Time Between Samples
ε - Wrap around Timing
-Interleave time
-Event to event jitter

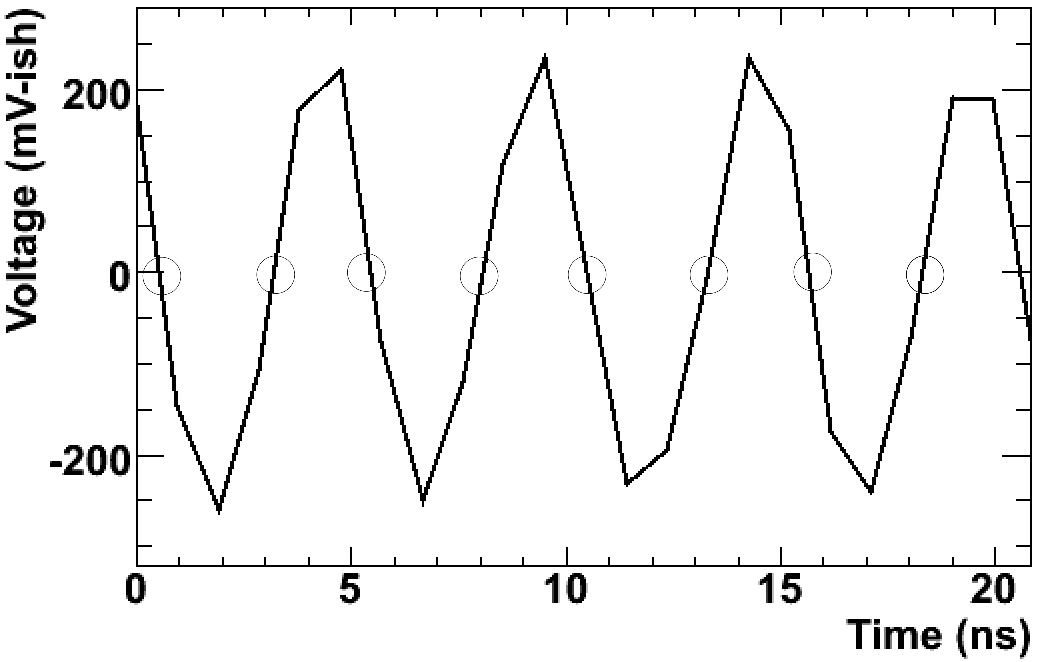
ARA Timing Calibration



ARA Timing Calibration

Time Between Samples Δt

1. Voltage in each waveform is zero-meaned
2. Total no. of zero Crossings counted over run
3. Zero-crossing occupancy averaged over run, then scaled to input wavelength



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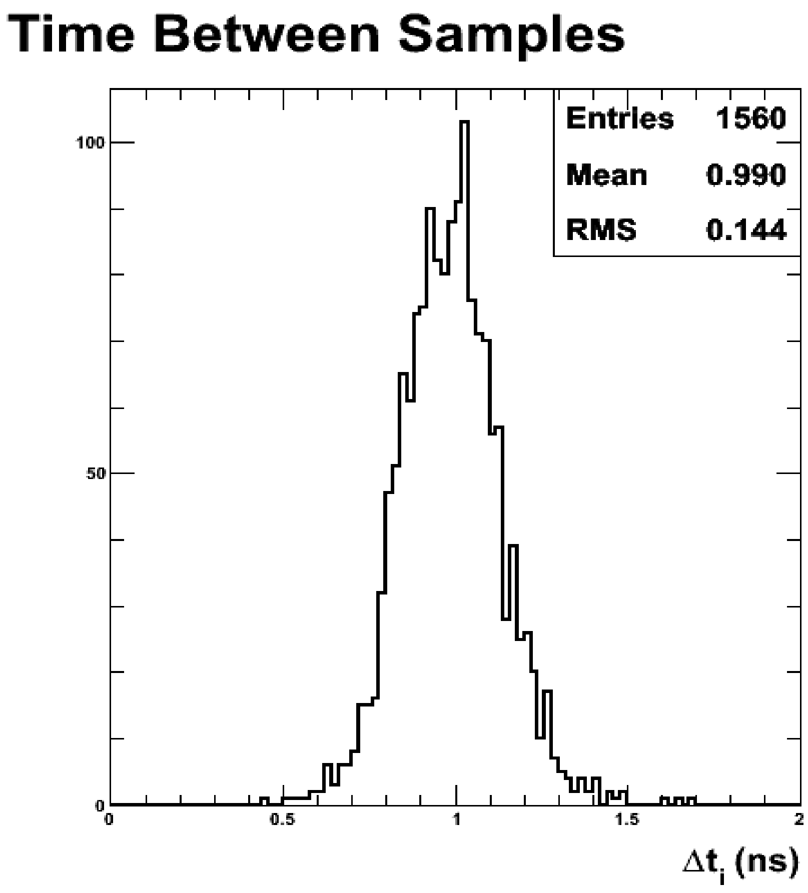
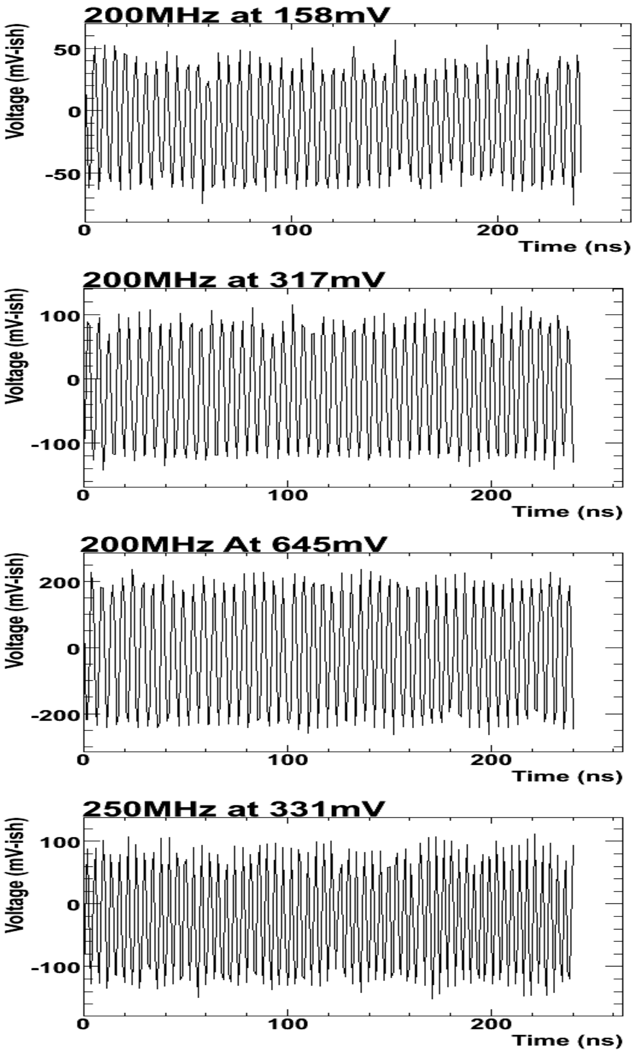
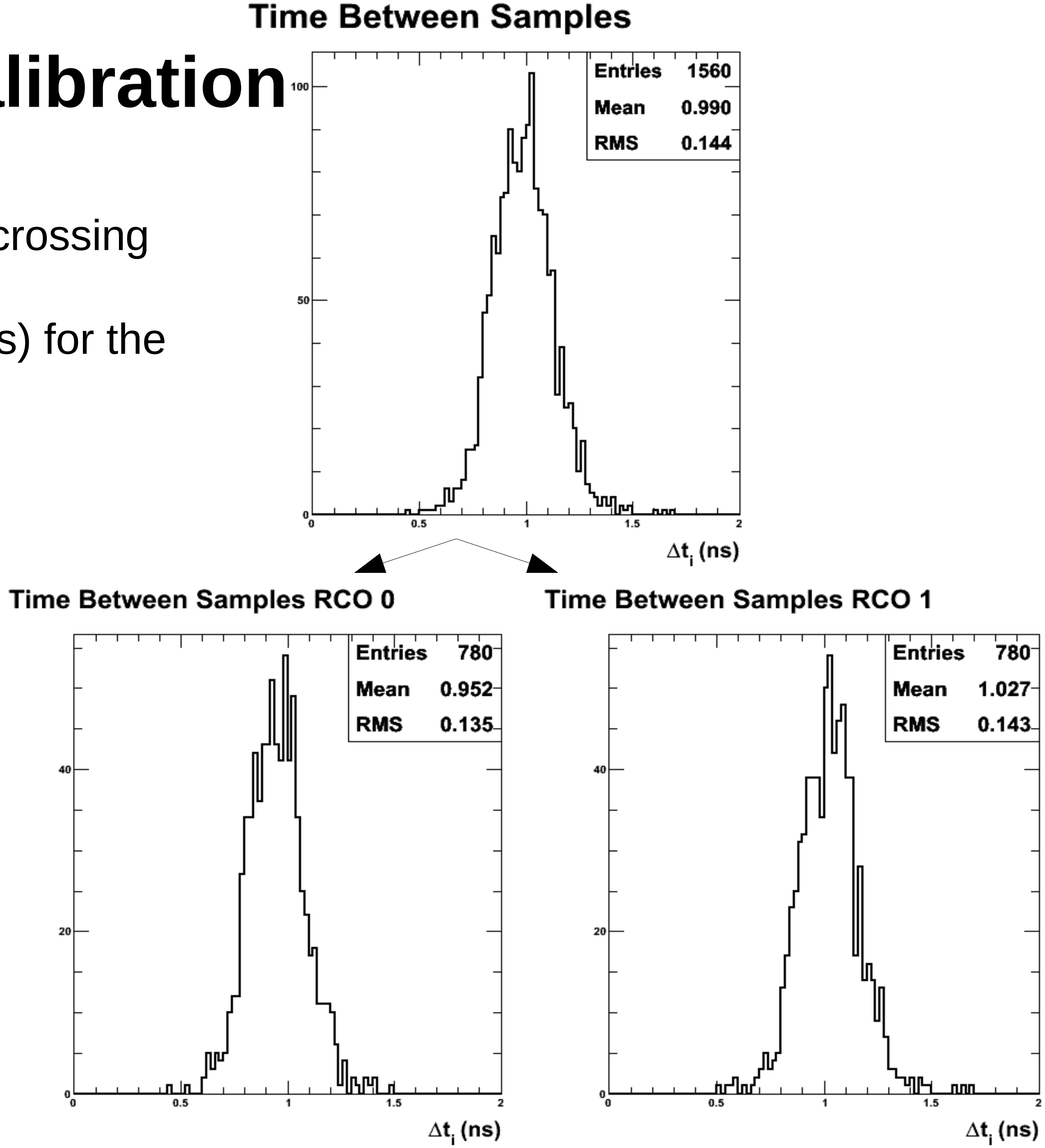




ARA Timing Calibration

Bin to bin widths using zero crossing method.
Mean width 0.952ns (1.027ns) for the RCO fast (slow) phase.



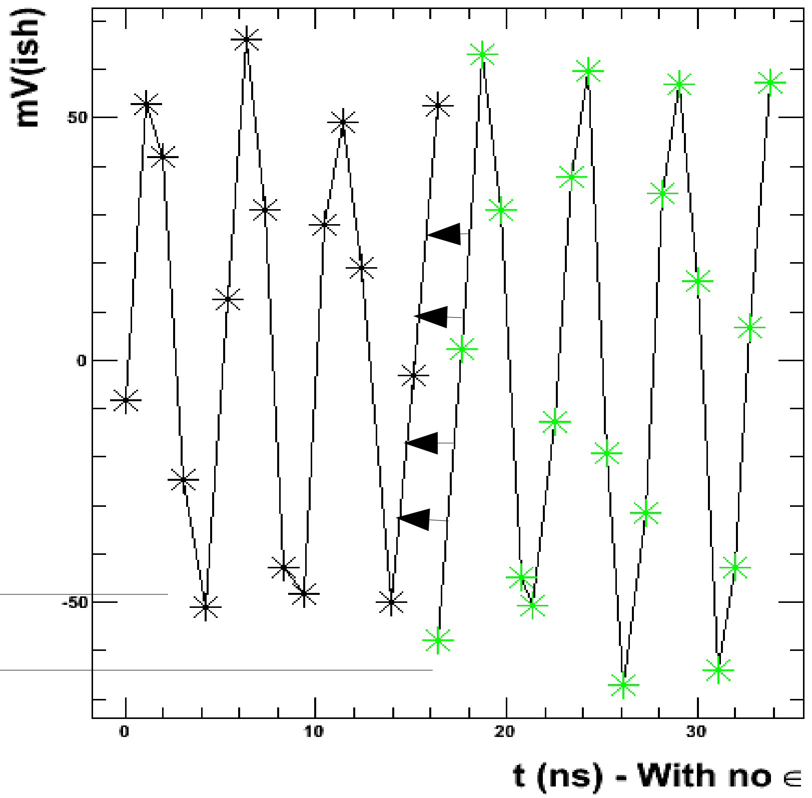
ARA Timing Calibration

Wrap Around ε

1. Voltage in each waveform is zero-meaned
2. Apply time between samples
3. Find the last (first) -ve to +ve zero crossing before (after) the wrap arounc
4. Interpolate to find times
5. Move waveforms so they overlap
6. ε is the Δt required to match waveforms

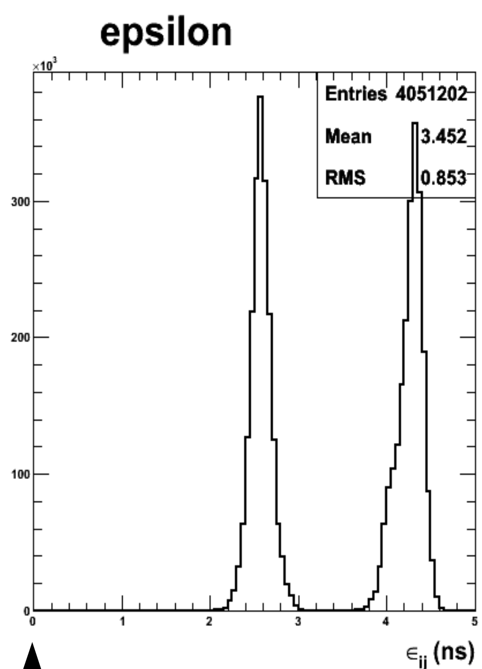
Before wrap around

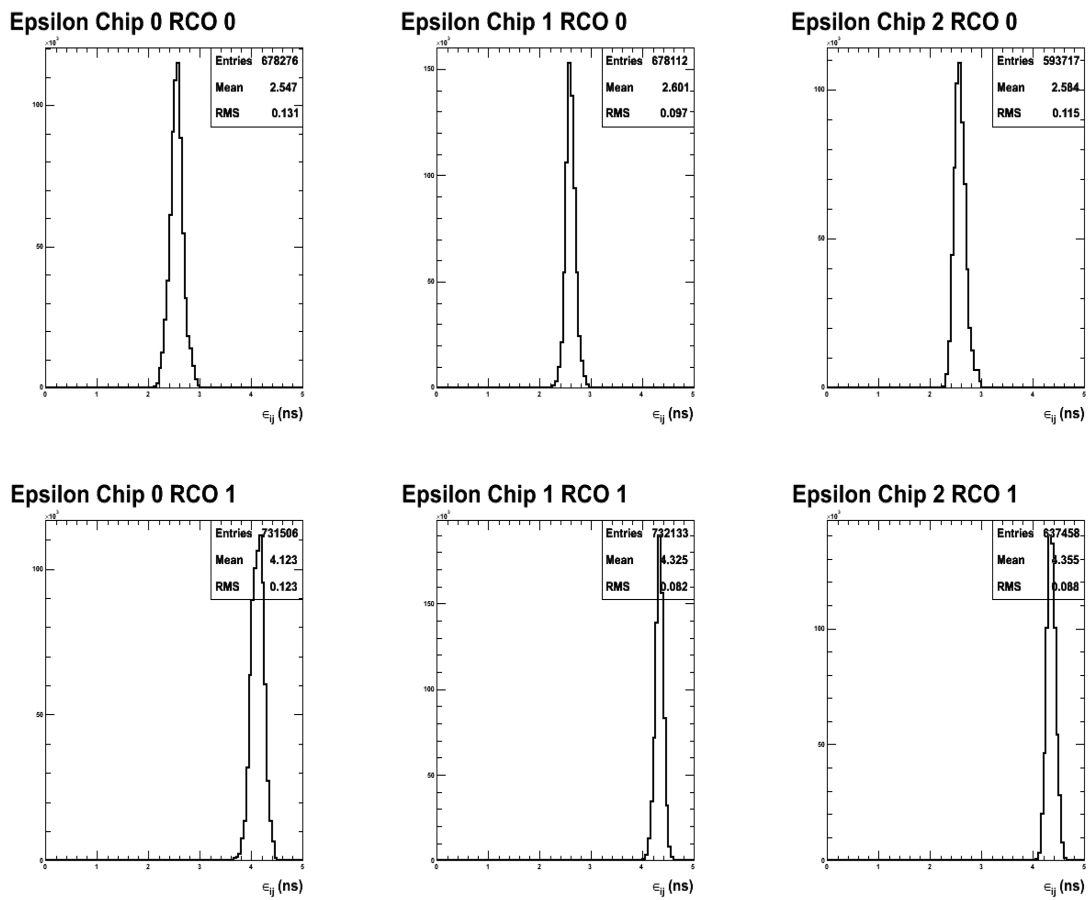
After wrap around



ARA Timing Calibration

Wrap Around ε





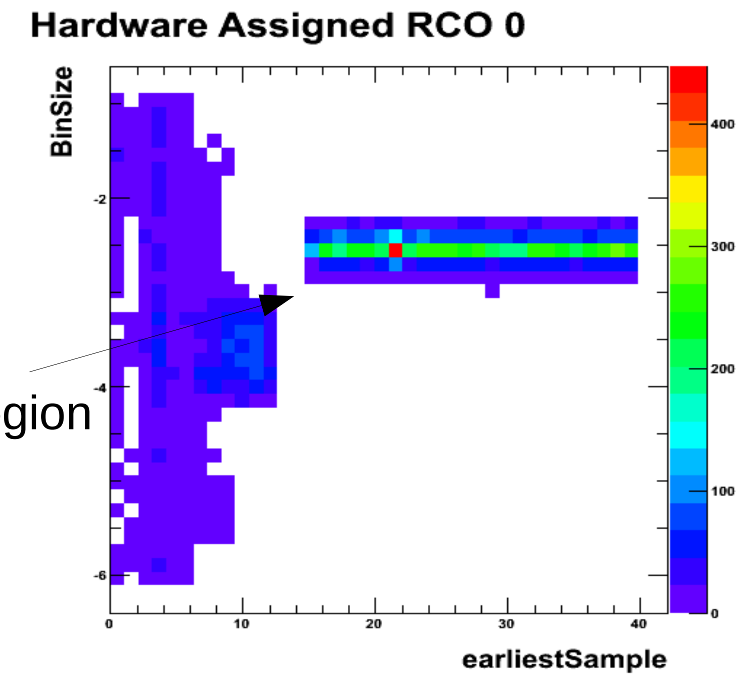
All chips and RCO 200MHz at 158mV

200MHz at 158mV

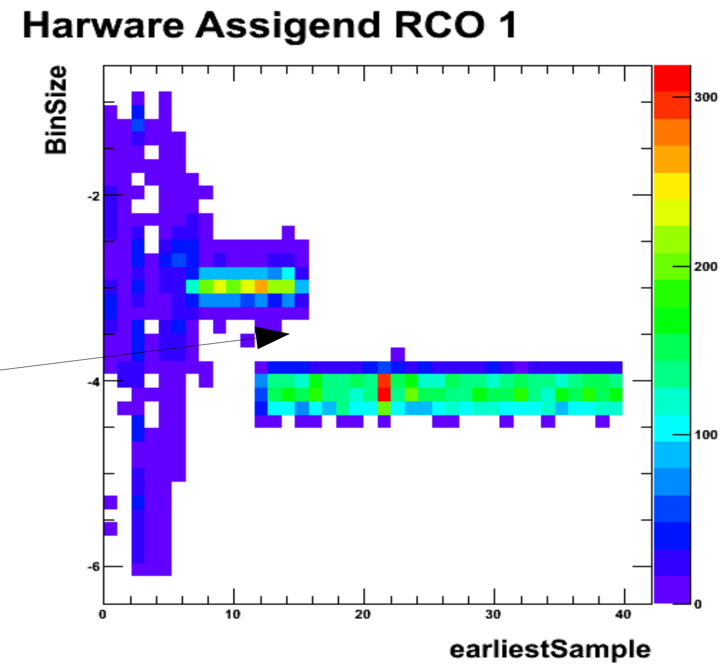
ARA Timing Calibration

RCO Phase Determination

Hardware problem where RCO phase is incorrectly assigned if earliest sample < 20



Missing region

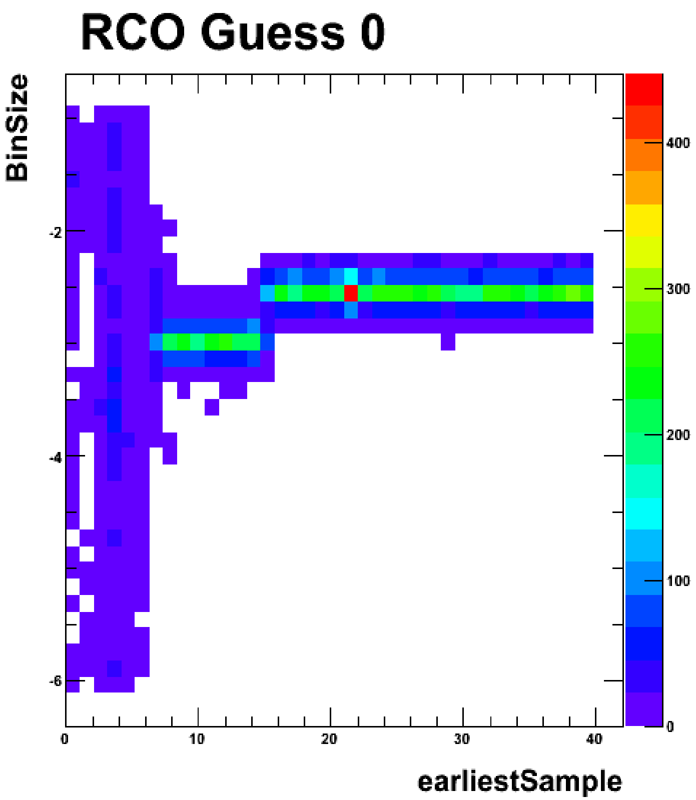


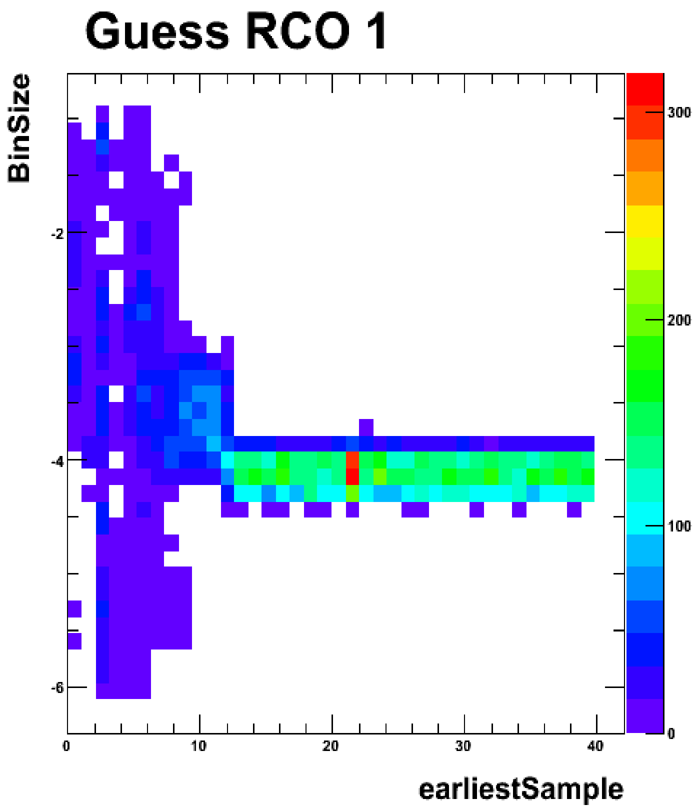
Wrong RCO

ARA Timing Calibration

RCO Phase Determination

Guess RCO in UsefulAraEvent.h tries each RCO and chooses the one closest to the clock period

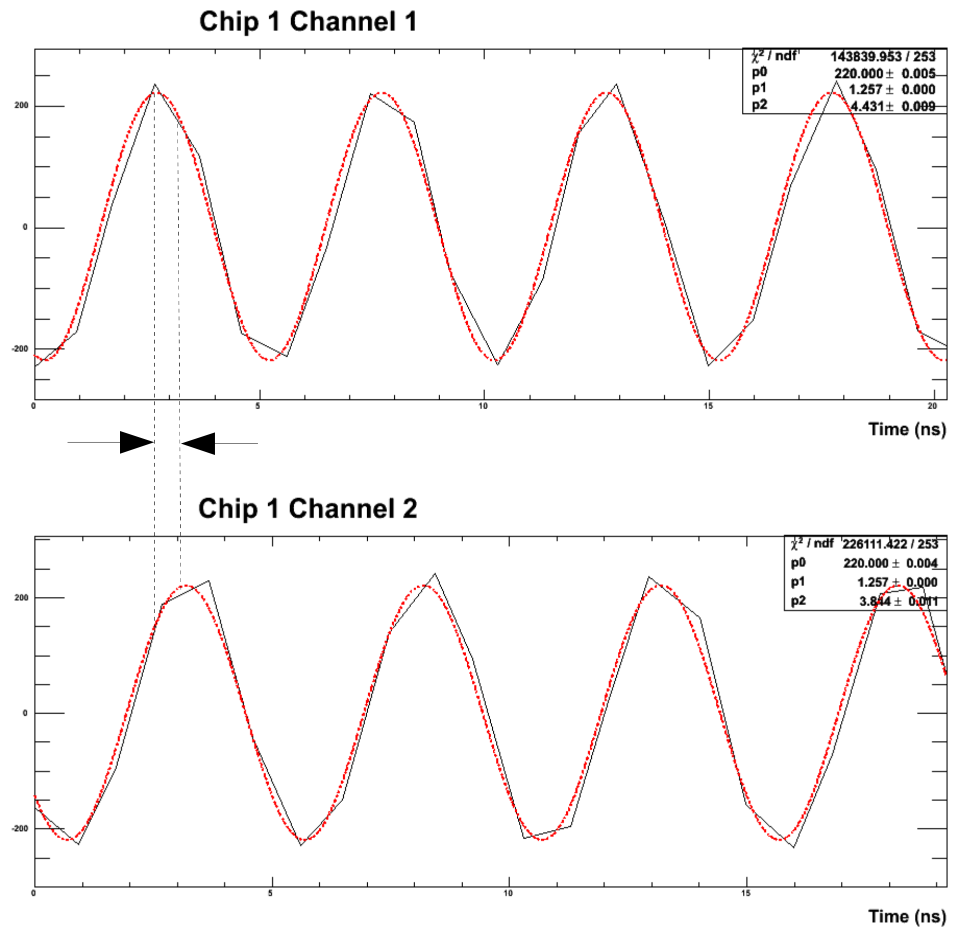




ARA Timing Calibration

Interleave Timing

1. Zero mean the wavform
2. Apply Δt and ε calibrations
3.Fit sine waves to interleaved channel pairs
4. Interleave time taken from the difference in phase

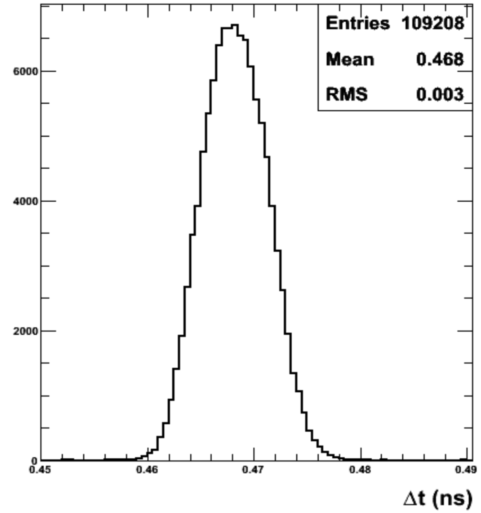


ARA Timing Calibration

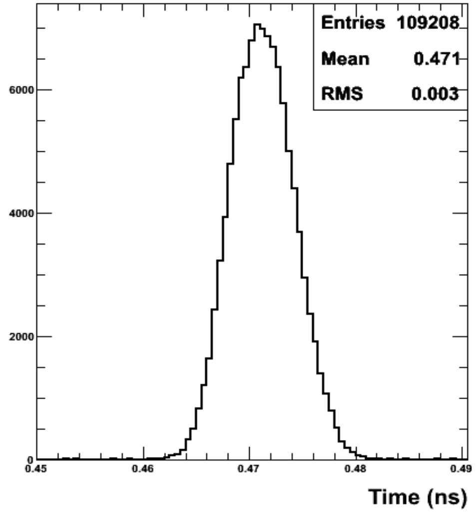
Interleave Timing

200 MHz at 158mV
Sample used

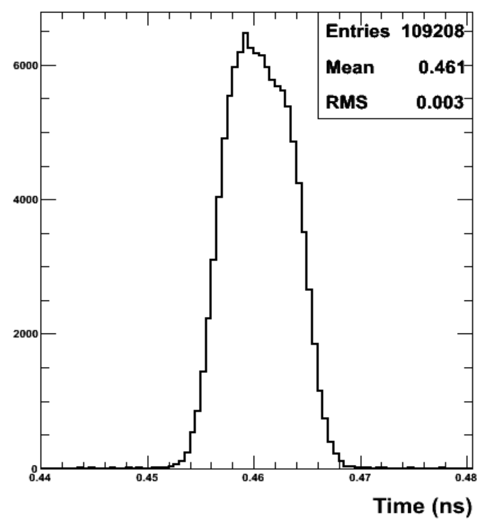
Chip 1 - Channels 1 & 2



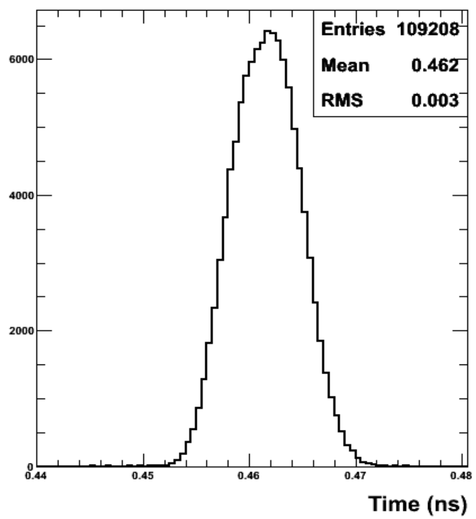
Chip 1 channels 3 & 4



Chip 1 - Channels 5 & 6



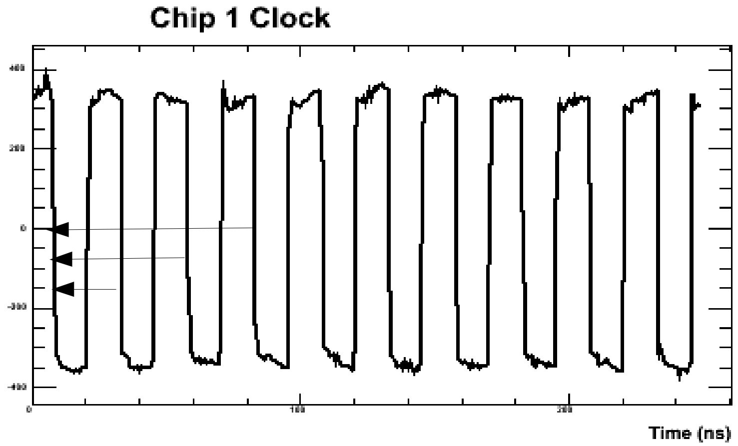
Chip 1 Channels 7 & 8

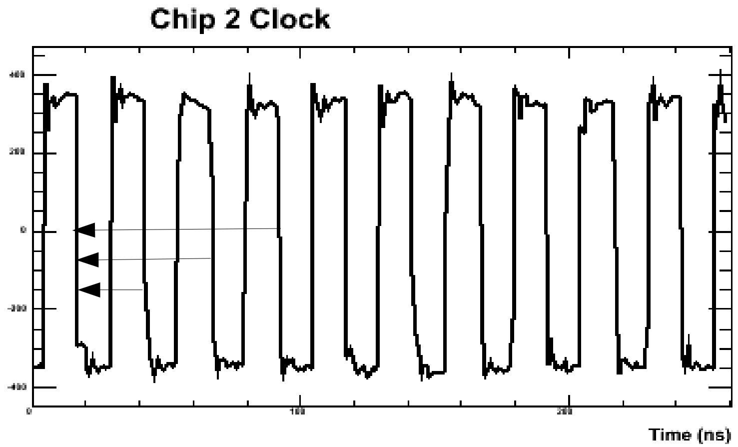


ARA Timing Calibration

Event to Event Jitter

1. Zero mean the waveform
2. Apply Δt, ε and Interleave timing calibrations
3. Look for +ve to -ve zero crossings in clock channel, taking off wavelengths
4. Compare the average clock pulse start in the three chips

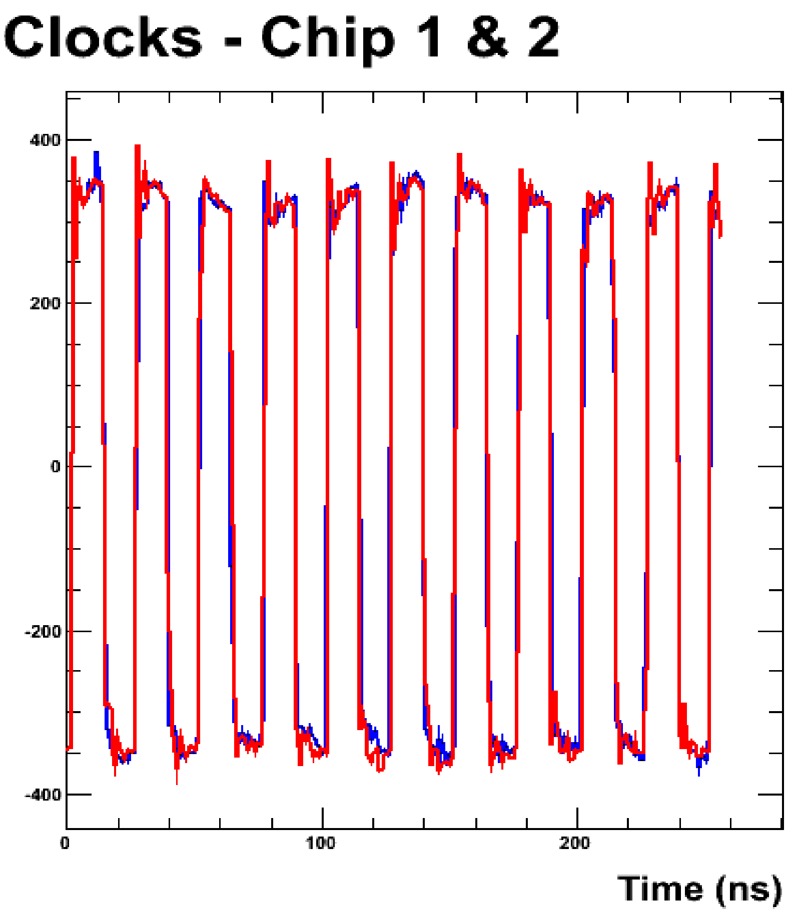




ARA Timing Calibration

Event to Event Jitter

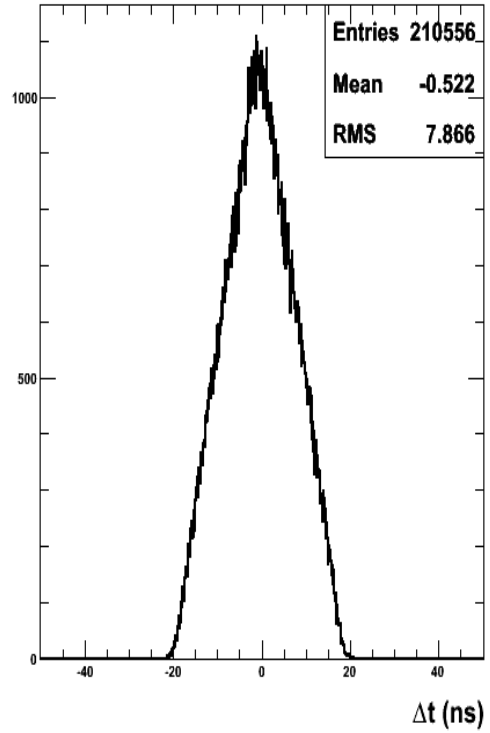
Having used the clock timing calibration the clocks are now aligned



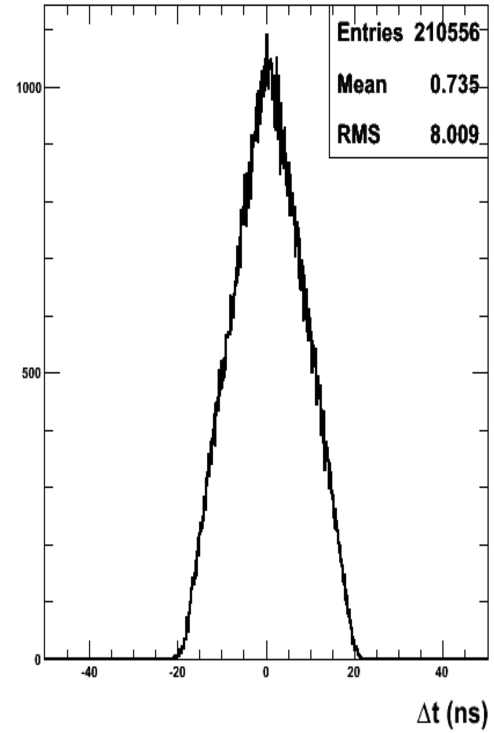
ARA Timing Calibration

Event to Event Jitter

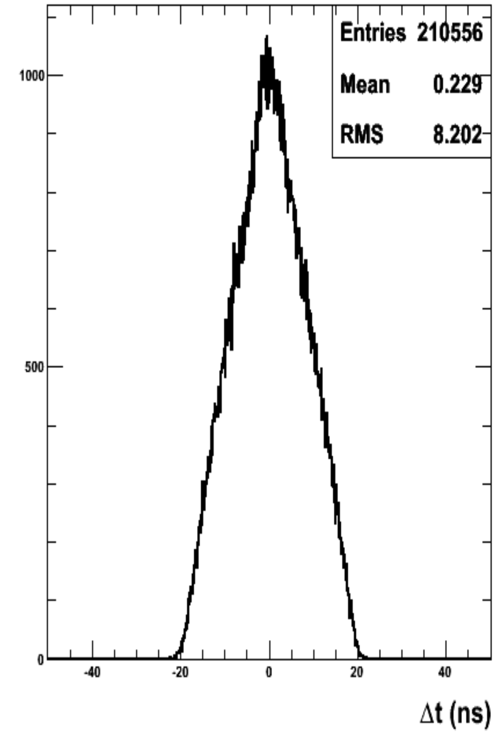
Clock Timings Chip 1 - Chip 2



Clock Timings Chip 2 - Chip 3



Clock Timings Chip1 - Chip 3



ARA Timing Calibration

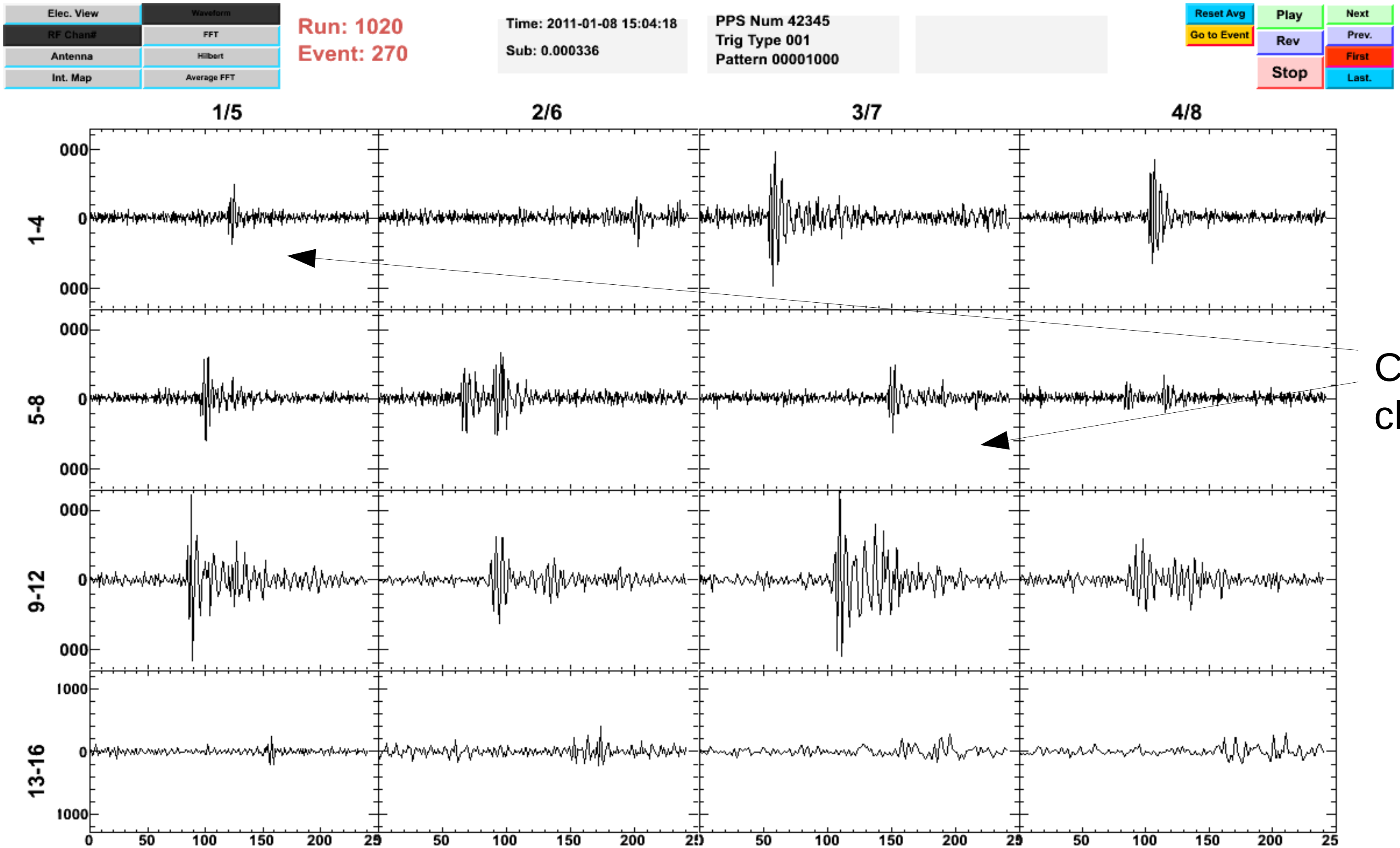
Calibration Types

KnoCalib – Gets first 260 samples from RAW data
kFirstCalib – Applies Δt, ε and Interleave
kSecondCalib – Applies Δt, ε, Interleave and event to event jitter
kLatestCalib – Currently kSecondCalib + cable delay calibration

Best to use kLatestCalib in code as this will always be the most up to date calibration

ARA Timing Calibration

Pulser Data

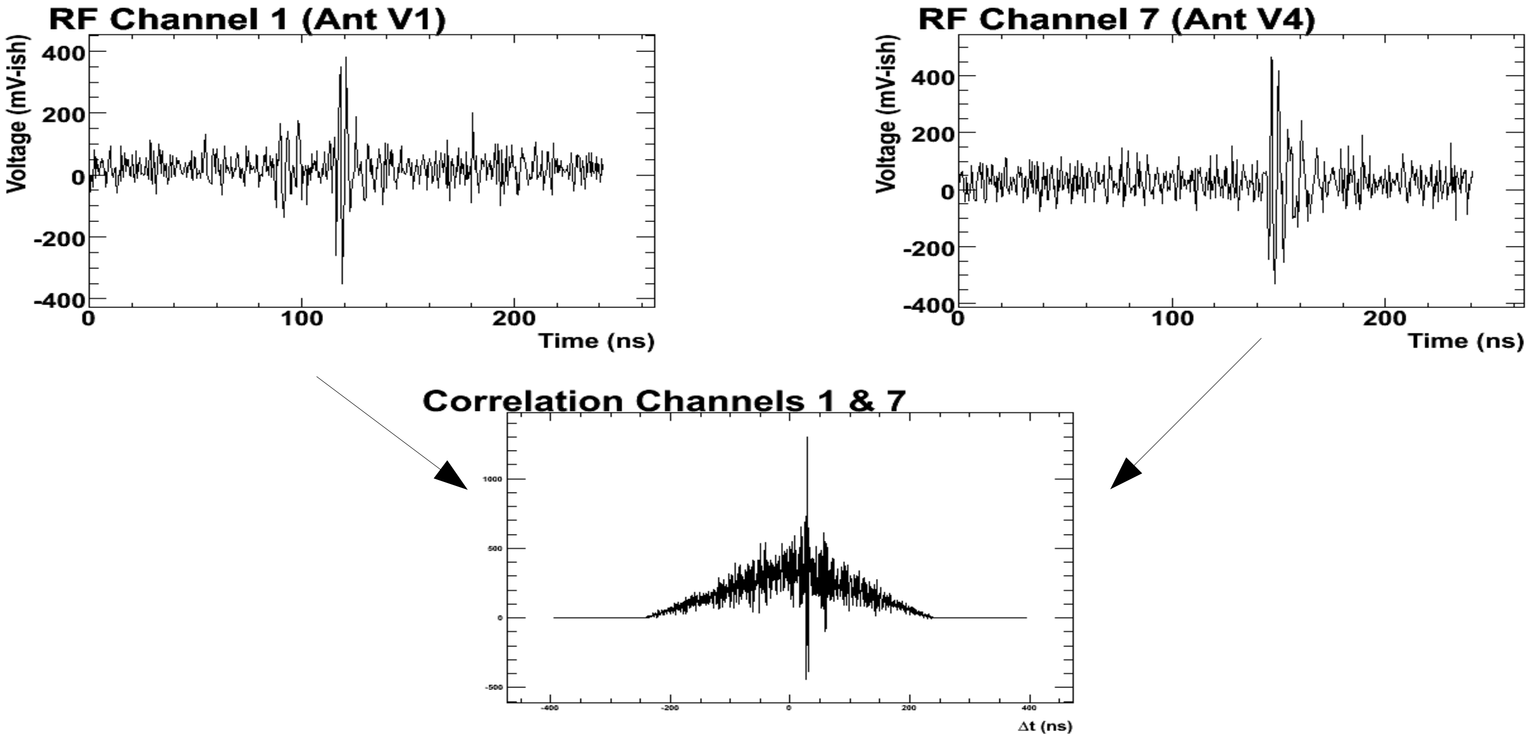


Correlate channels

ARA Timing Calibration

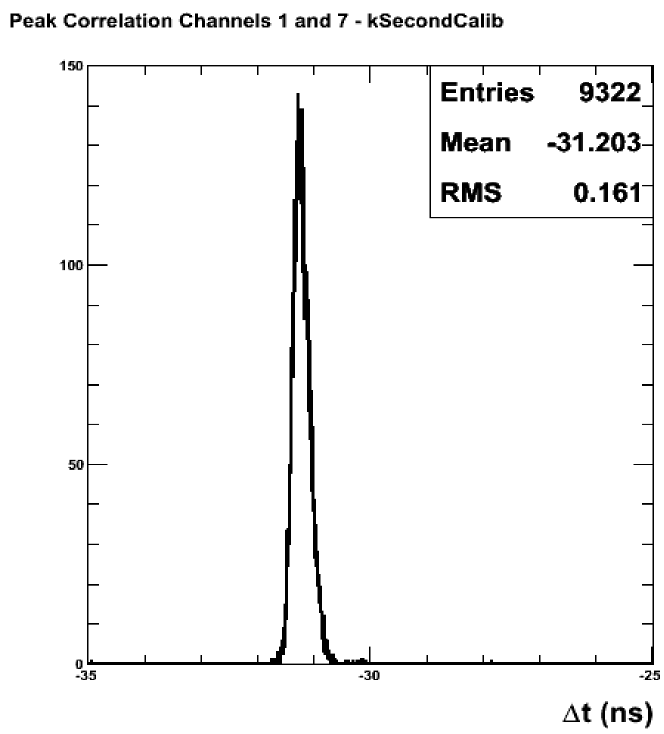
Pulser Data

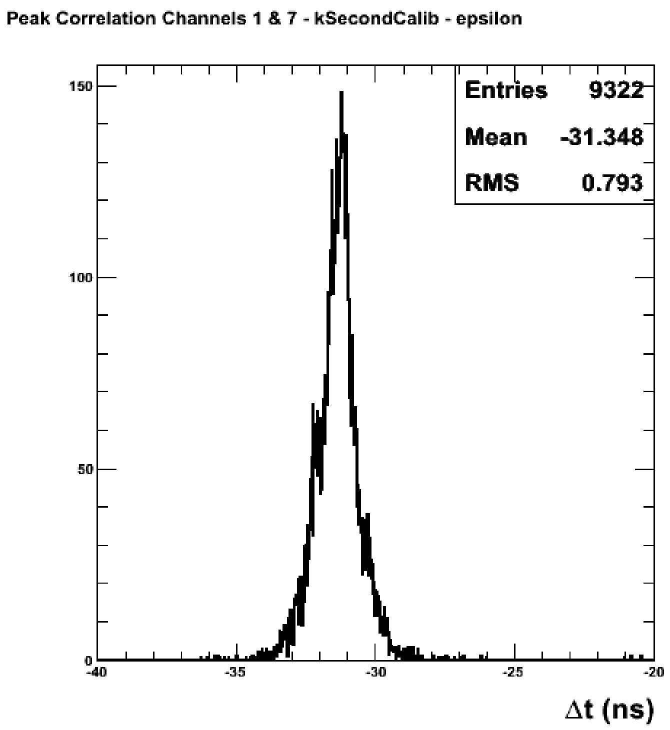
Correlate Channels 1 & 7 then look for timing offset of the peak correlation value



ARA Timing Calibration

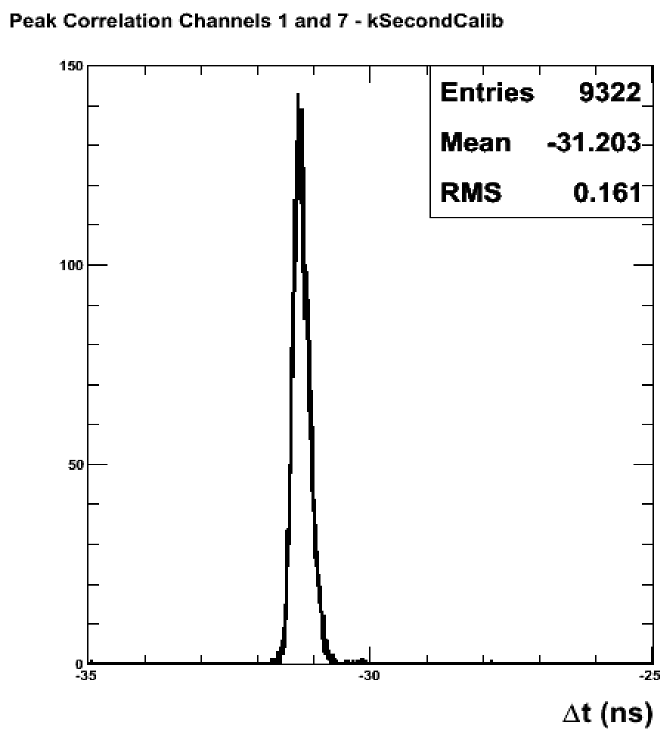
Pulser Data

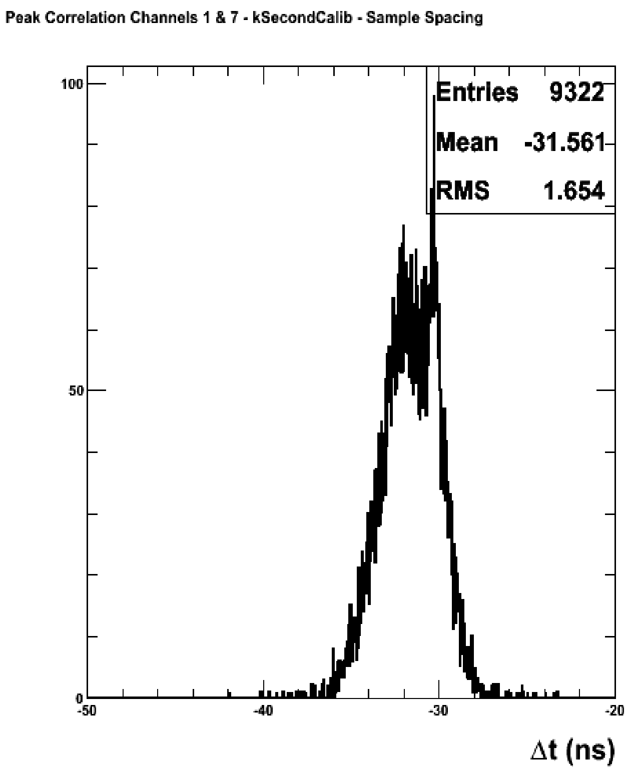




ARA Timing Calibration

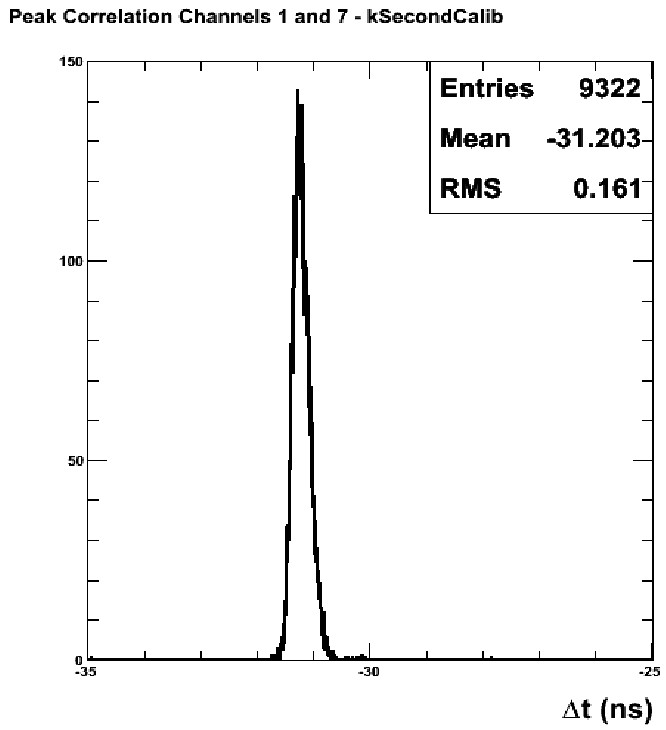
Pulser Data

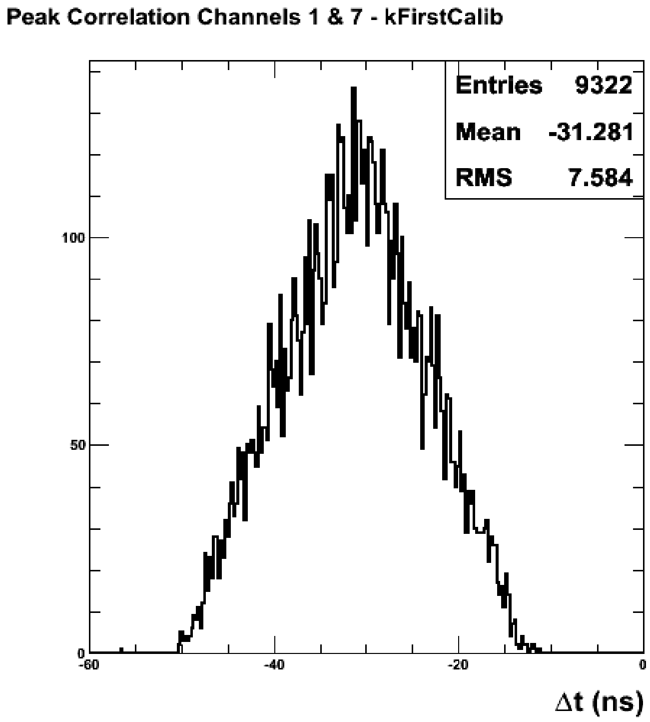




ARA Timing Calibration

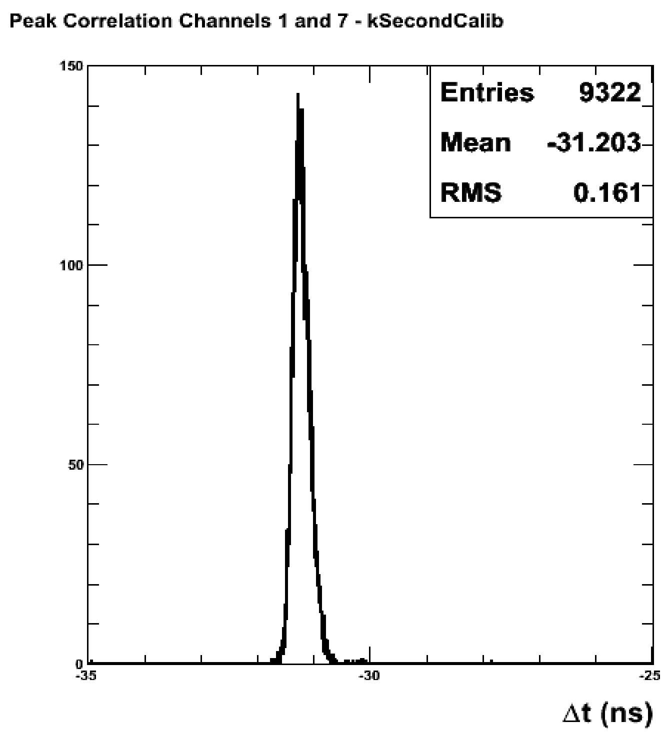
Pulser Data

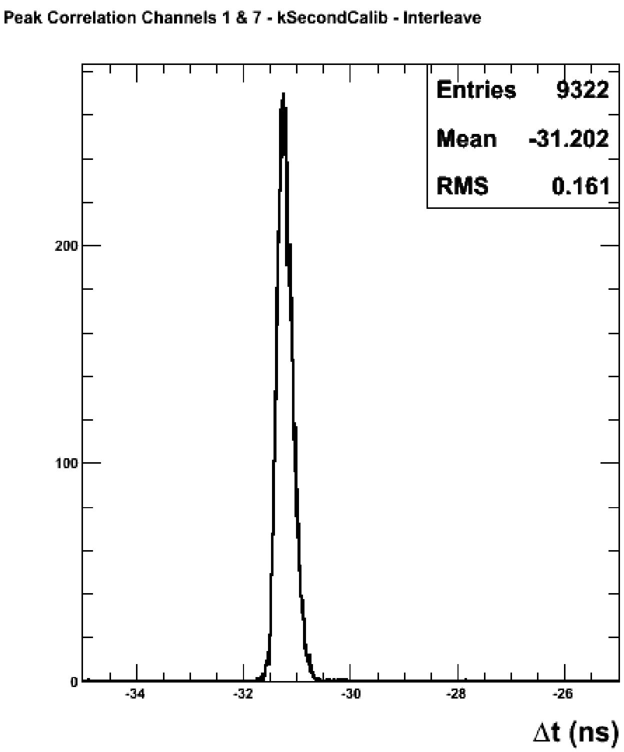




ARA Timing Calibration

Pulser Data





Looking at other ways of characterising this

ARA Timing Calibration

Conclusions

Electronics calibration seems to be working
The event to event jitter has the greatest impact ~ 7ns
Followed by time between samples ~ 1.8 ns and epsilon ~ 793ps

Looking at ways of better characterising interleave timing effects

Use kLatestCalib in your code as this contains the most recent calibrations

Further Work

Build on these calibrations to look at cable delays and further calibrations