ATRI rev B

PSA

Tested on Rev A

- FPGA powers up, programmable, JTAG is 3.3V
- Hotswap controller measures current/voltage and can turn off FPGA
- PCIe link works (with Rx/Tx switch)
- Clock multiplier works, outputs correct frequencies, can alternate between clocks
- USB I^2C interface
- GPS 1PPS output
- PPS input
- LVDS fanout (for CRSV0+/-)
- USB power/data switching
- USB-to-FPGA communication

Errata

- LTC4215 timer cap is too small – up to 2.2 uF
- EX5 conflicts with SBC – move out farther
- EX1-EX5 do not have shields grounded
- FX2LP footprint incorrect
- PCIe Rx/Tx swapped
- Input/output caps missing on FAN2514
- TPS2110 switches to wrong voltage with both plugged in
- Silkscreen for PPS LED wrong
- GPIO inputs to 74AC04 need pulldowns
- X1 (USB clock) has wrong pad layout (pin order)
- Pullups needed on EXPSCL[2:1] and EXPSDA[2:1] and pulldowns on EN[4:1] for PCA9518
- U16/U17 pass transistor design was stupid – replace w/ tristate buffer (74AUP1G125)

Other changes for safety…

- 0402 pad layout a bit too small – expand
- Straighten decoupling caps under Si5367 for layout
- Add fiducials opposite FPGA
- Add pin header for GPS serial (didn’t work out of the box) and 0-ohm jumper to FX2 serial port

Still left to do?

- Clean up FX2 devboard hack
- Install daughterboard connectors and test (tomorrow morning)
- Spin next rev of board
  - Hopefully coordinate so built/stuffed while I'm away – so beginning of June boards will be done

All board errata/documentation at:

http://ara.physics.wisc.edu/cgi-bin/DocDB/ShowDocument?docid=210