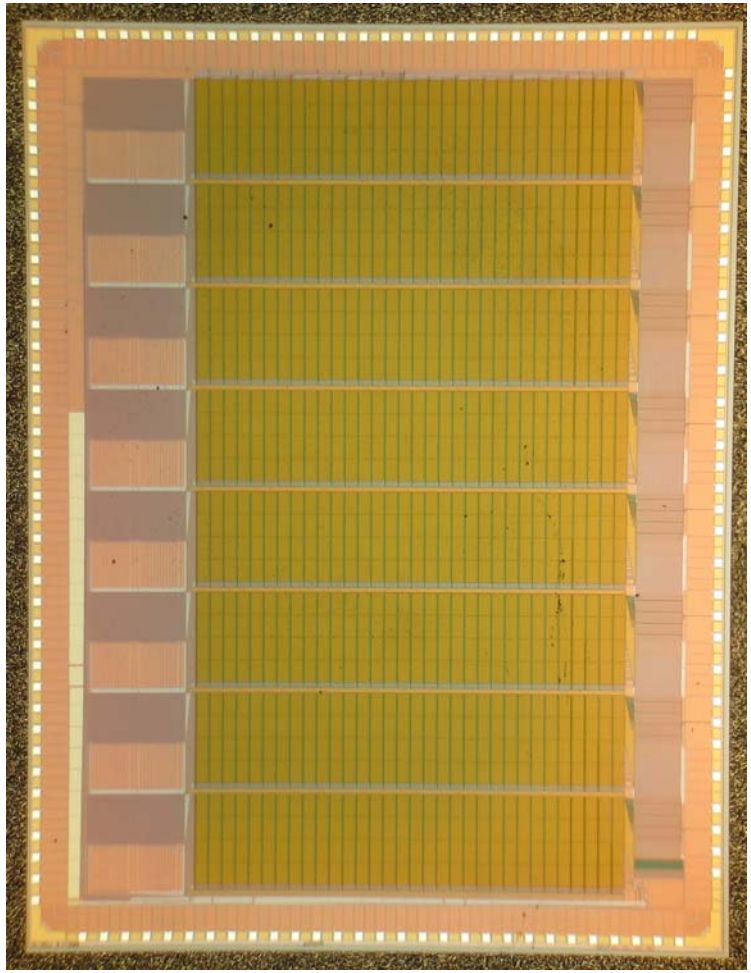
Station Overview, ARA Trigger & Digitizer

- Station geometry
- Triggering Overview
- Trigger Simulation
- Geometrical constraints
- Trigger rates
- Digitization &
- Data rates

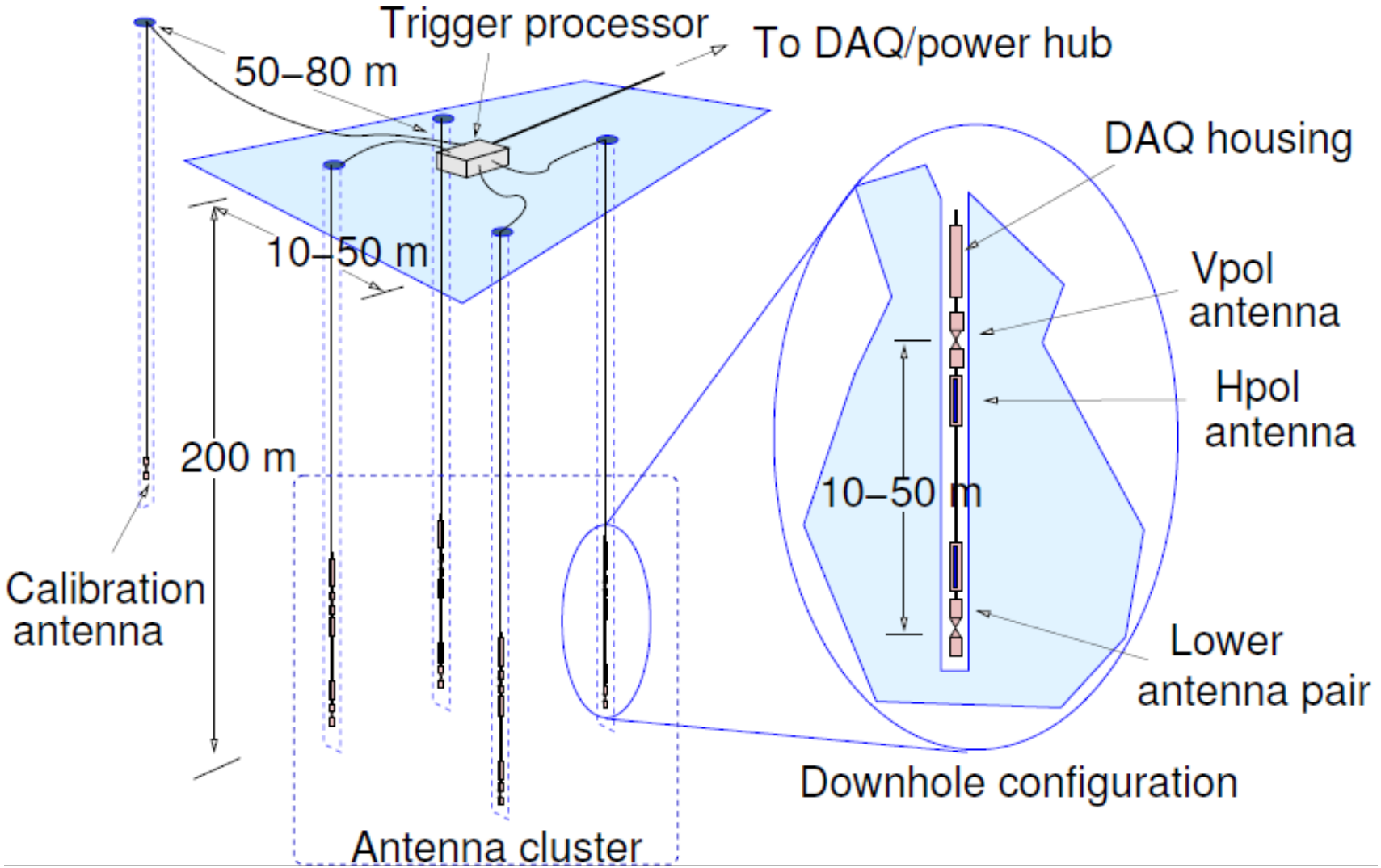


Gary S. Varner

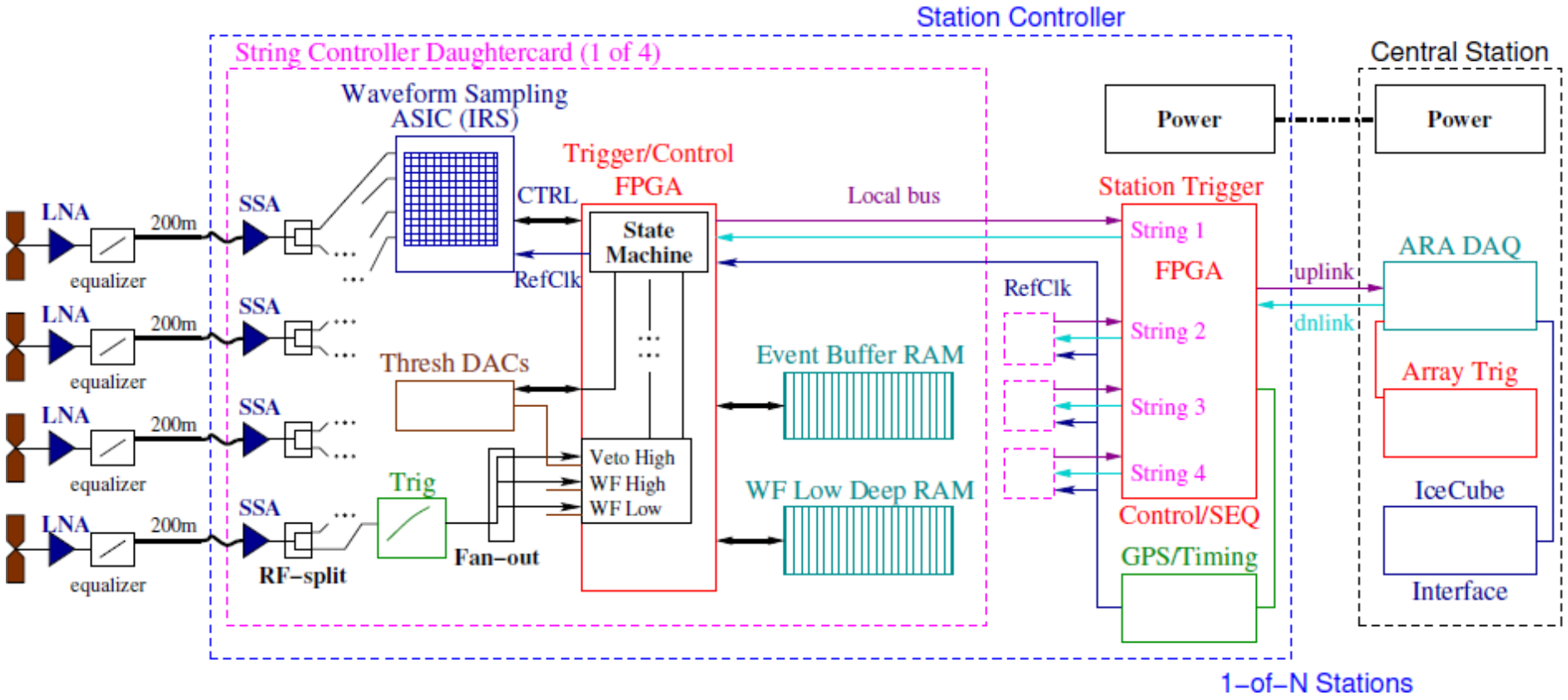
ARA Workshop in Honolulu, 17-AUG-10

Basic Station Geometry -- Initial

ARA Station & Antenna Cluster

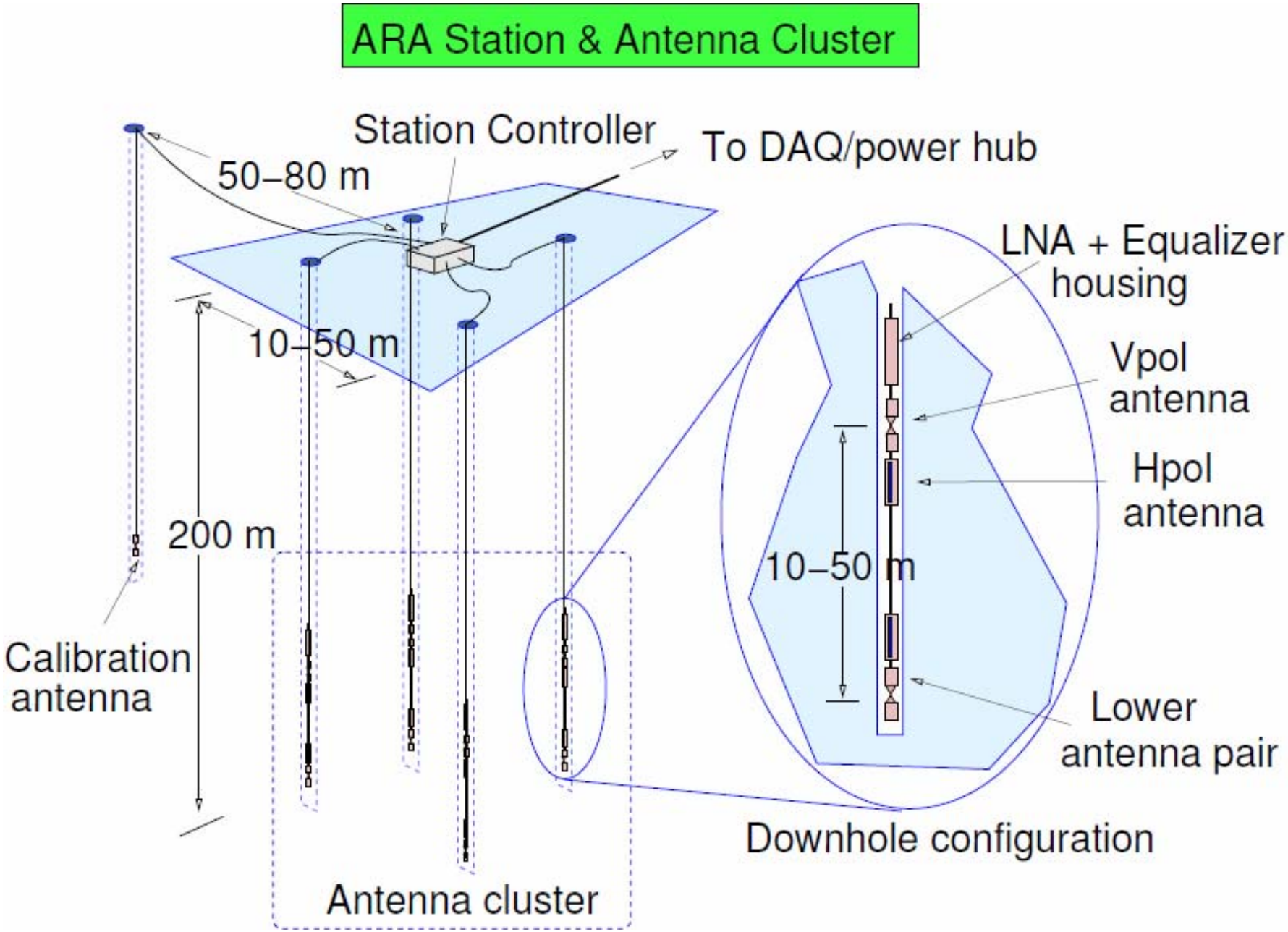


ARA Readout Electronics

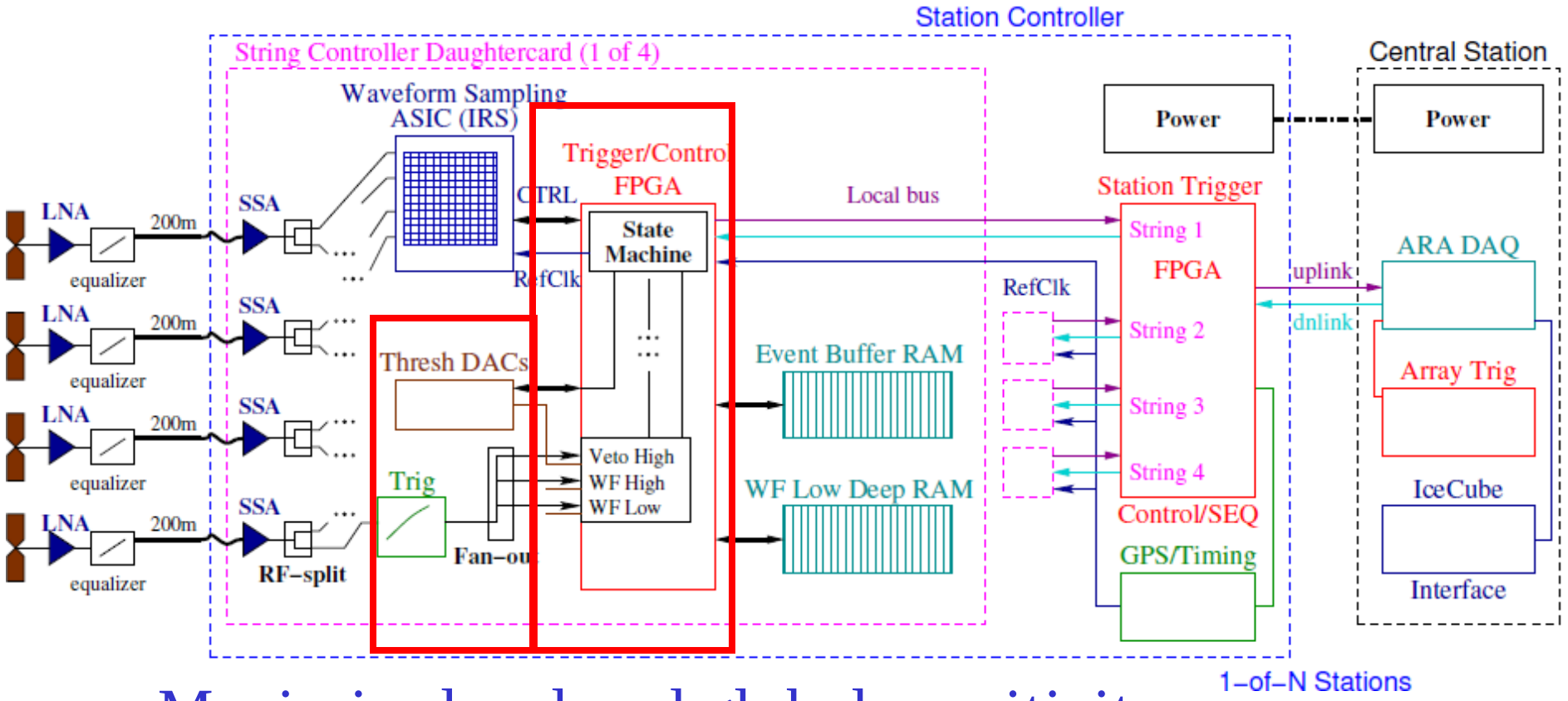


- Defer general discussion of architecture
  - Trigger update
  - ASIC (IRS) update

Basic Station Geometry -- Revised

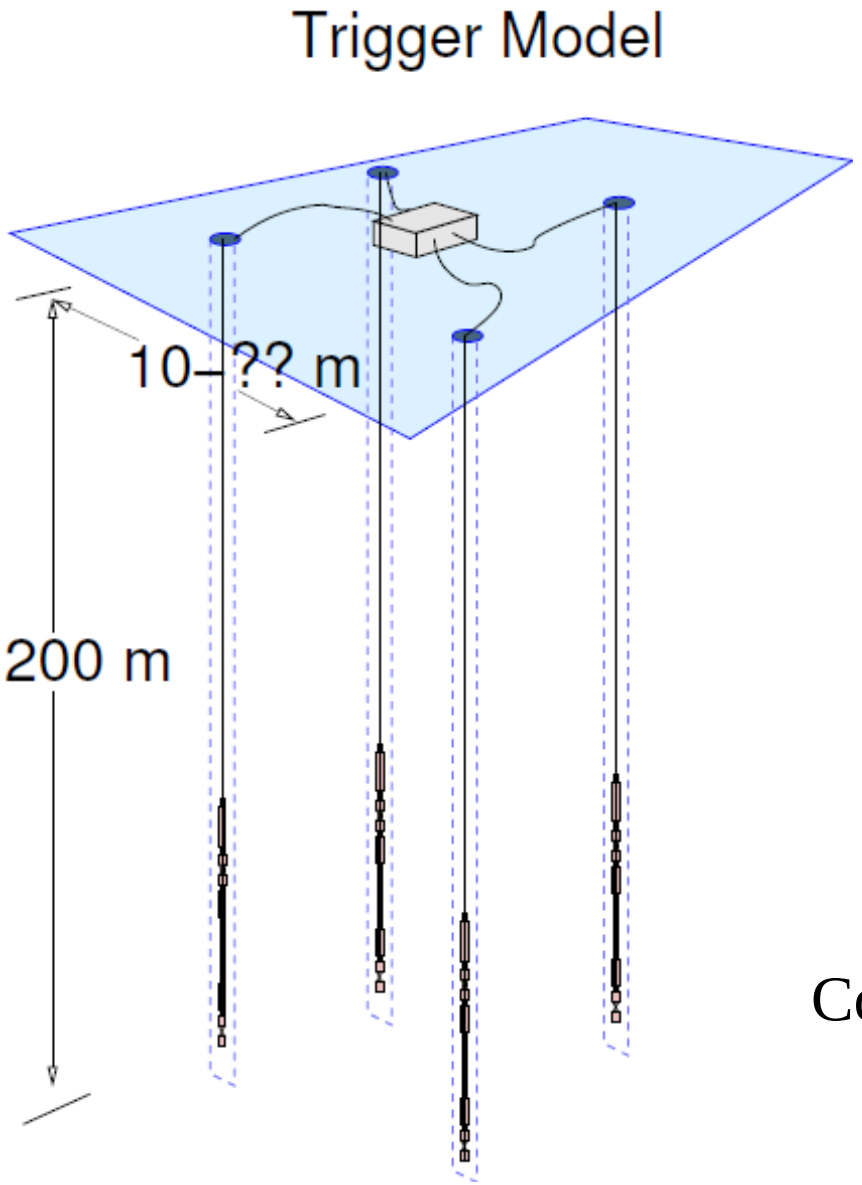


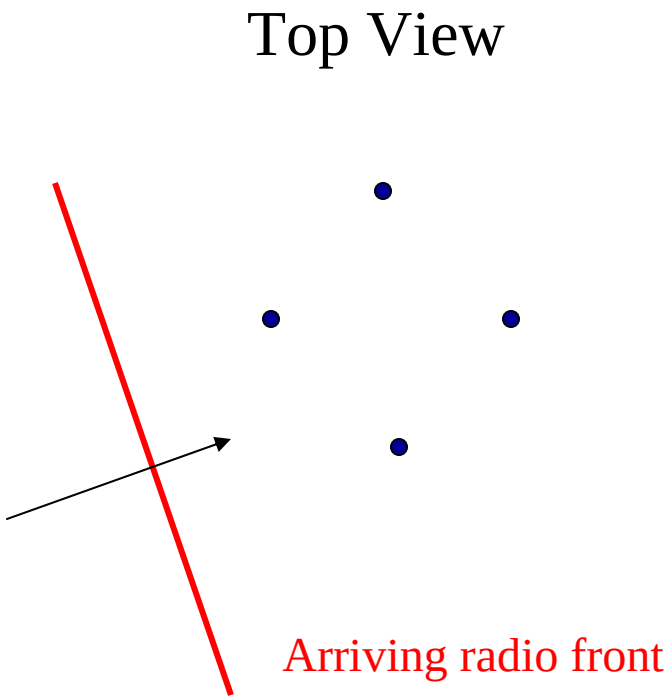
ARA Readout Electronics: Triggering



- Maximize local and global sensitivity
  - Station (few 100ns window) [local]
  - Array prompt (10's of us) [global, subthreshold]
  - High level (100's of seconds) [global, WF low threshold]

Geometric Considerations

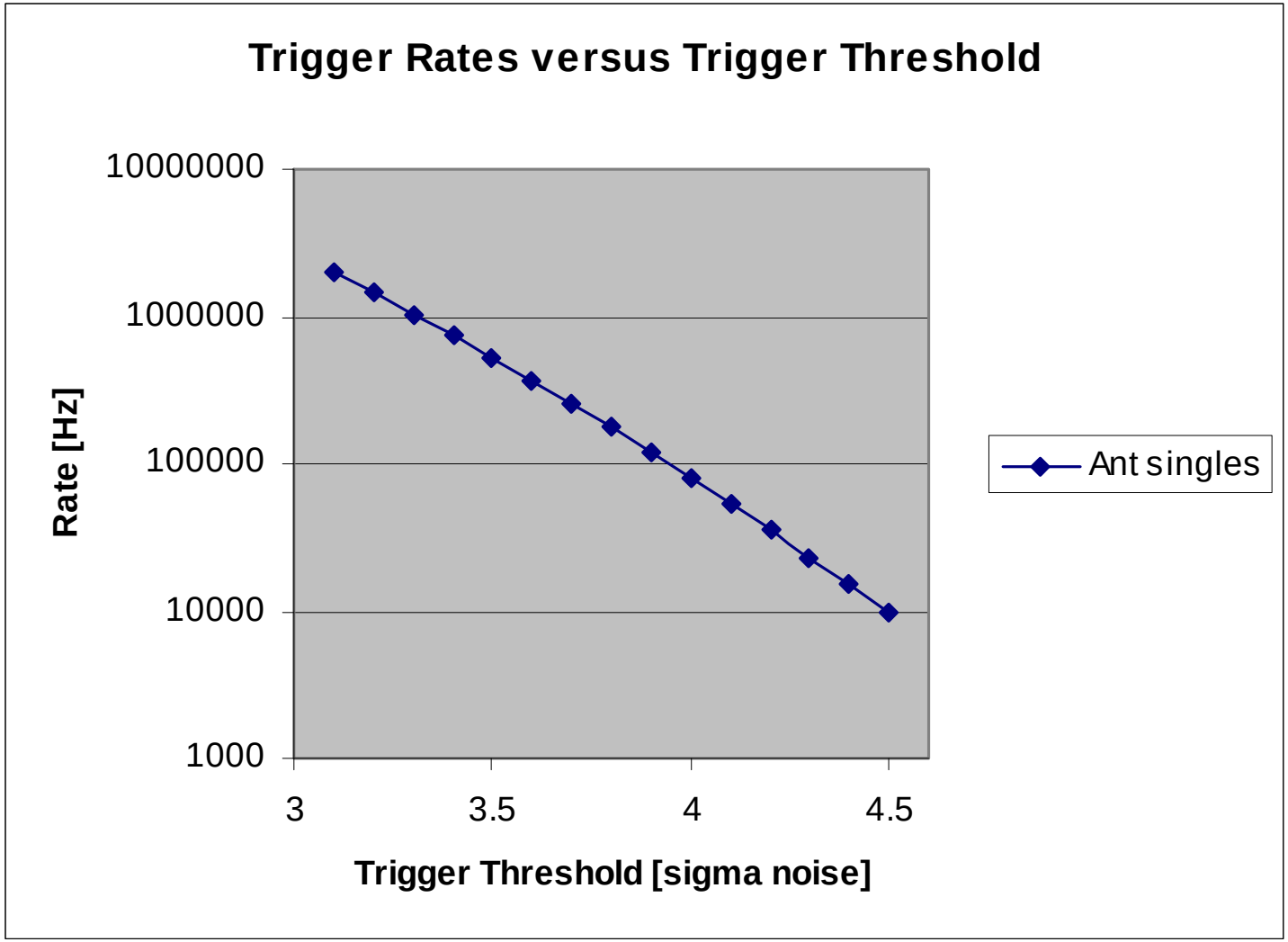




Consider simple coincidence – as a function of string spacing

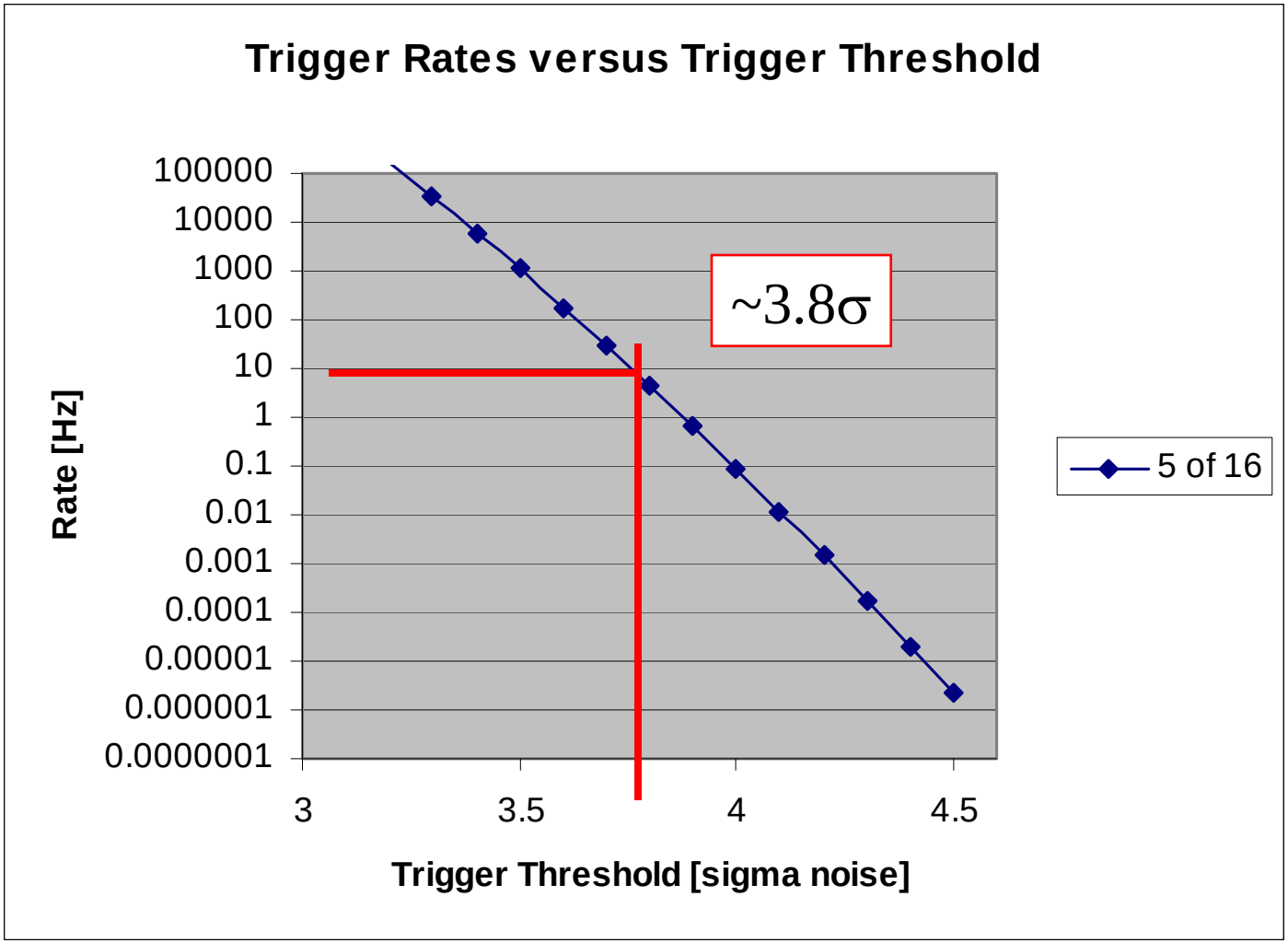
Single Antenna “singles” rates

- Raw rates

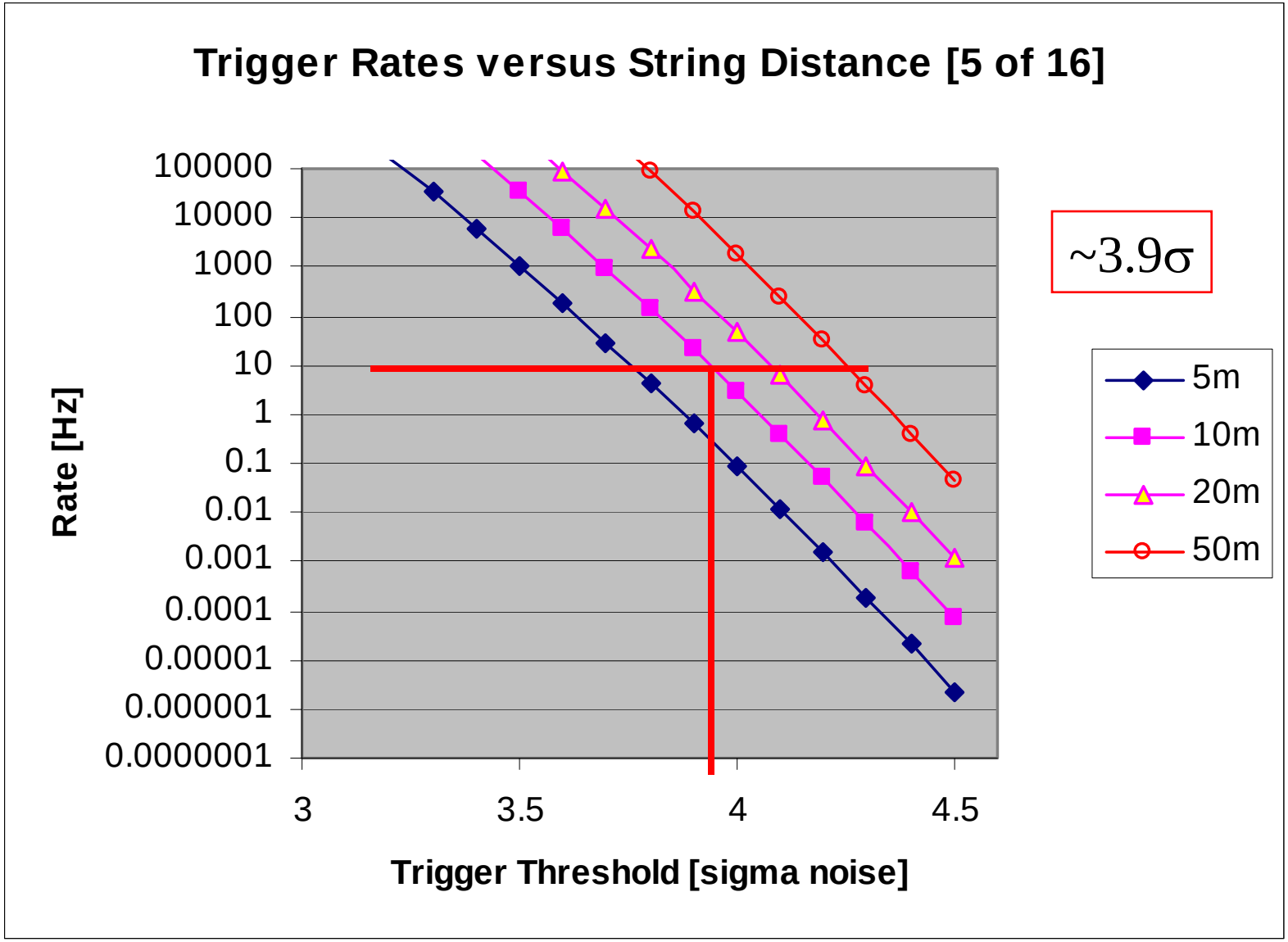


Station coincidence

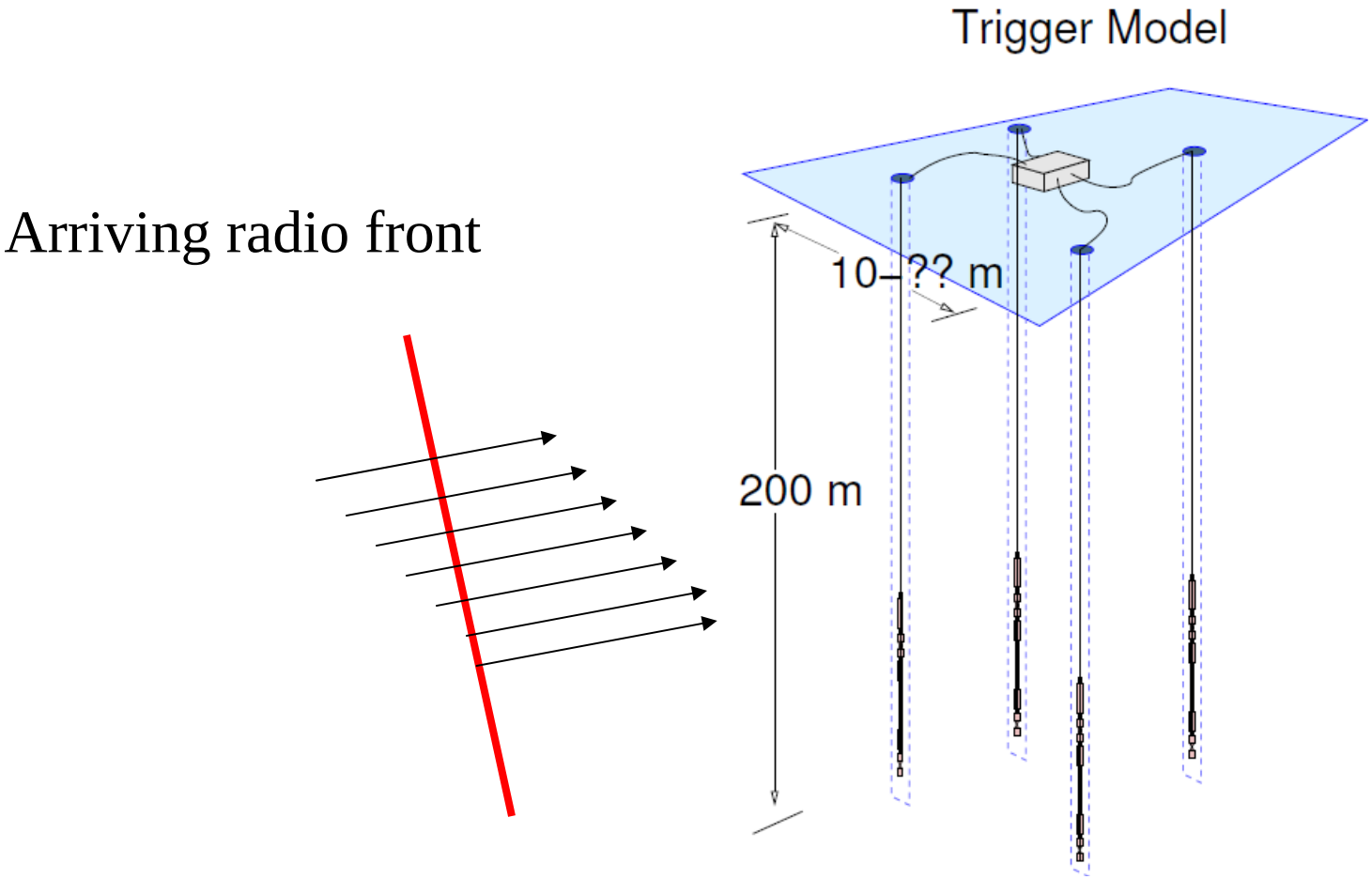
- 5 m “tight” spacing (50ns window)



Station coincidence



Additional constraint: causality

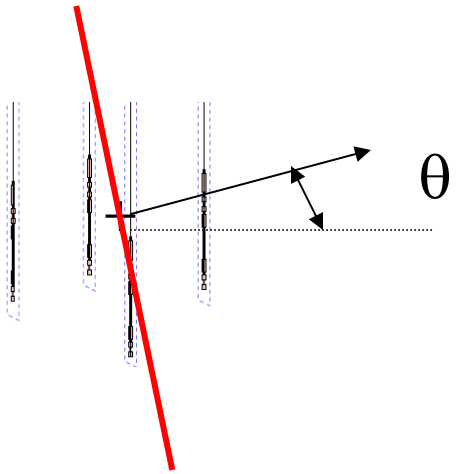


Use temporal/spatial constraints to reduce incoherent thermal accidentals and reject pathological directions (e.g. surface noise)

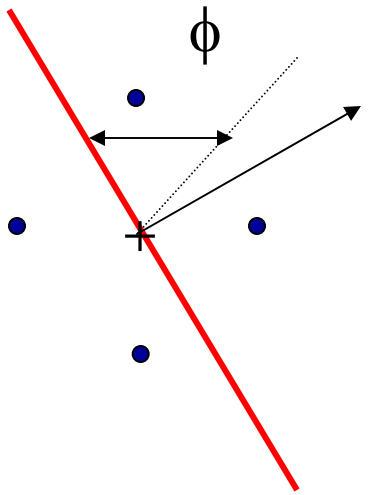
Implemented as a 2D sliding window

Simplified coordinates

Side View

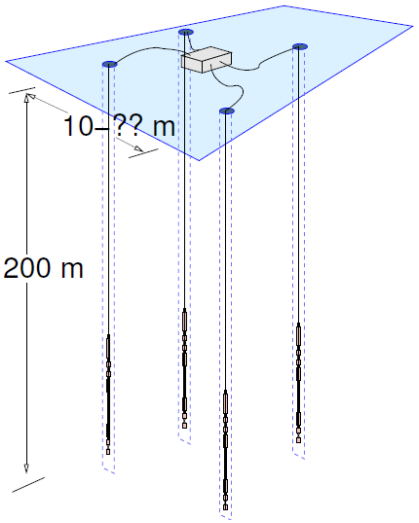


Top View

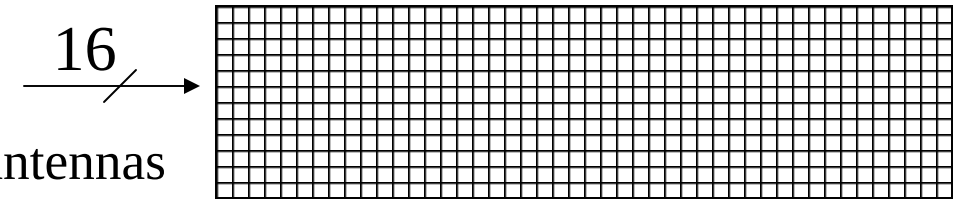


Arriving radio front

Trigger Model



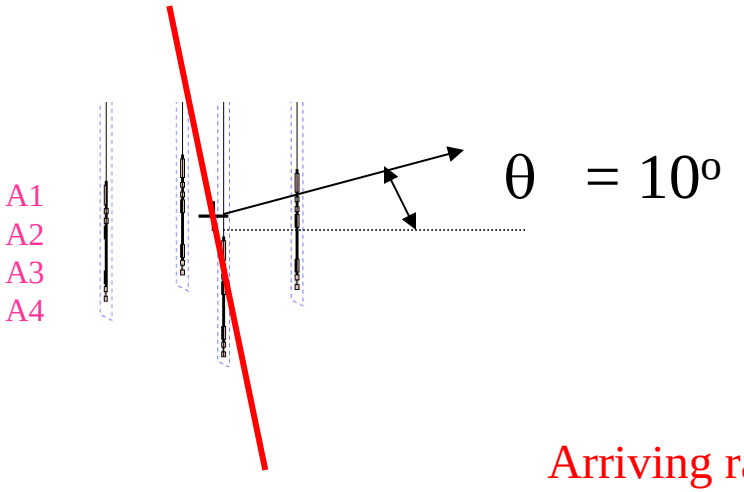
Antenna hits quantized with 4ns resolution (250MHz pipeline)



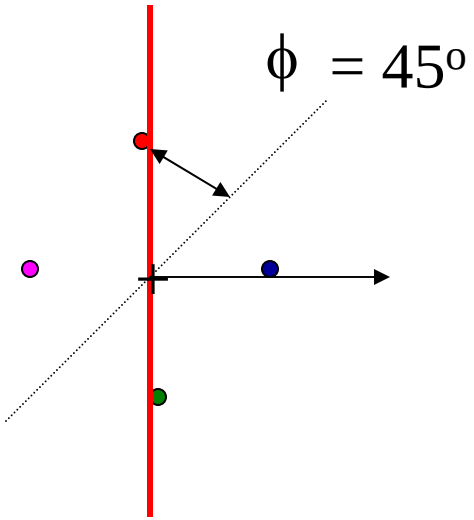
N time bins (32 for 128ns)

Example – strong nu signal

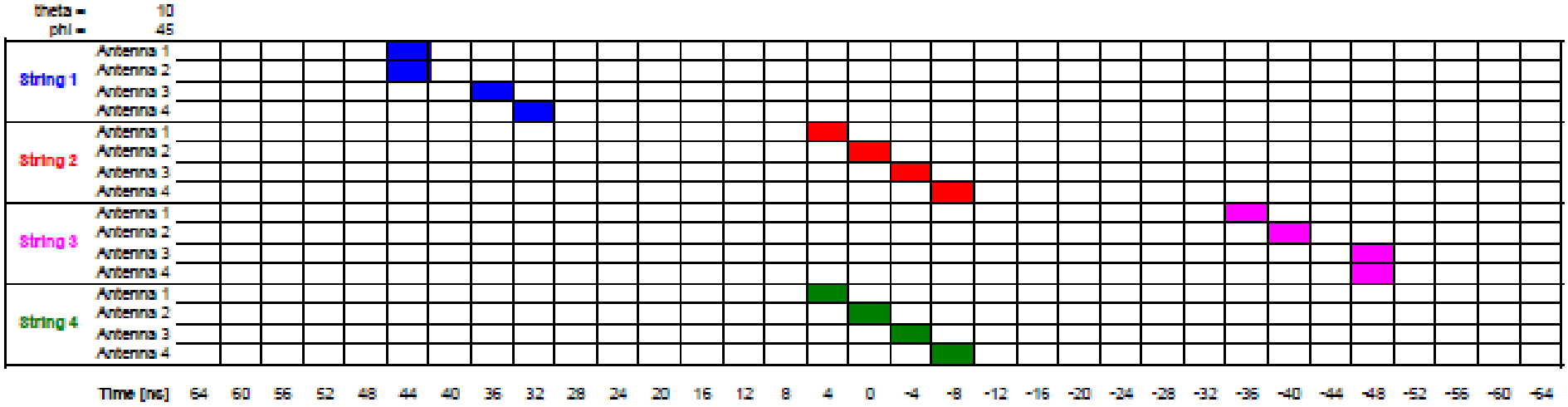
Side View



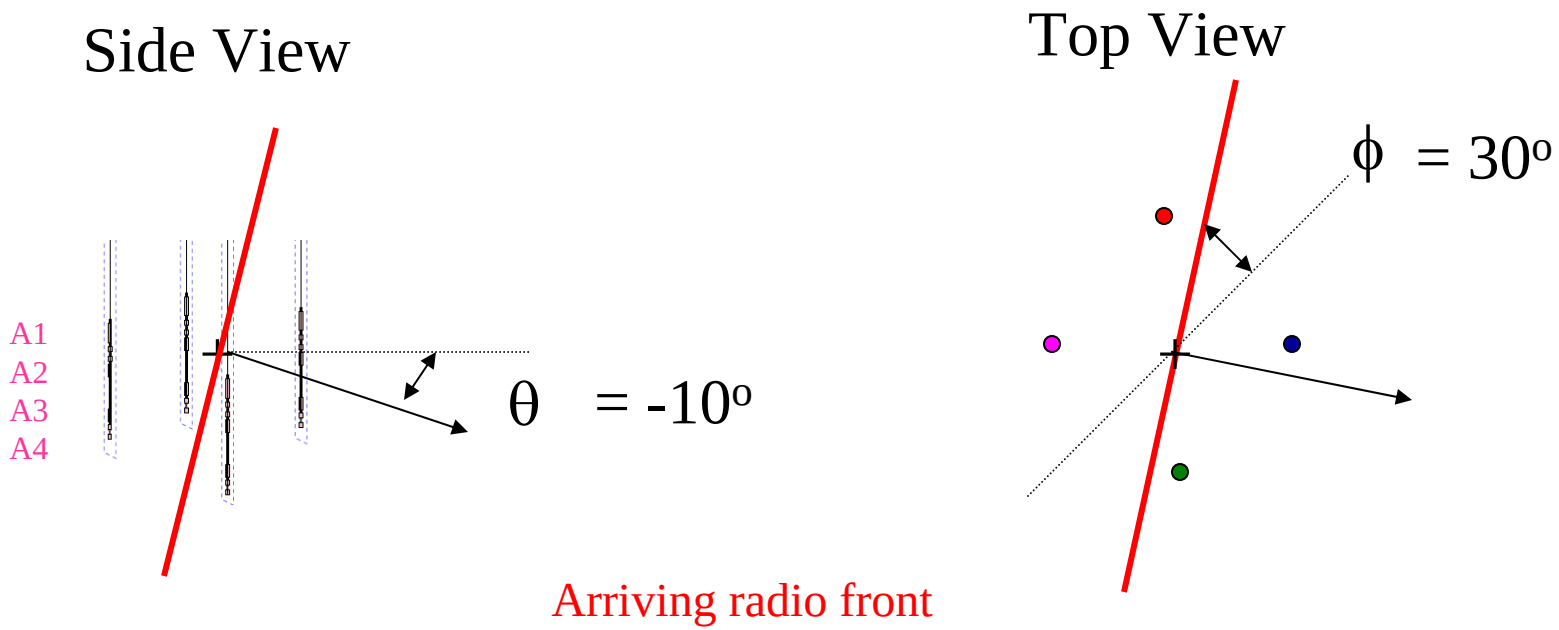
Top View

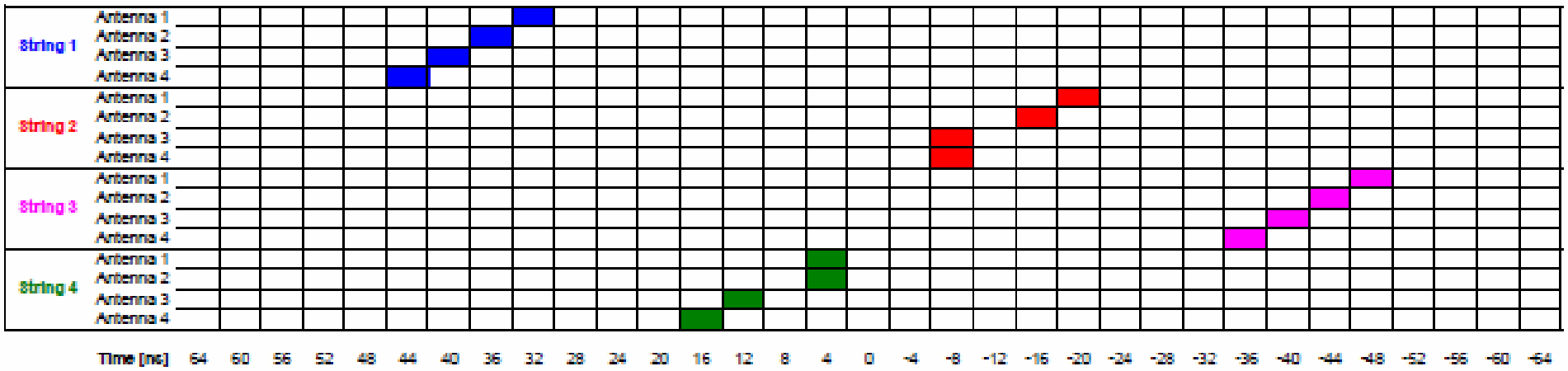


Arriving radio front



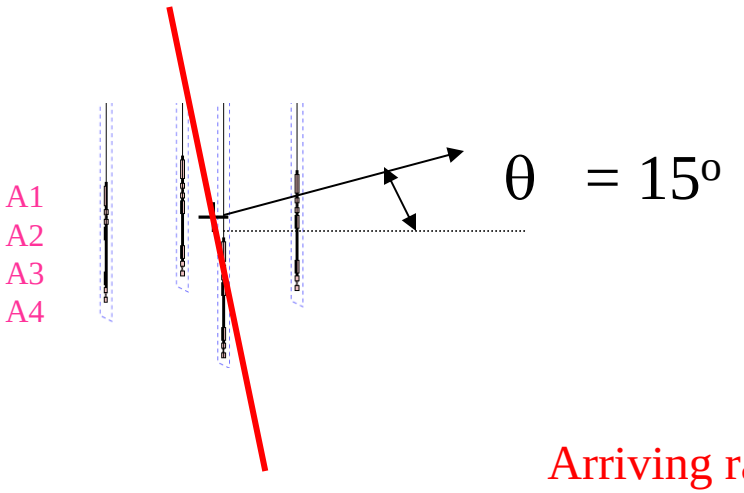
Example – strong signal (e.g. ICL)



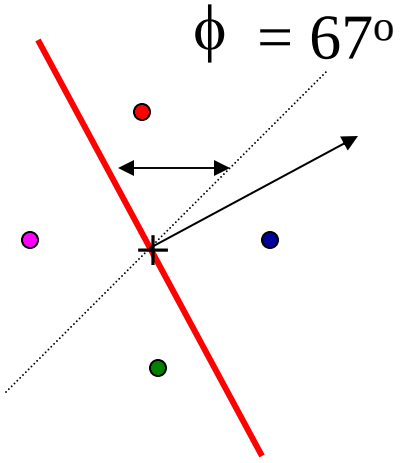


Example – at threshold nu signal

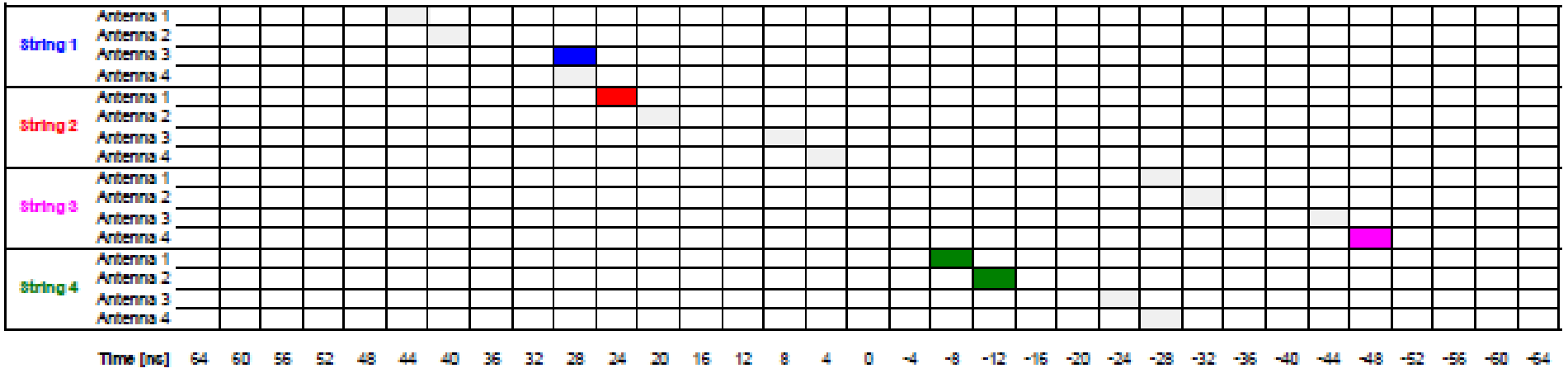
Side View



Top View

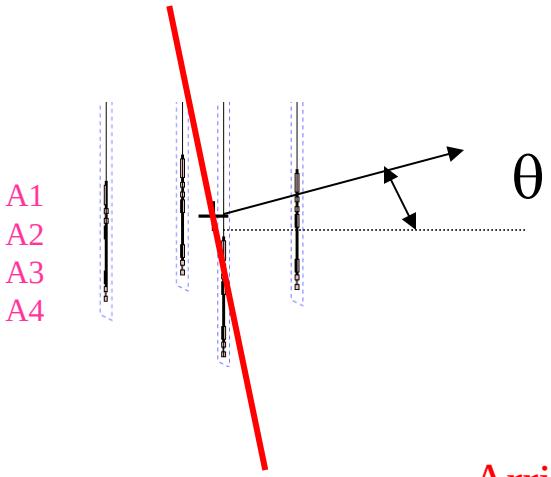


Arriving radio front

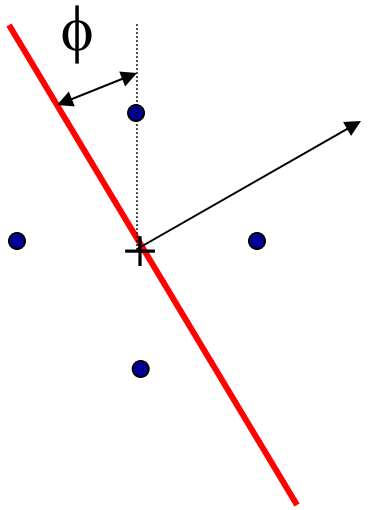


Thermal Noise (~10MHz singles)

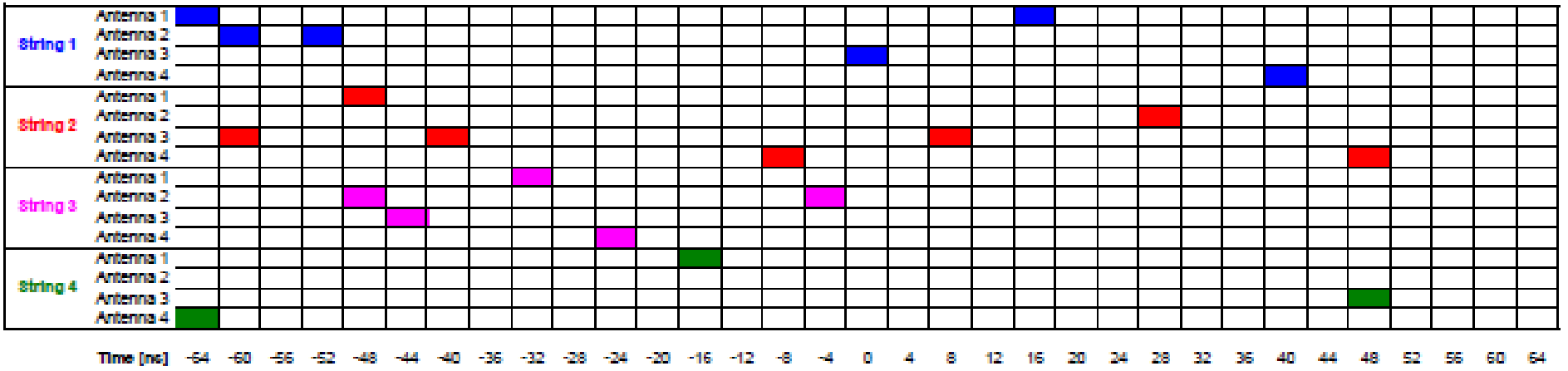
Side View



Top View

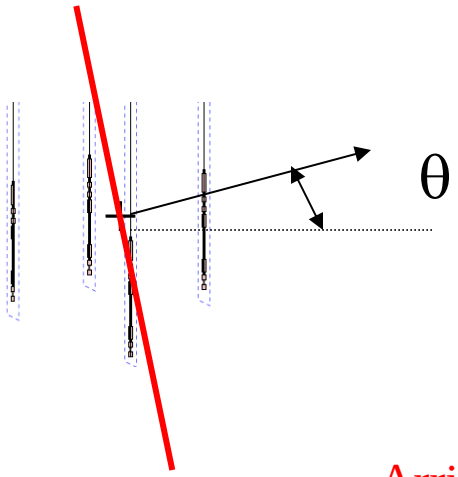


Arriving radio front ??

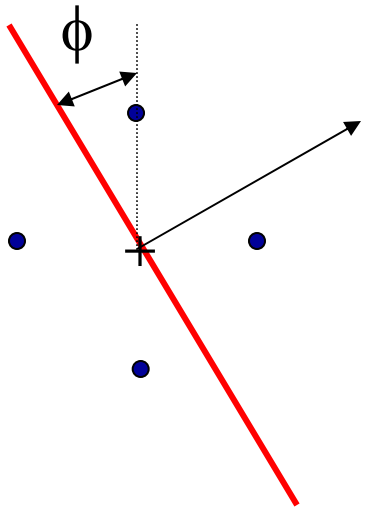


Thermal Noise (~3.x sigma)

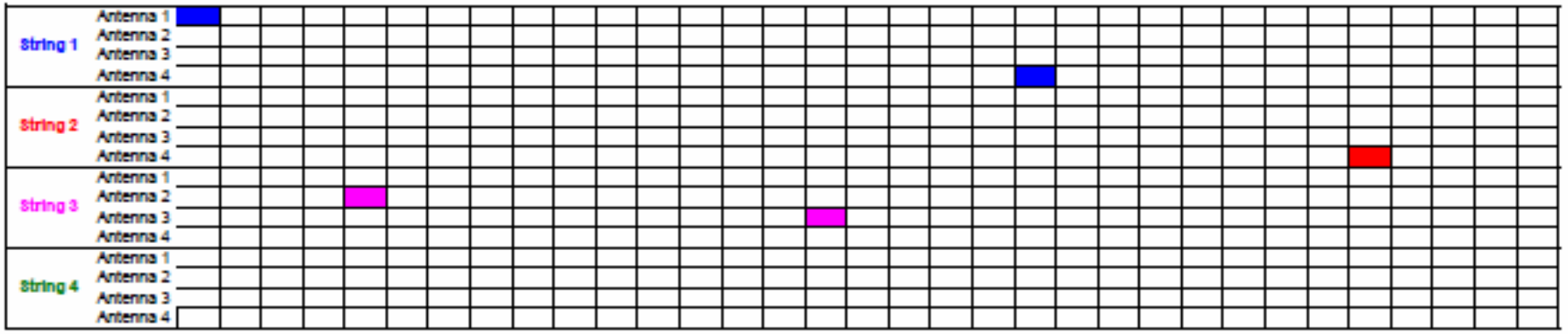
Side View



Top View



Arriving radio front ??



Combinatorics are enormous (C[512,5]=512!/(5!*(512-5)!))

How to implement?

1. Track “road” search? (computationally intensive)
2. Step time thread logic
3. Fit to plane wave (again CPU heavy)
4. Brute force pattern match?

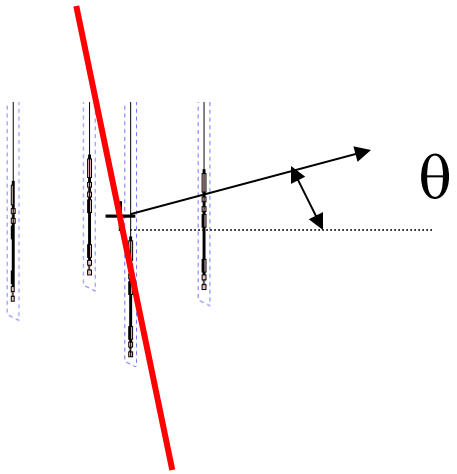
   – 2^(16+32) ~ 280 Terabits (very sparse)

Direct logic search – programmable logic good at this

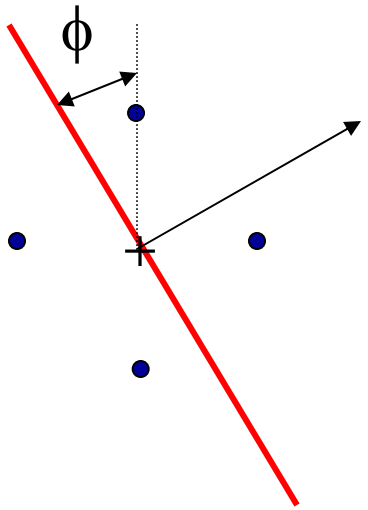
Use “5th” (last hit as seed)

Divide up sky into arrival directions

Side View



Top View



Arriving radio front

Many downgoing directions pathological

With quantization, something like

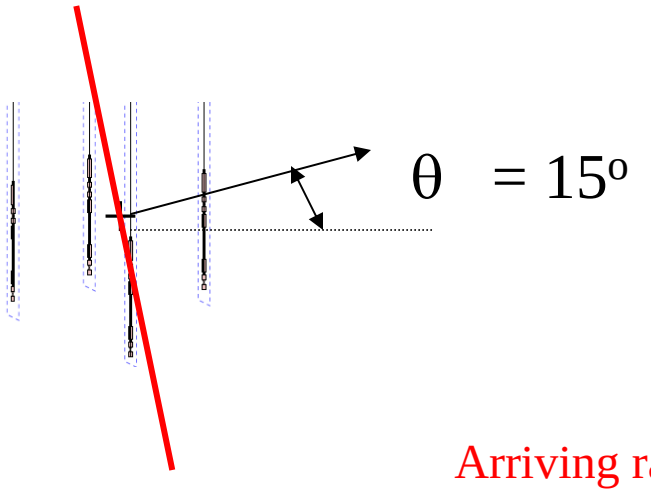
Something like 5^o θ 36

Something like 10^o ϕ 36

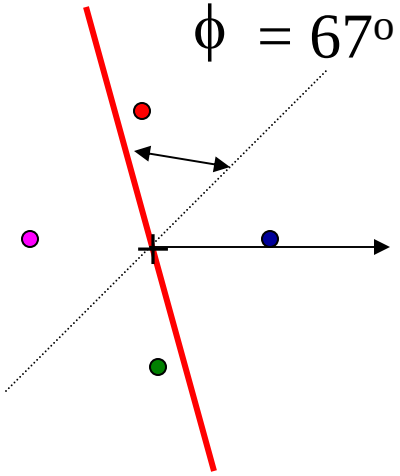
} 1296 equations

Example – at threshold nu signal

Side View

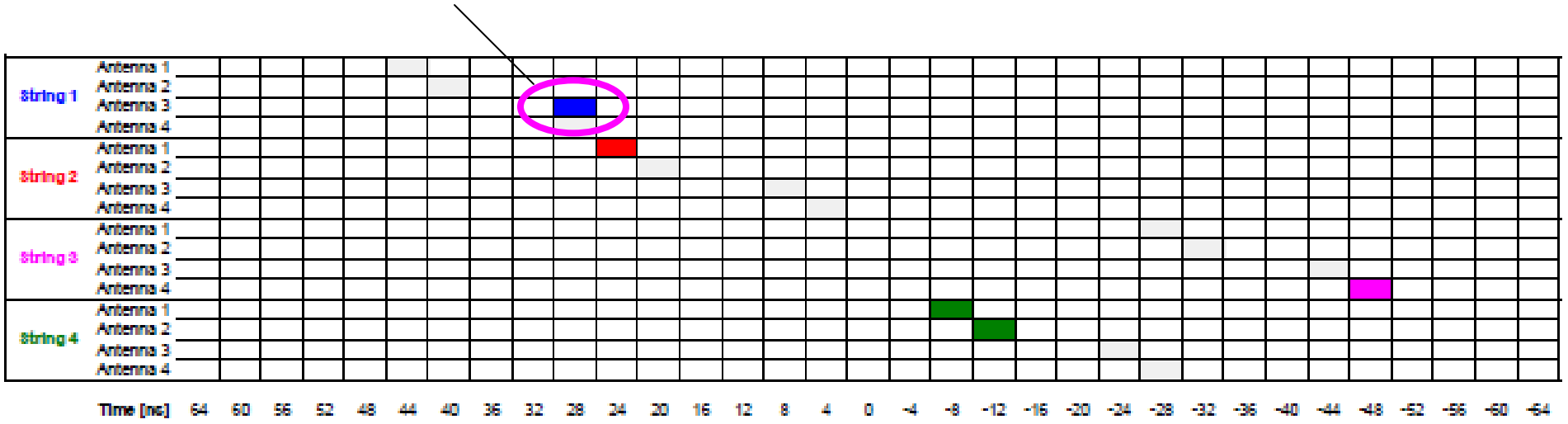


Top View



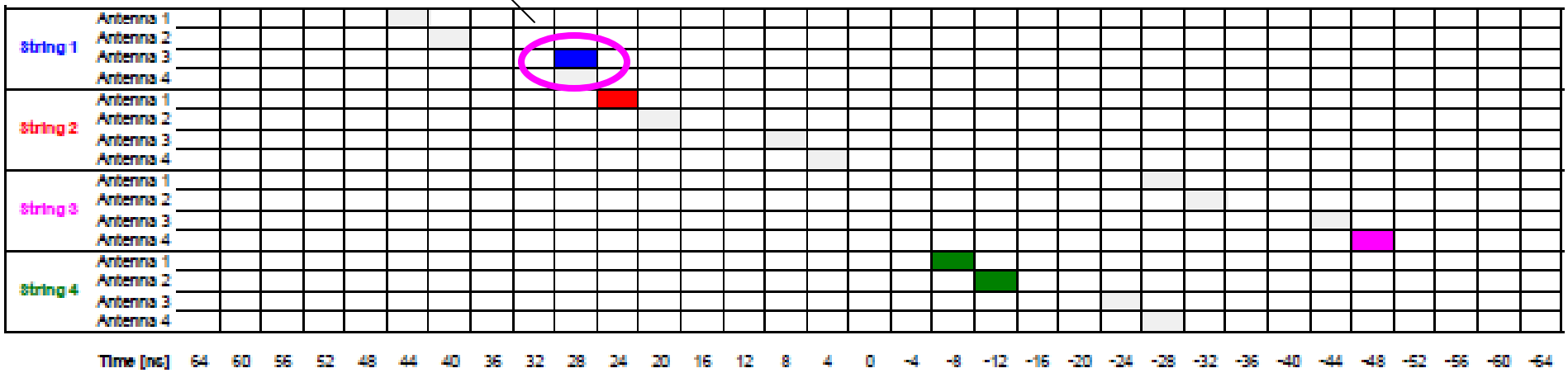
Arriving radio front

Hit search seed



Example – at threshold nu signal

Hit search seed



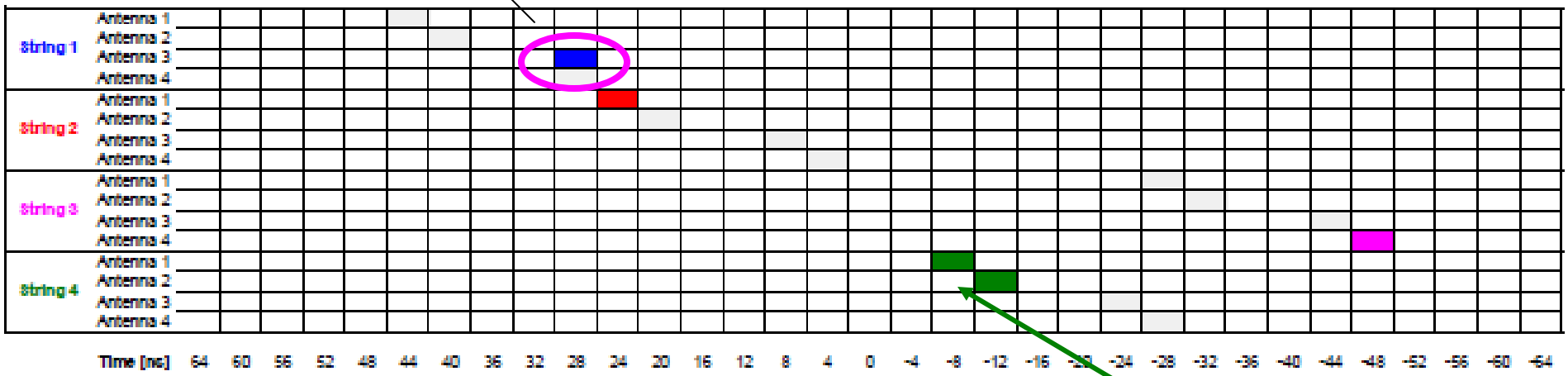
Term of equation:

Hit = S1A3[0]*S2A1[1]*S3A4[19]*S4A1[9]*S4A2[10]

Build terms from MC

Since degenerate – some OR terms

Hit search seed



Reduce Terms of equation:

Hit = S1A3[0]*S2A1[1]*S3A4[19]*S4A1[9]*(S4A2[10]+S4A2[9])

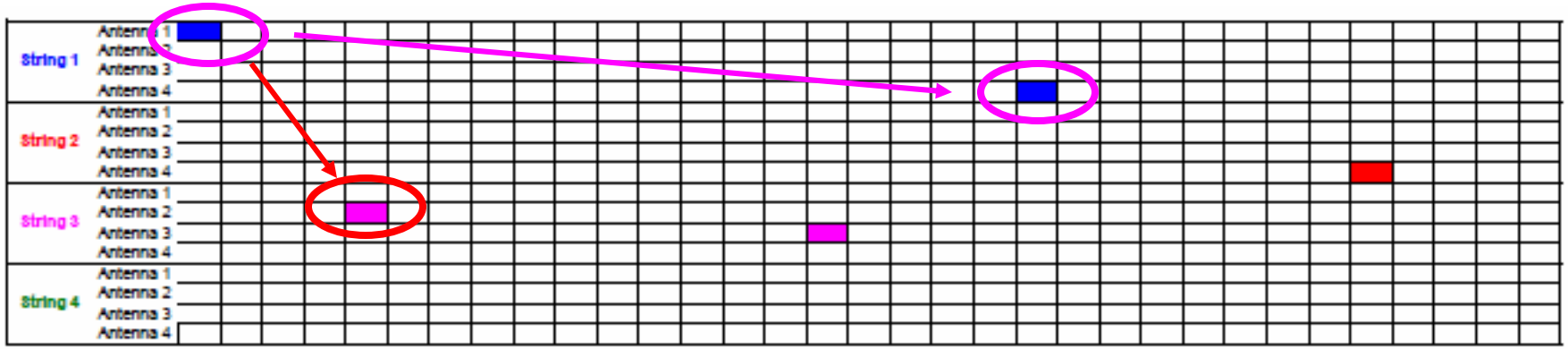
Needs detailed study, but can guesstimate:

16 ant seeds * (16 theta * 8 phi) * 32 patterns ~ 65k terms

Thermal Noise (~3.x sigma)

seed

Physically impossible



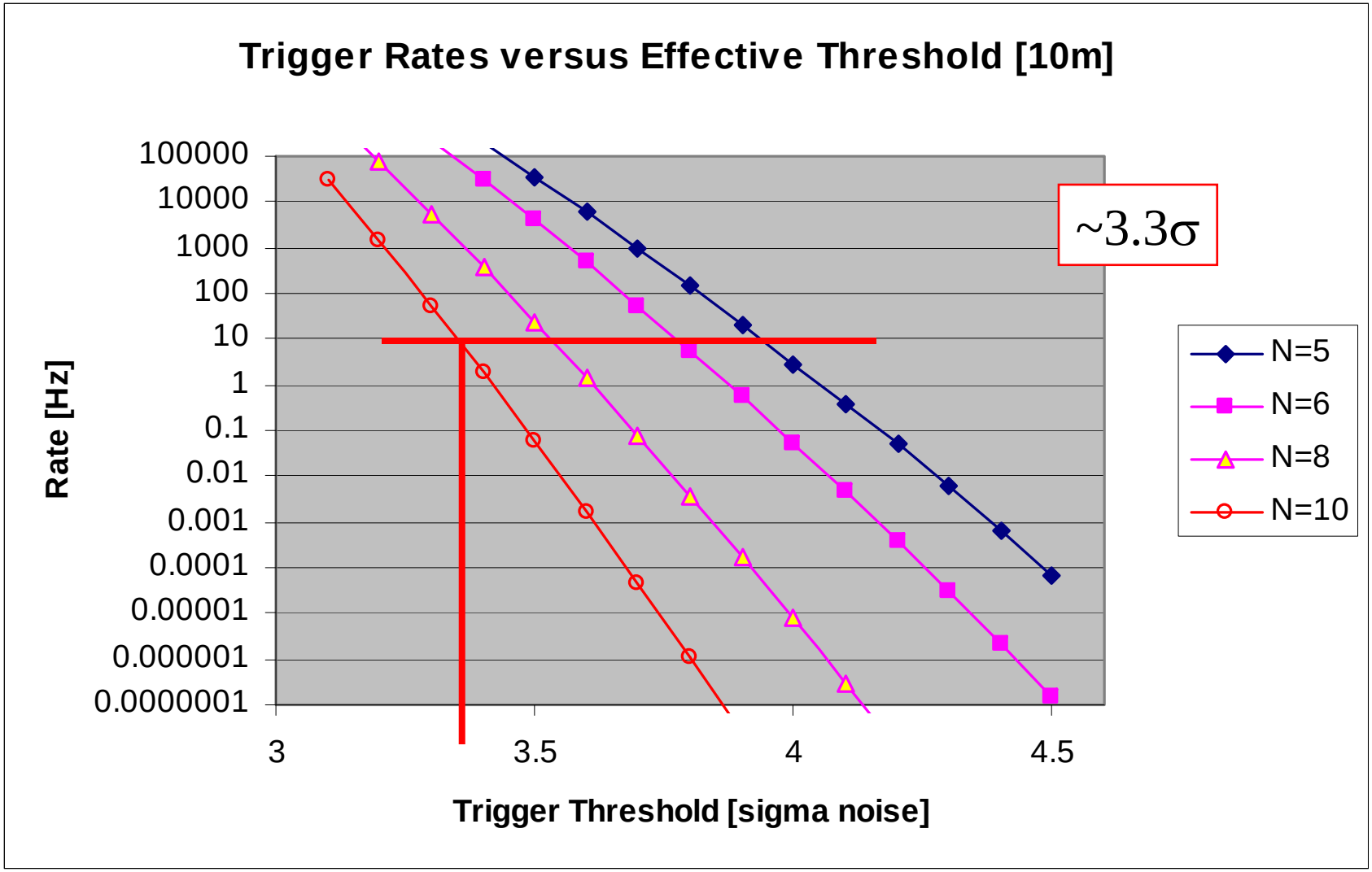
Hit predicts allowed other times

Combinatorics are enormous

One way to think of this: can tolerate a larger number of spurious hits

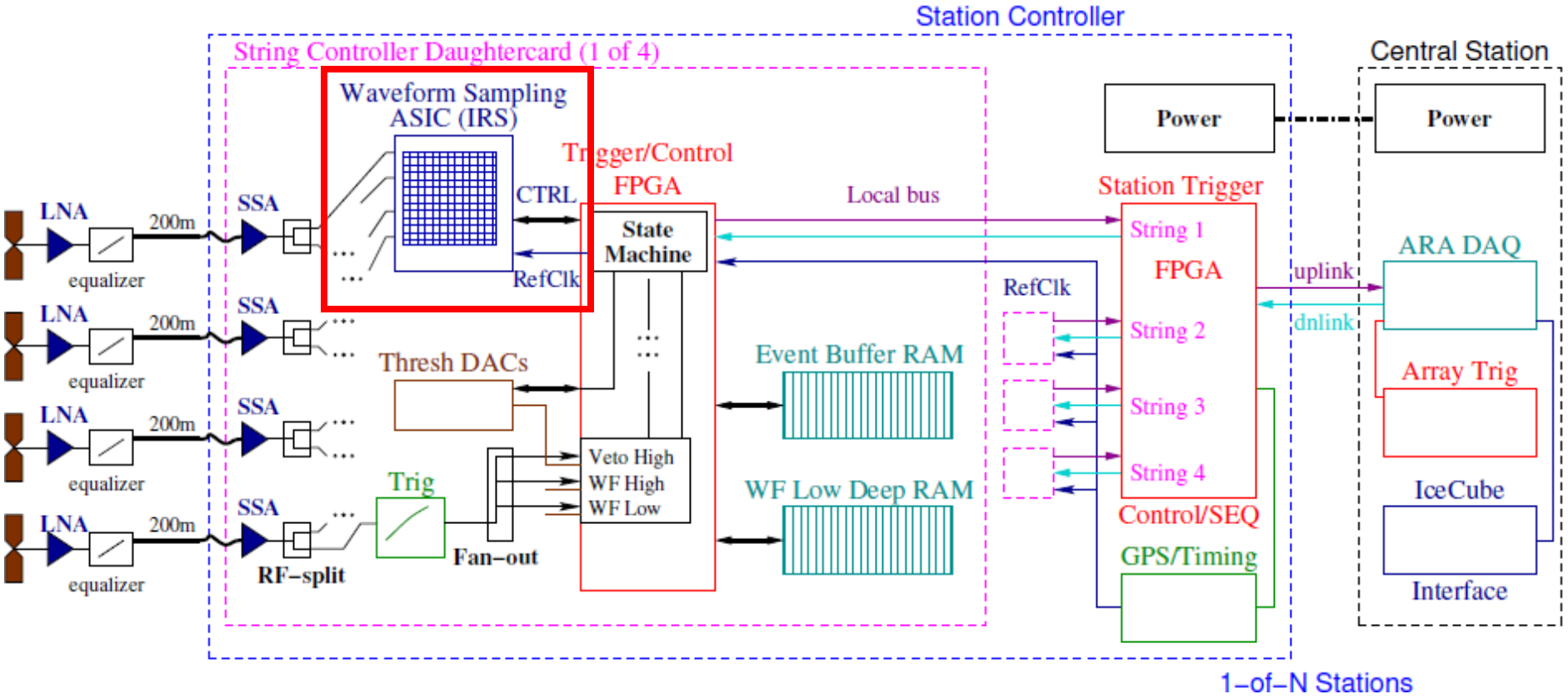
→ Effectively raise coincidence level in the window

Station coincidence



Looks promising – Lisa to continue…

ARA Readout Electronics: ASIC



- Build on experience with “next generation” ASICs
  - Deeper storage depth, higher bandwidth?
  - Fewer timing alignment constants

Ice Radio Sampler (IRS)

- Actually a fairly generic part
  - Follow-on evaluation of deeper storage [TARGET, others] (LABRADOR technology now >half decade old)
  - "2 stage" transfer mechanism (reduced calibration)
  - No amplifier on the input
  - Self-trigger capability (not useful this application)

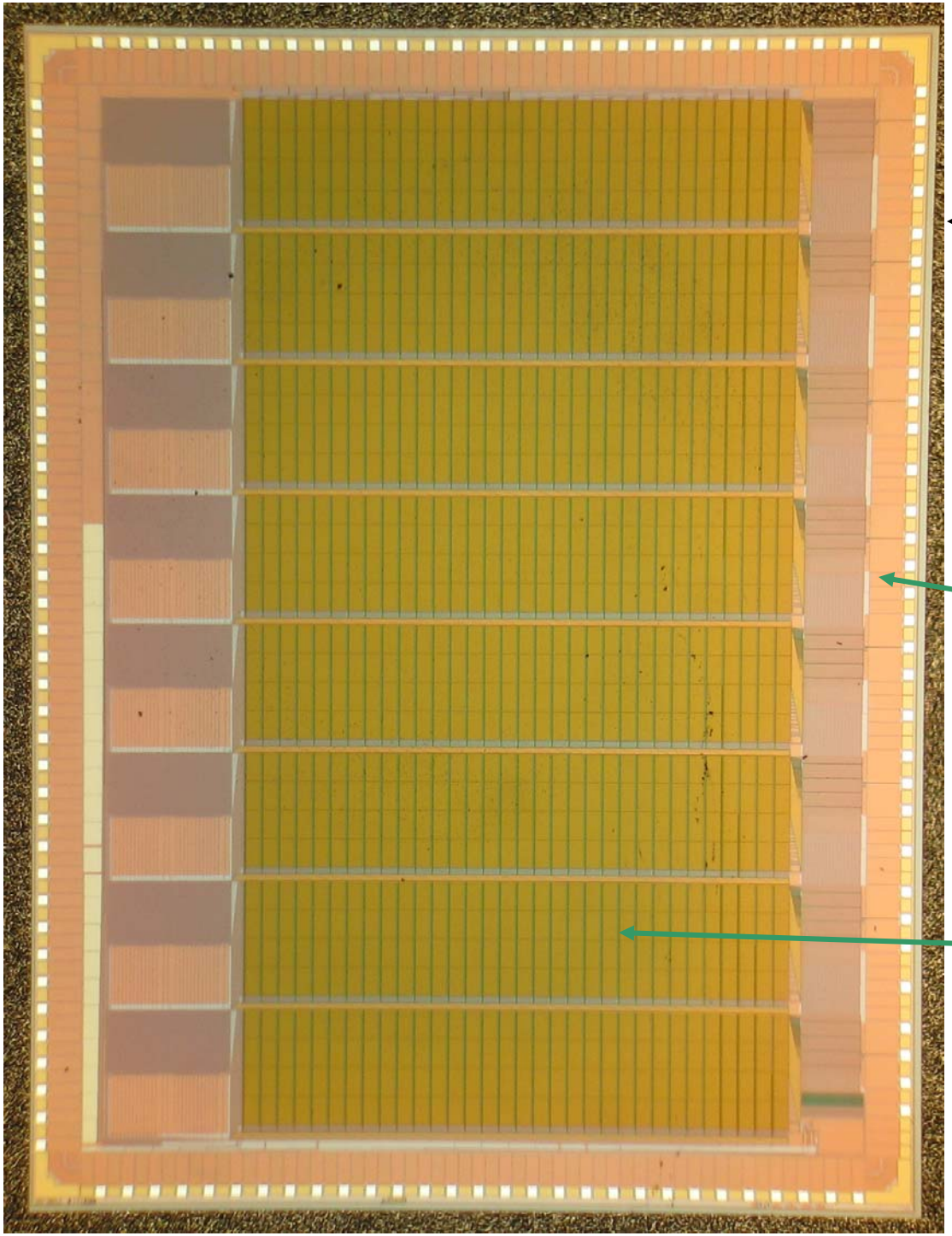
Collaborative effort with NTU

Ice Radio Sampler (IRS) Specifications

32768	samples/chan (16-32us trig latency)
8	channels/IRS ASIC
8	Trigger channels
~9	bits resolution (12-bits logging)
64	samples convert window (~32-64ns)
1-2	GSa/s
1	word (RAM) chan, sample readout
16	us to read all samples
100's	Hz sustained readout (multibuffer)

- Strictly only 5 channels necessary
  - 4x antenna, 1x reference channels
  - Could interleave for twice depth, or multiple reference channels

IRS Floorplan



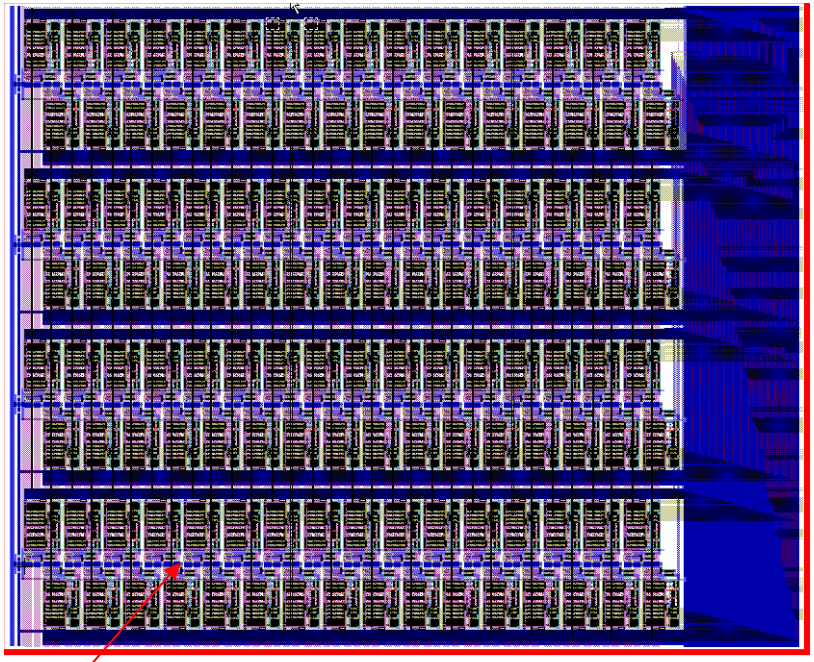
5.82mm

7.62mm

8x RF inputs
(die upside down)

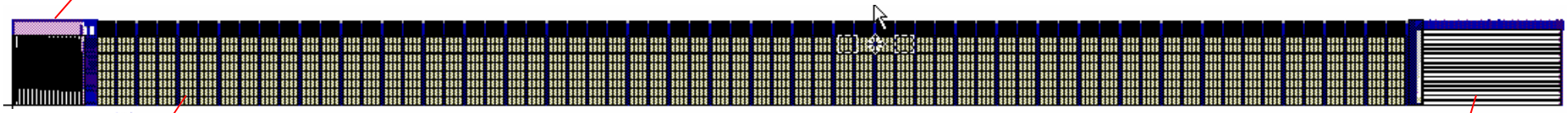
32k storage cells
per channel
(512 groups of 64)

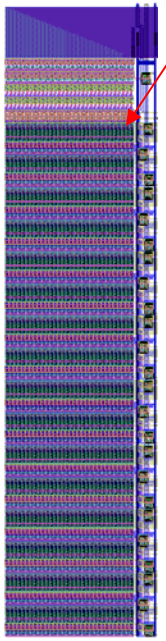
IRS Single Channel



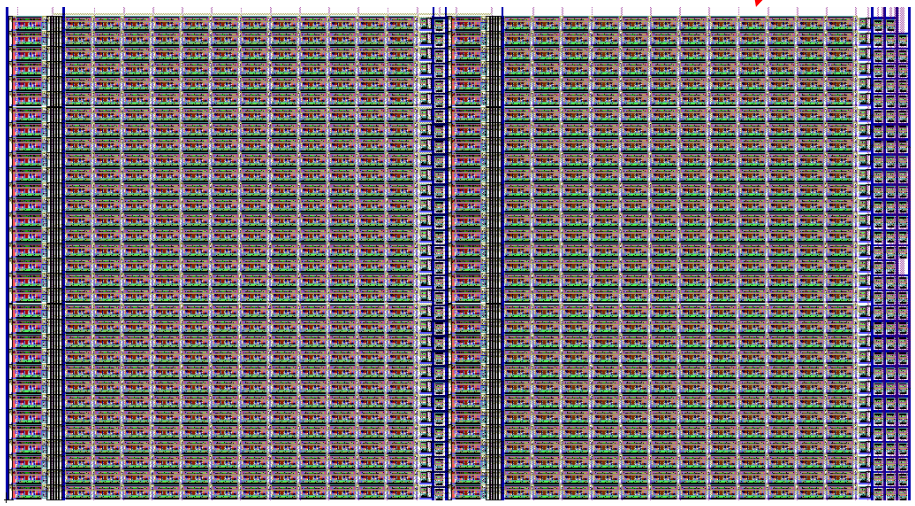
- Sampling: 128 (2x 64 separate transfer lanes

Recording in one set 64, transferring other (“ping-pong”)



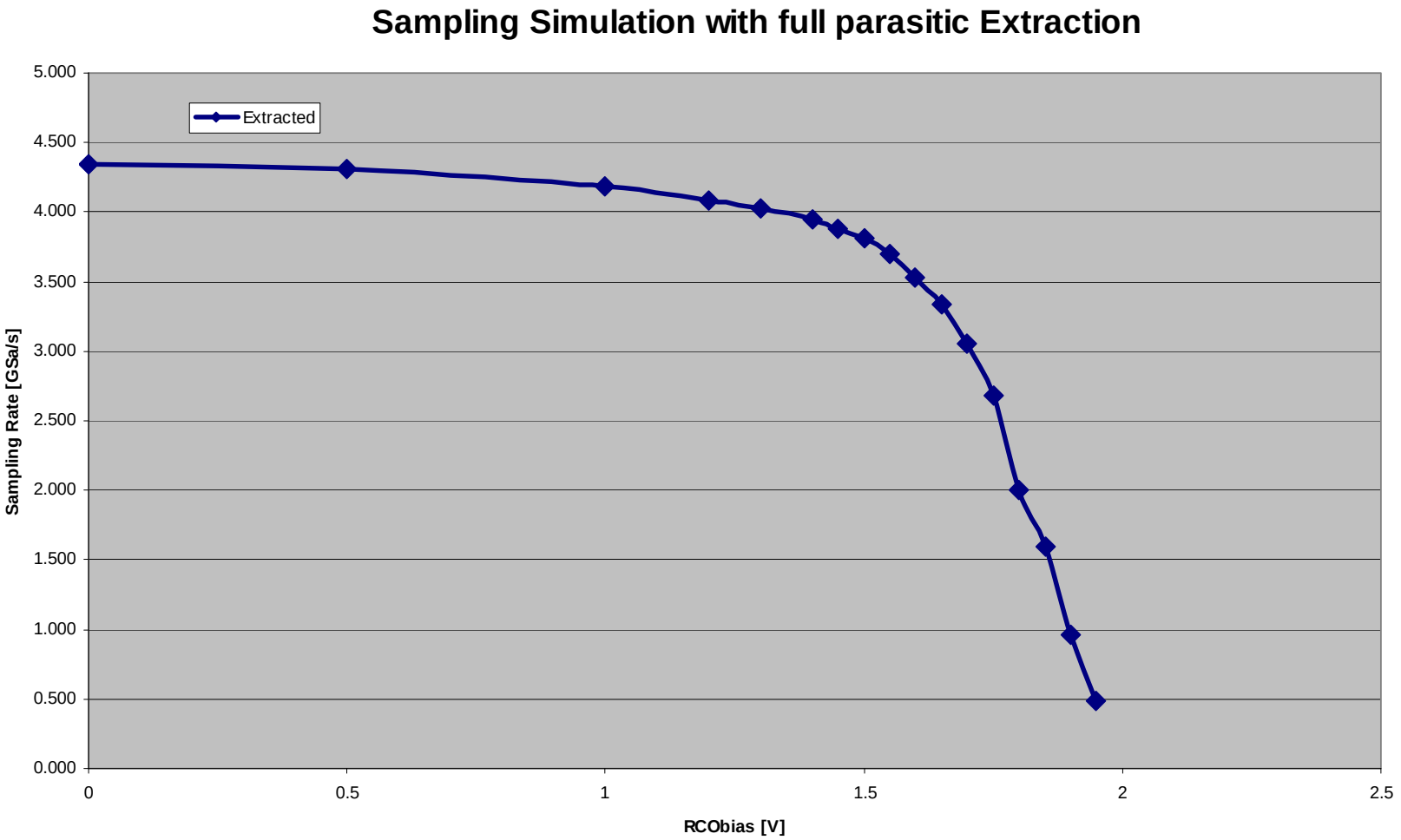


- Storage: 64 x 512 (512 = 8 * 64)



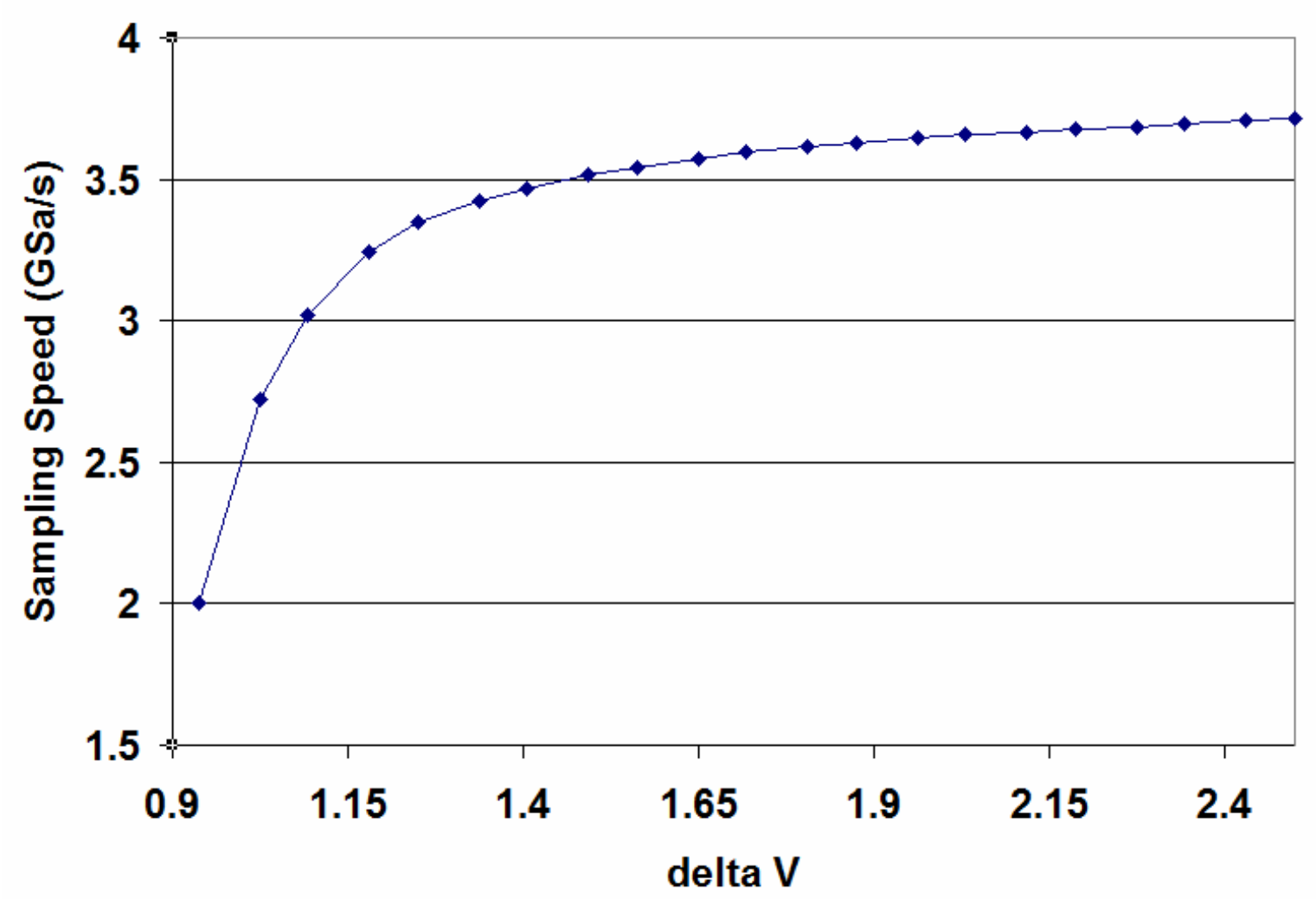
- Wilkinson (32x2): 64 conv/channel

2 stage sampling speed sim



"RCObias" → VadjP1,2 = RCObias; VadjN1,2 = VDD-RCObias

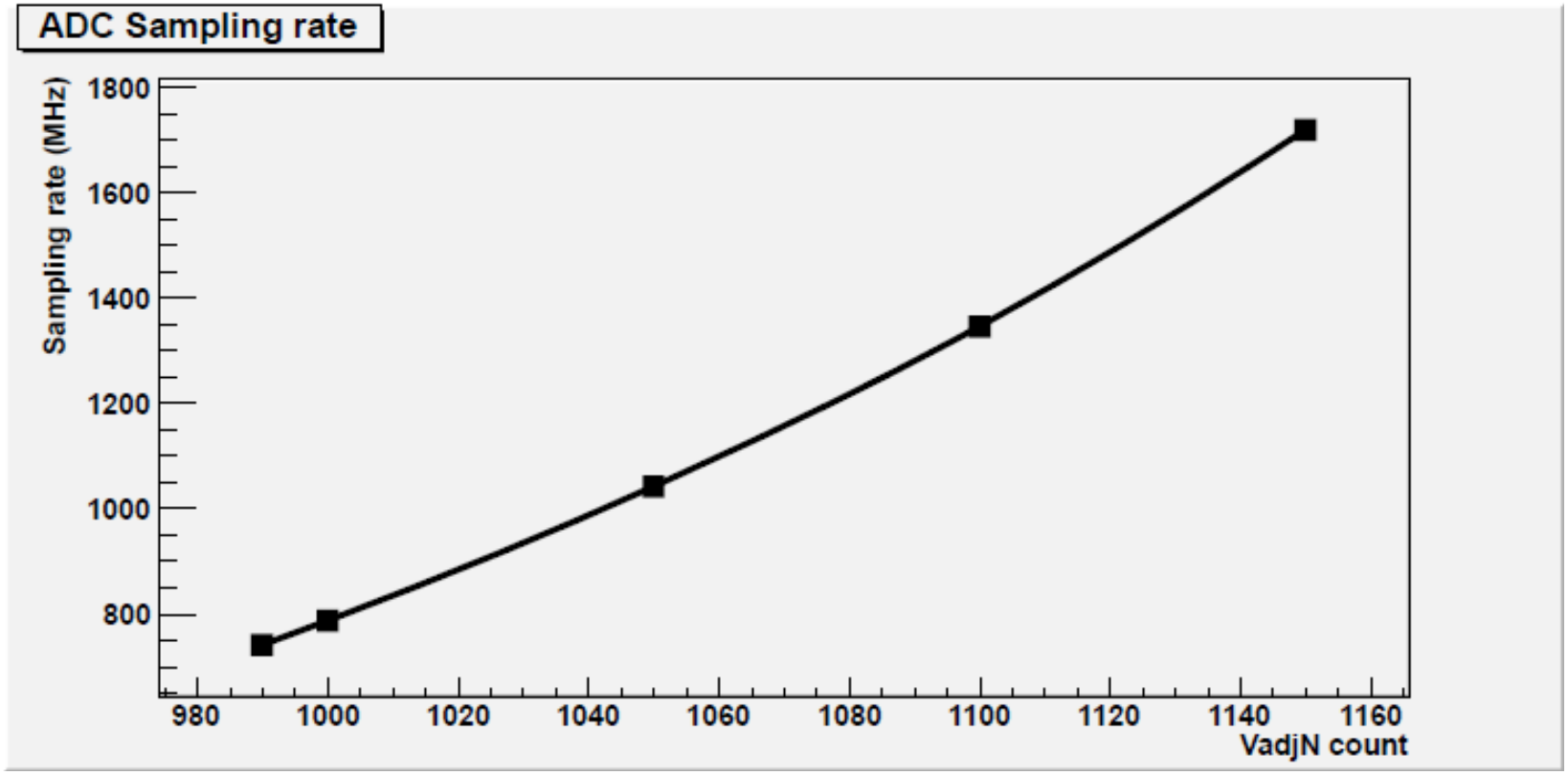
sampling speed measurement



Delta V ➔ RCObias

Matches expectation, but….

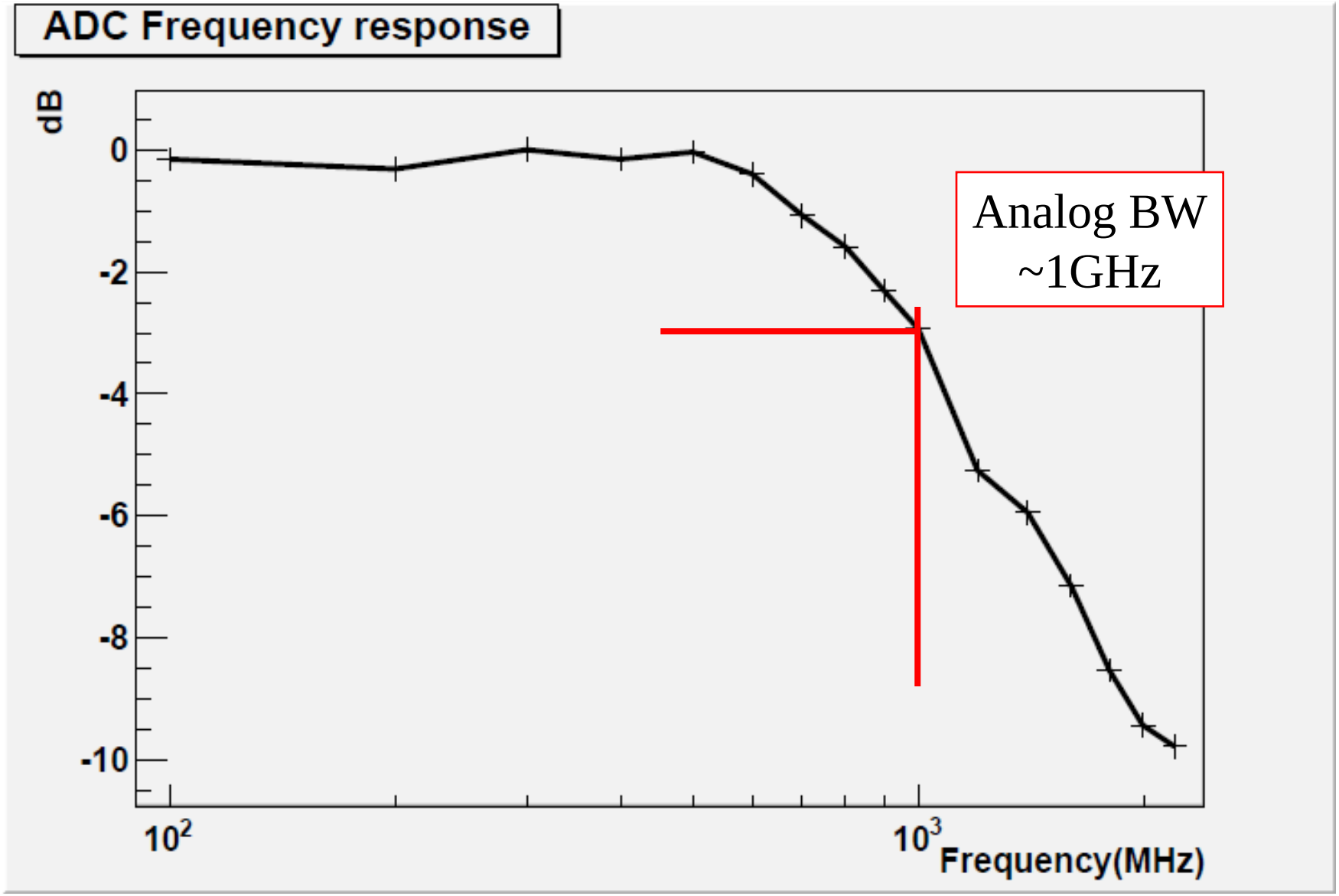
Measurement via RF sine



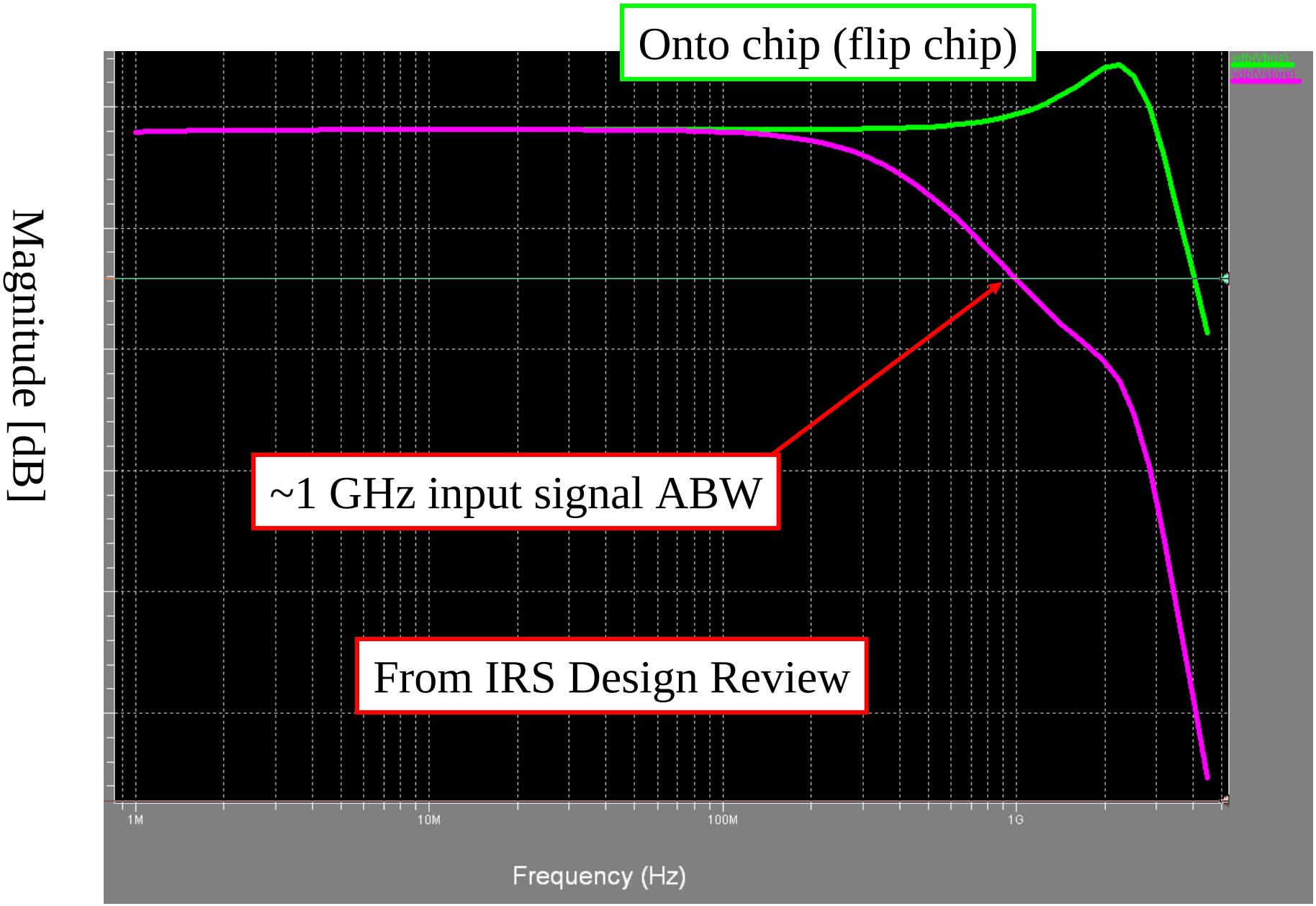
Samples much faster, but at higher sampling rate
Write strobe width problem

Measurements by Chih-Ching

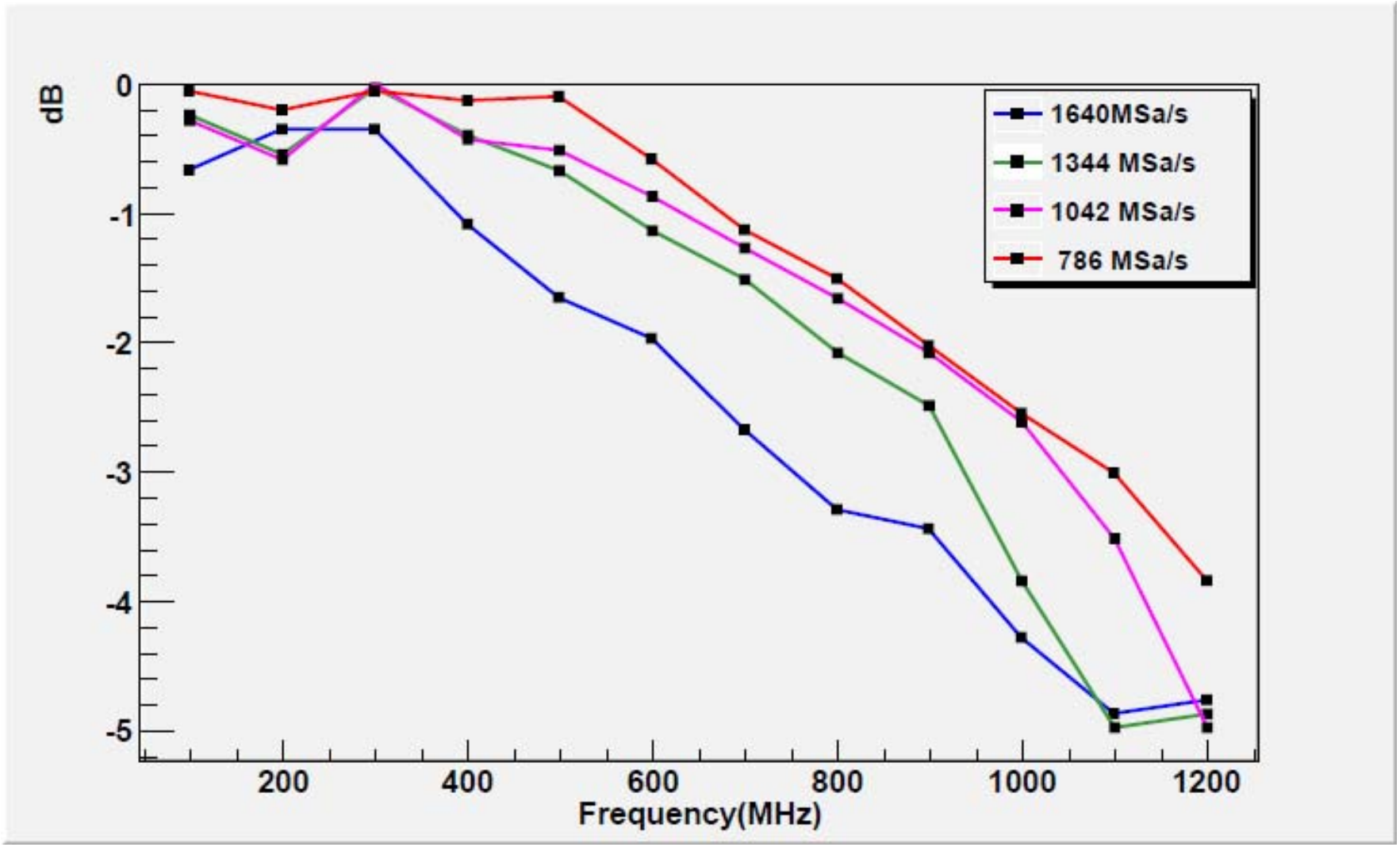
Measurement via RF sine



Input coupling sim (35fF sample)



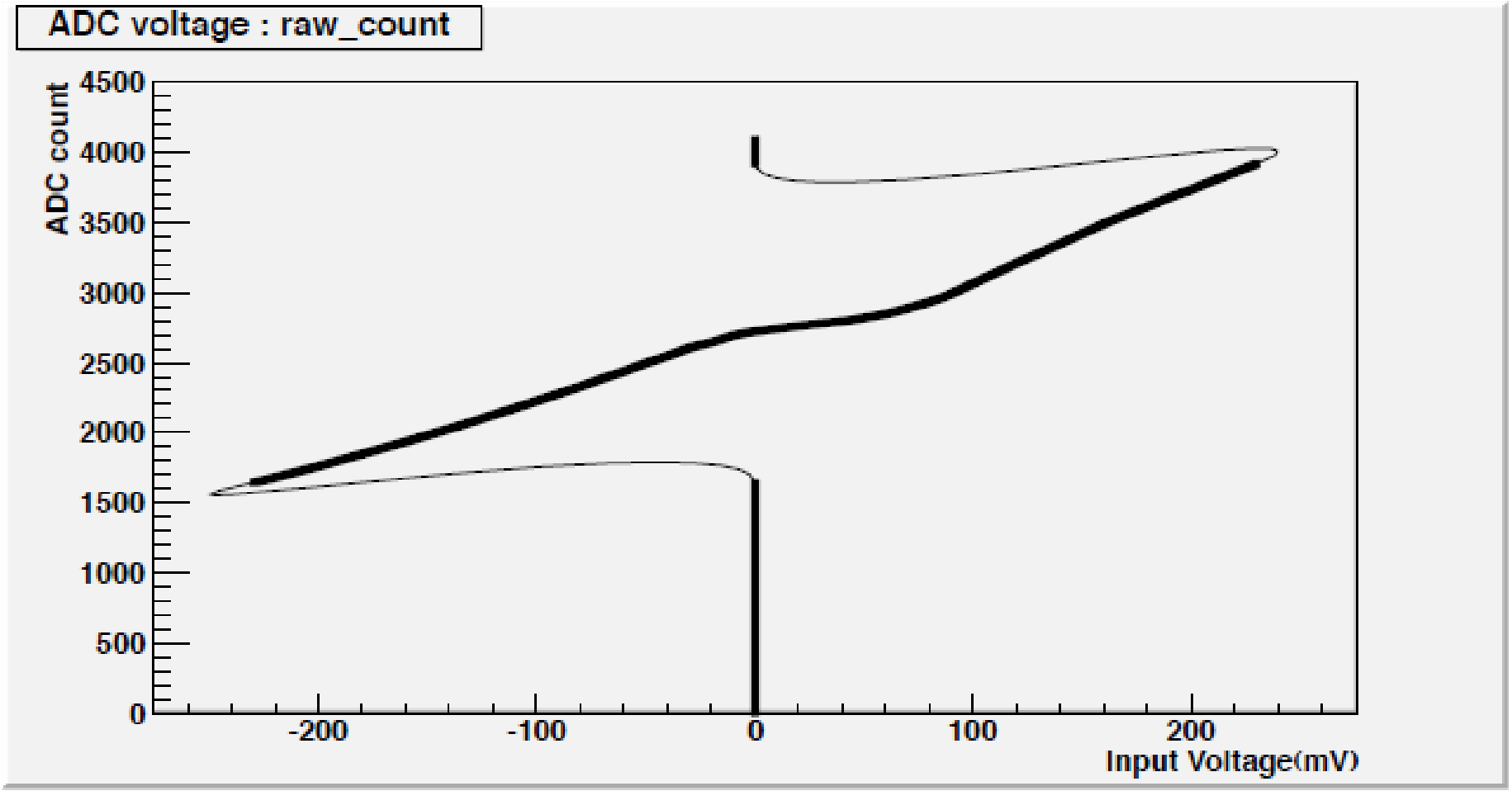
Measurement via RF sine



Samples much faster, but at higher sampling rate

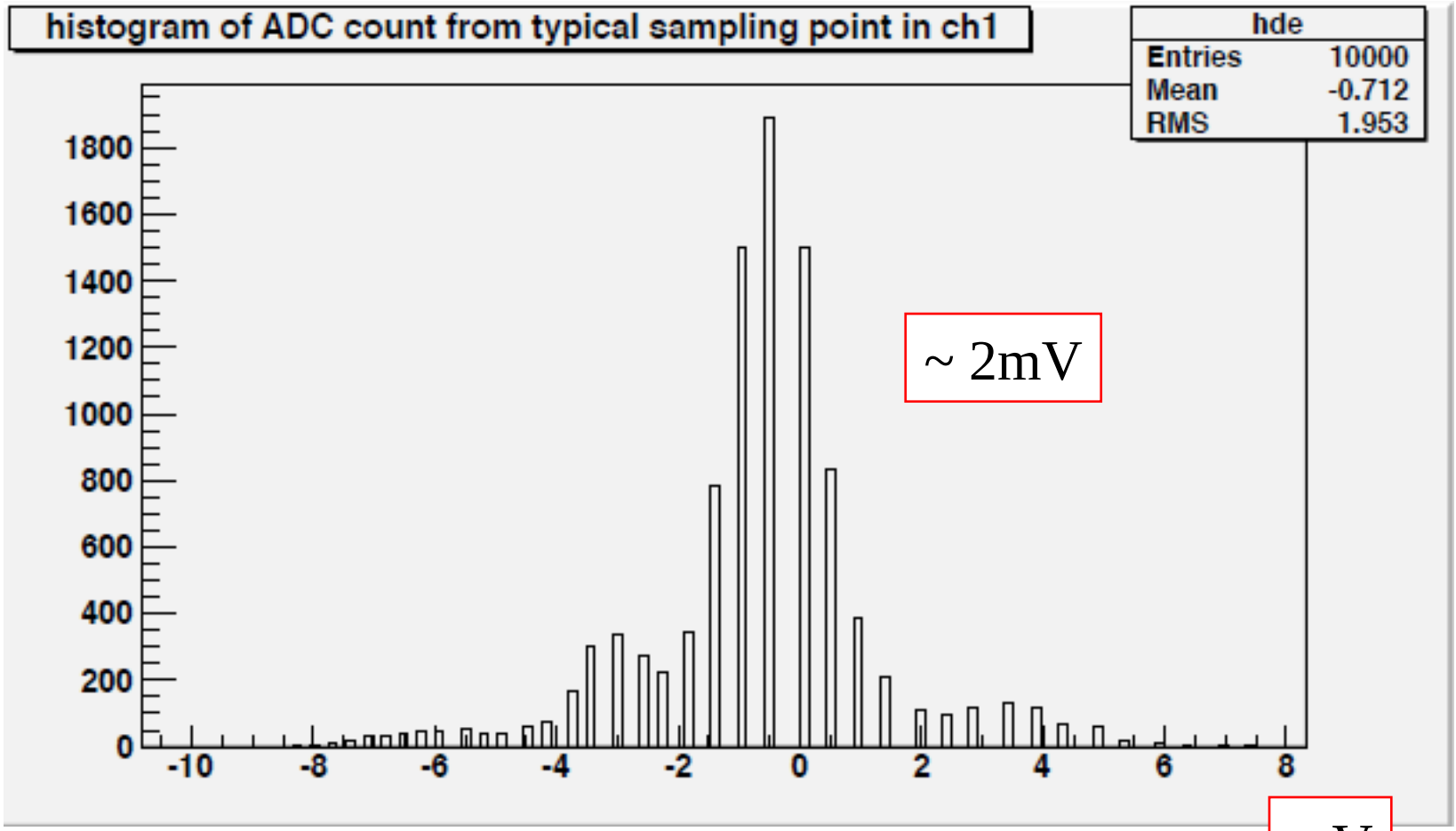
Write strobe width problem (know how to fix)

Linearity Calibration

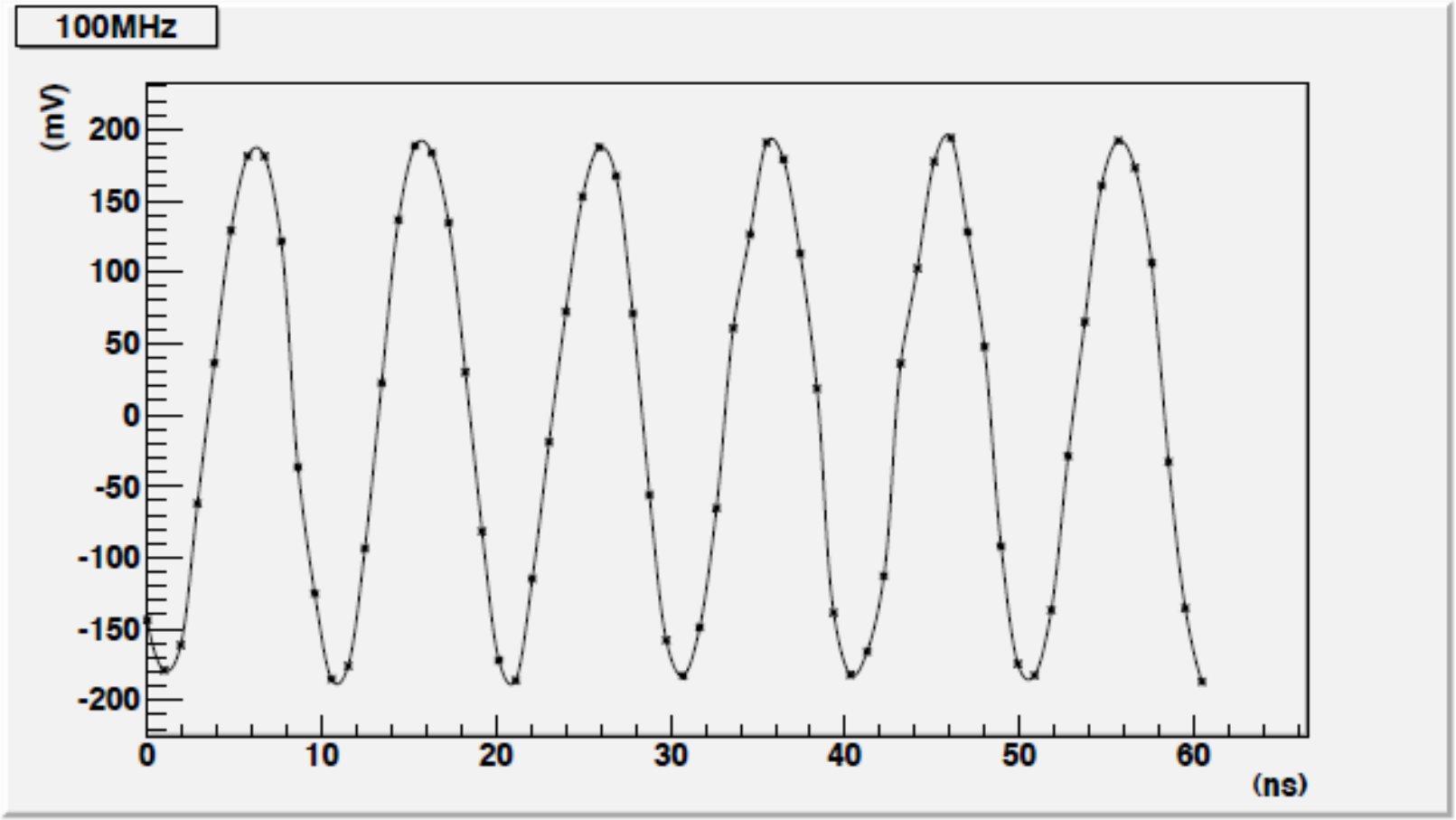


Comparator bias parameters NOT optimized

Noise Measurement



100MHz Signal IRS CH0 readout with cal by signal generator

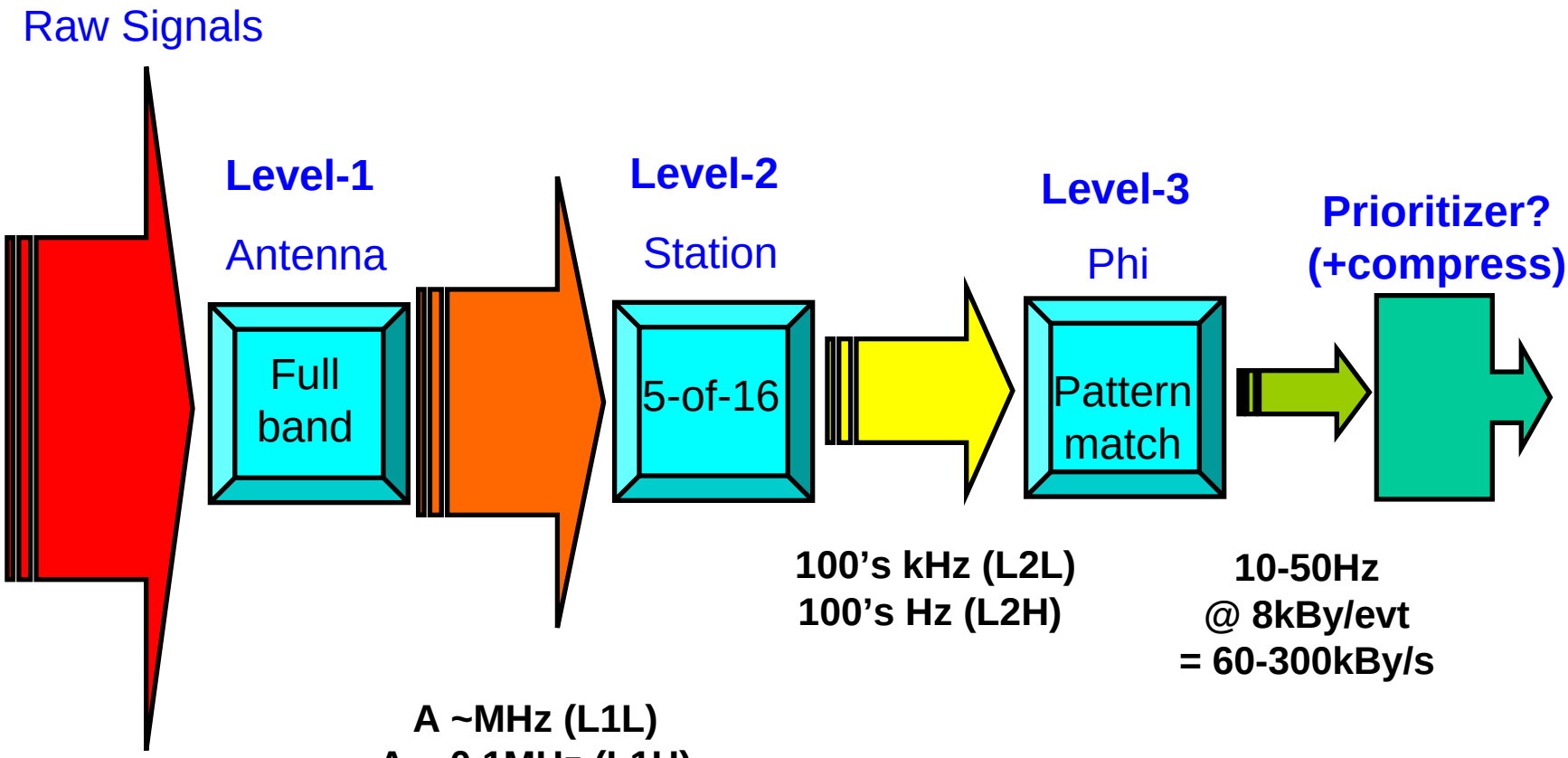


Need dT calibrations

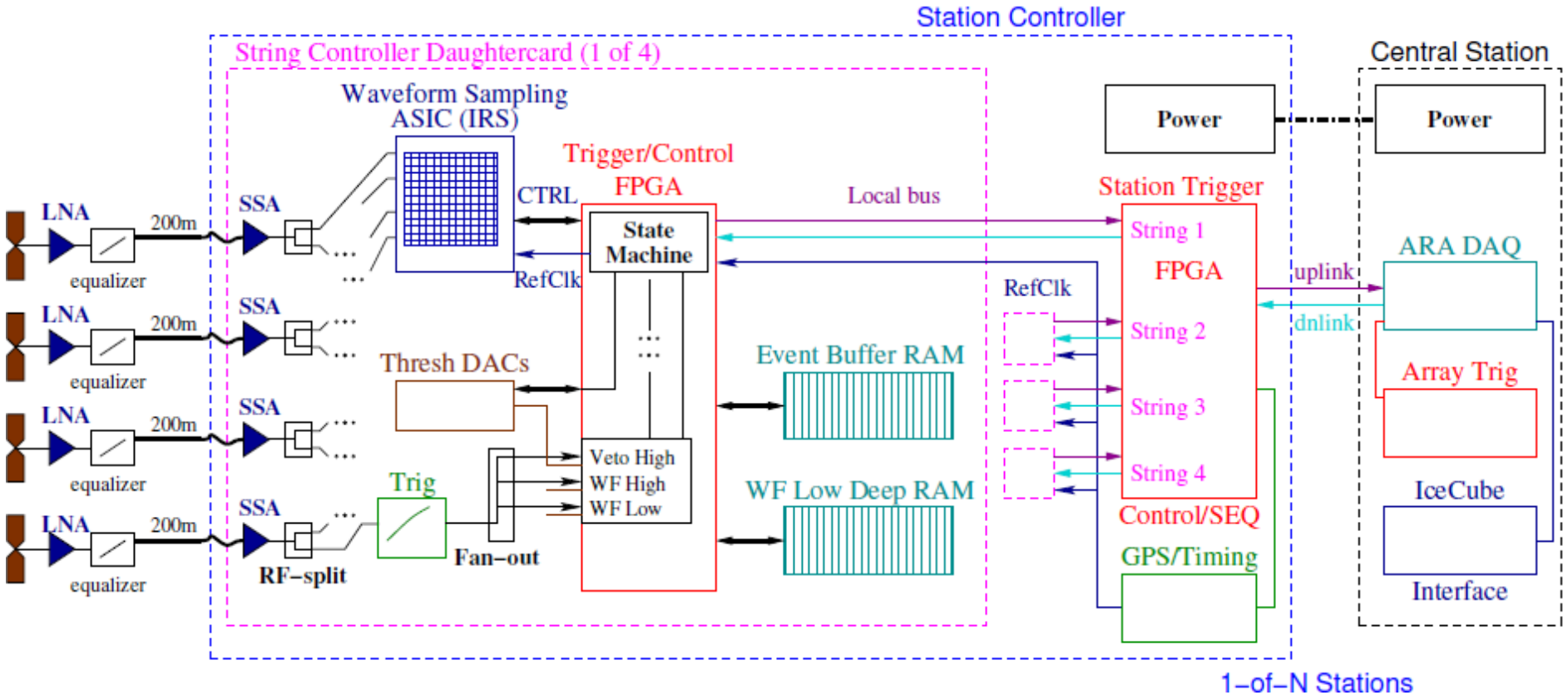
Conversion/readout speed

- Assume 8 channel (5 needed)
  - 5us/ADC cycle (8*64 samples/channel in parallel)
  - Transfer at 50MHz (20ns/sample) to FPGA
  - 1 conversion cycle ~ 5us (ADC) + 10us (transfer)
  - 256ns window (512 samples @ 2GSa/s) = 8 conv cycles
  - Total ~ 120us [CF: 1kHz trigger]
  - Deadtimeless: 256ns (512 samples) of 16us (32k samples) held – sampling continues on others

Station Data Reduction (self-trigger)



ARA Readout Electronics – system discussion



- Uplink bandwidth (~1Mbit/s [wireless])
  - Multi-tier trigger
  - Deeper sampling allows for “array” trigger (subthreshold)

IRS → AARDVARC Specifications ?

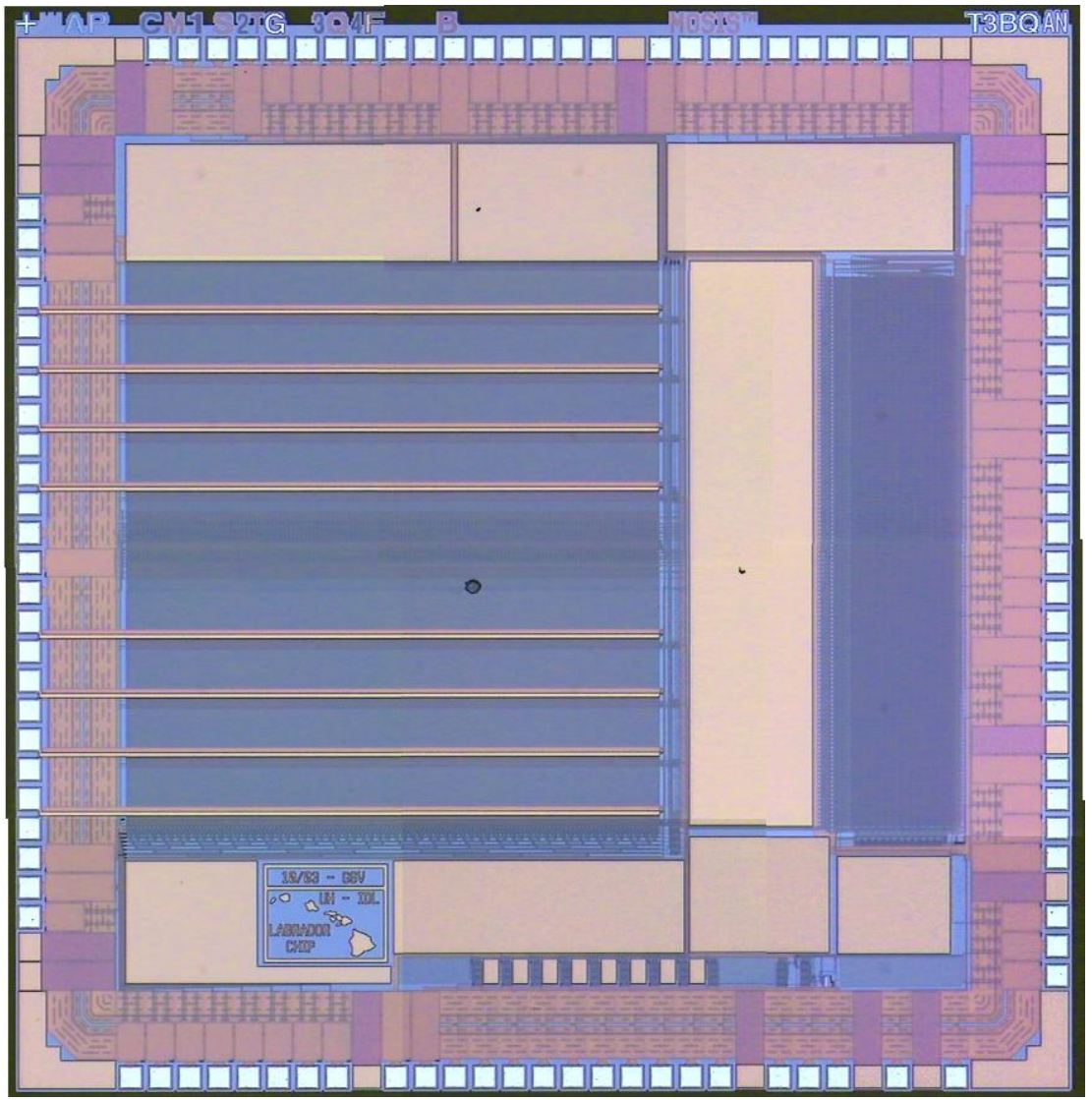
262144	samples/chan (130us trig latency)
1	channel/ASIC
--	Trigger channels
~9	bits resolution (12-bits logging)
64	samples convert window (32ns)
2	GSa/s
1	word (RAM) chan, sample readout
<10	us to read all window samples
10k	Hz sustained readout (multibuffer)

- Avoids issue of channel-channel cross-talk
  - Slave sampling all ASICs together
  - Plenty depth for multi-hit buffering

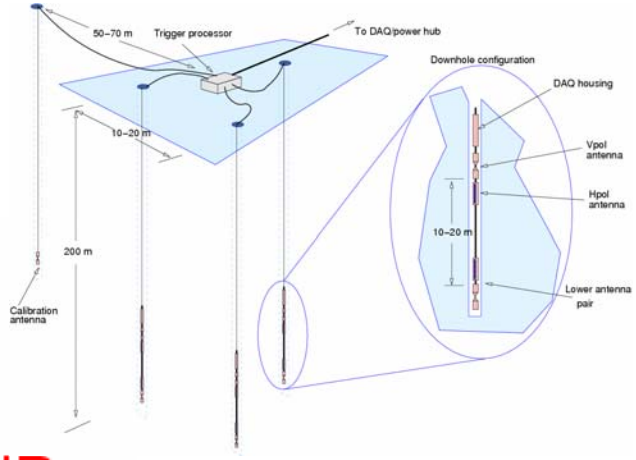
Summary

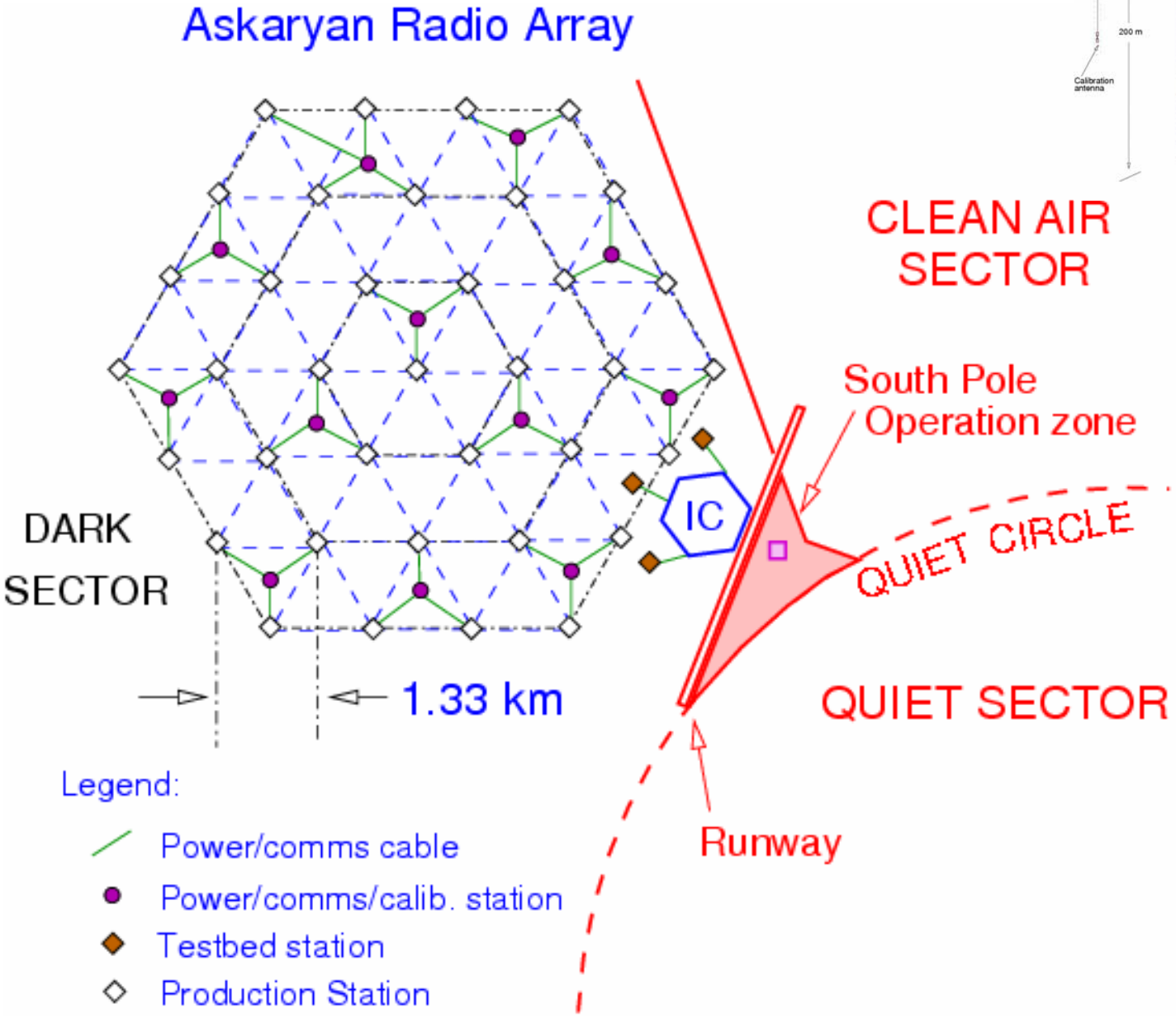
- Station design evolving
  - Build sample station for firmware/cal testbed development
  - Initially test with thermals (servo-loop software/firmware)
- Key technology decisions
  - Tunnel diode versus RF power mon
  - IRS → AARDVARC
  - Data and fast trigger links
- Proposed architecture
  - Rather flexible
  - Optimize as we go

Back-up slides

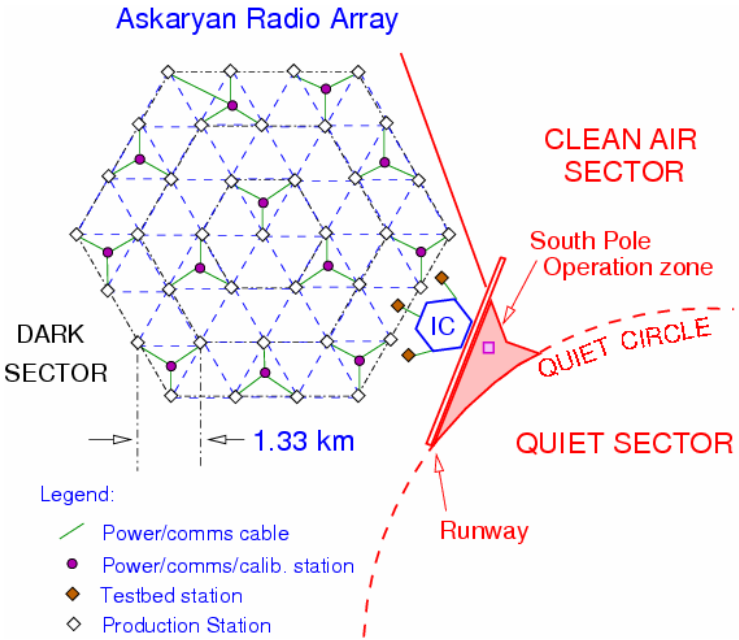


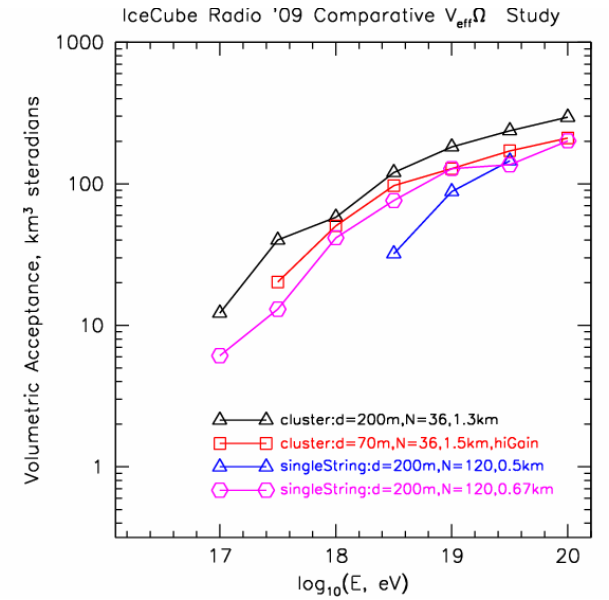
Askaryan Radio Array (ARA)

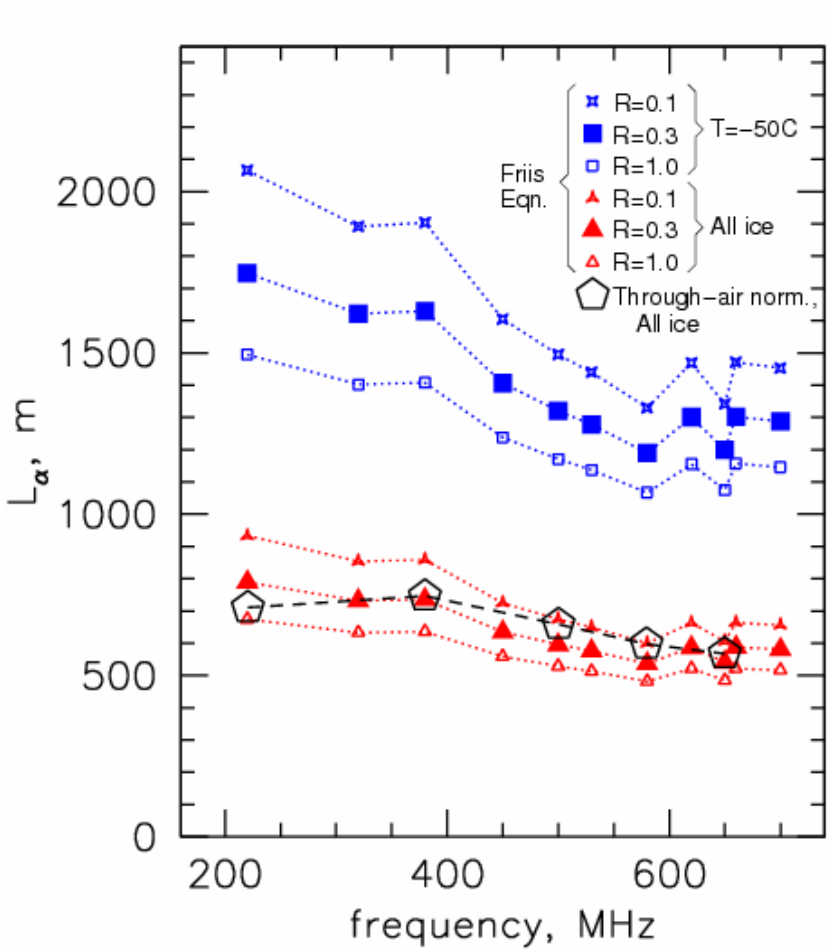




Askaryan Radio Array





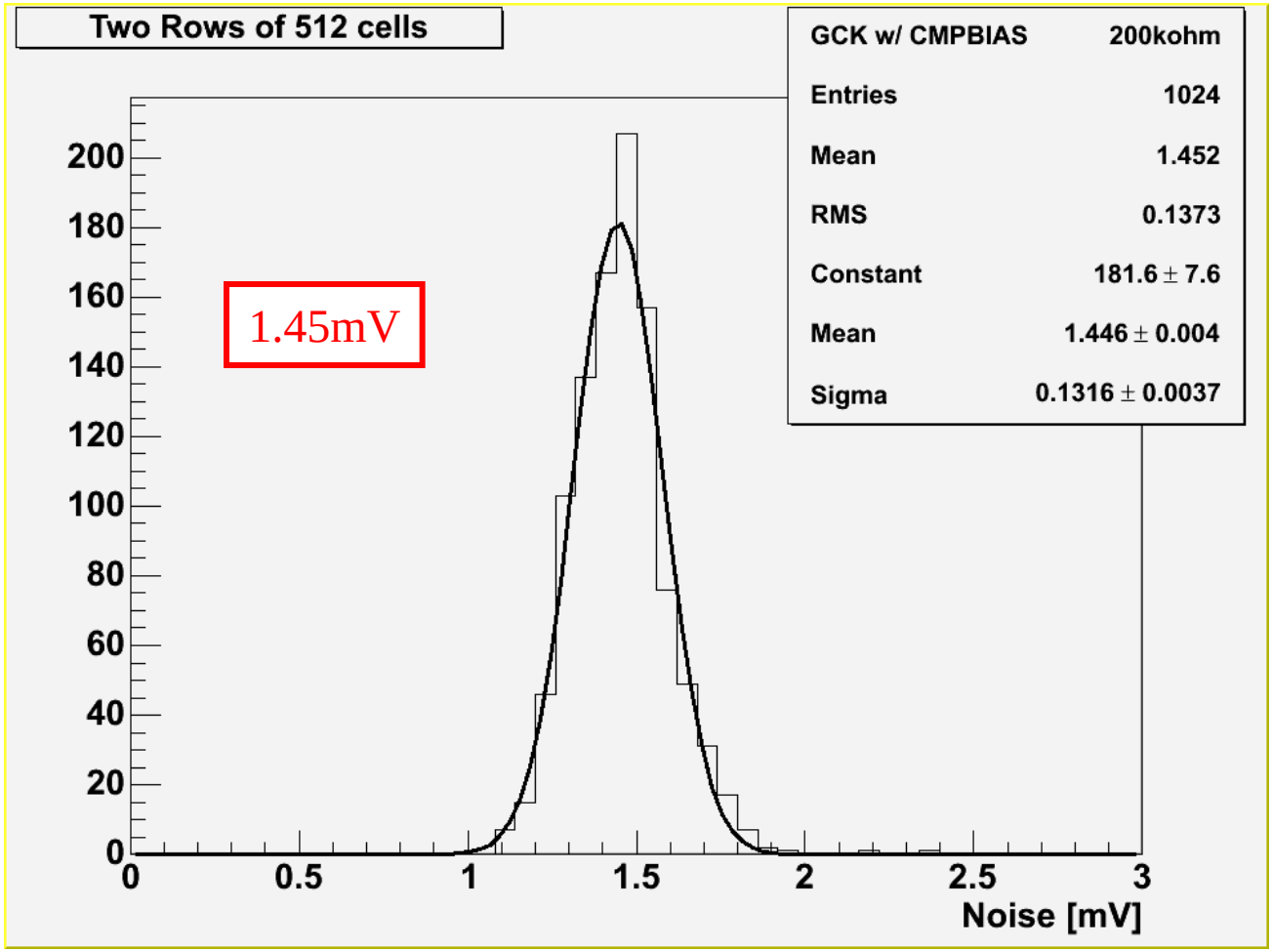


Buffered LABRADOR (BLAB1) ASIC

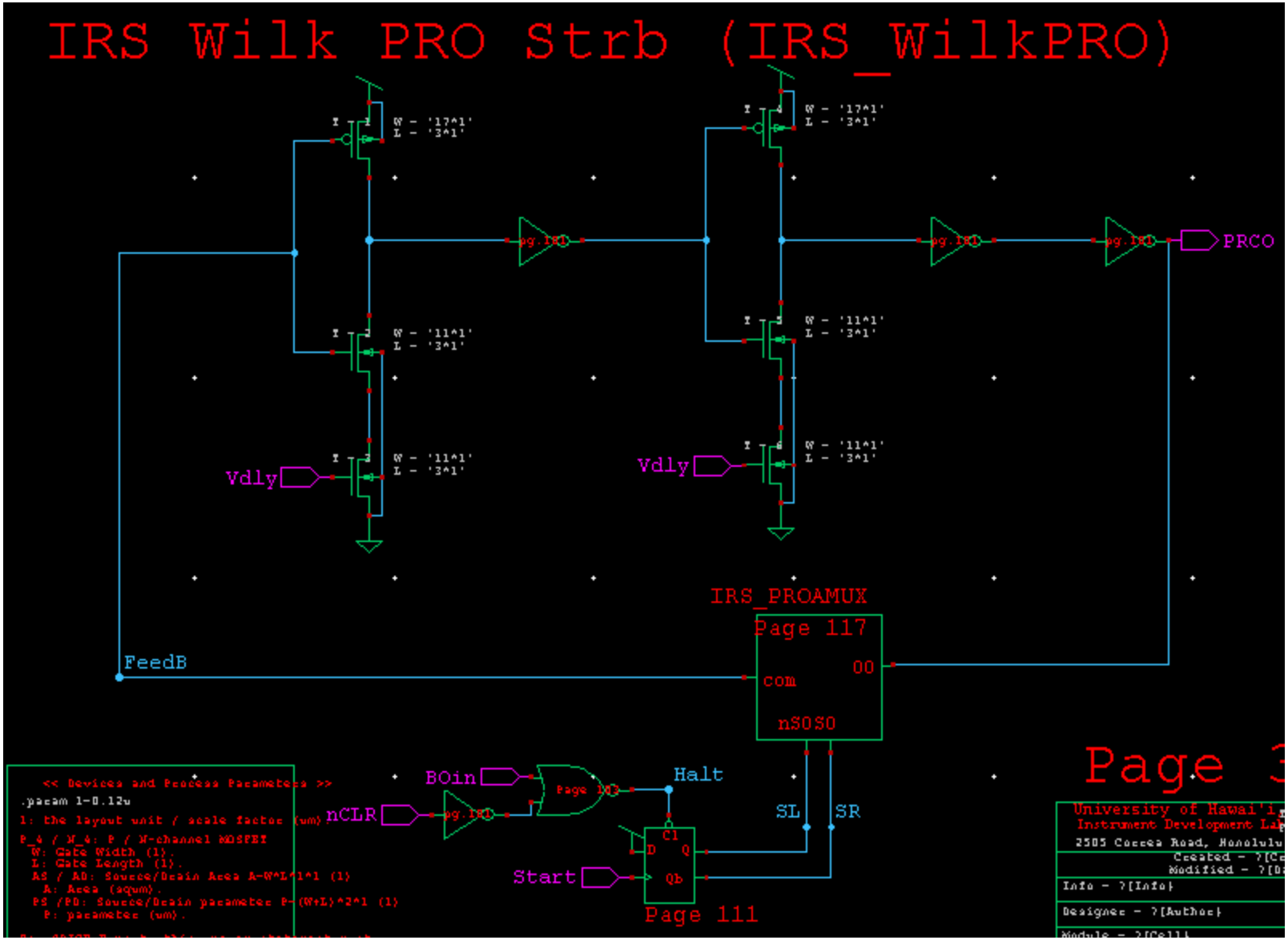
- 10 real bits of dynamic range, single-shot

Measured Noise

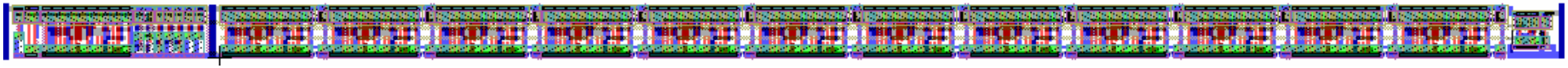
1.6V dynamic range

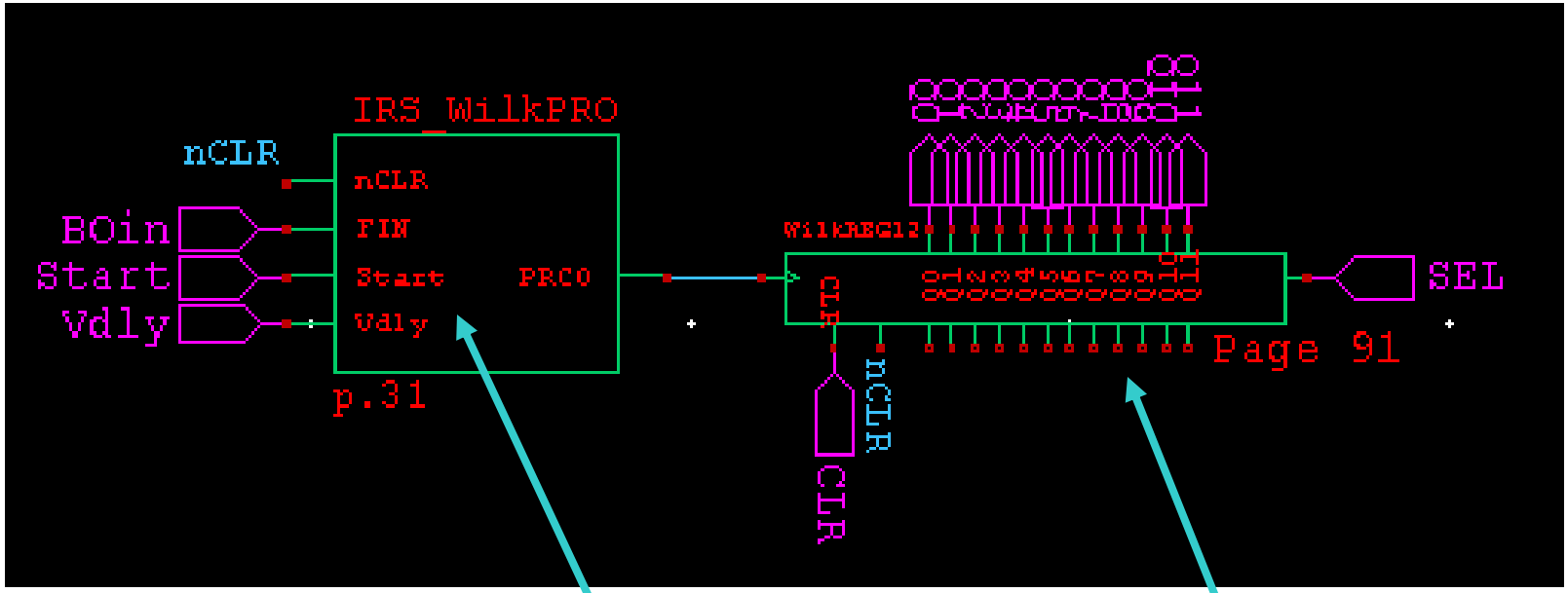


Wilkinson Clock Generation



Wilkinson Recording

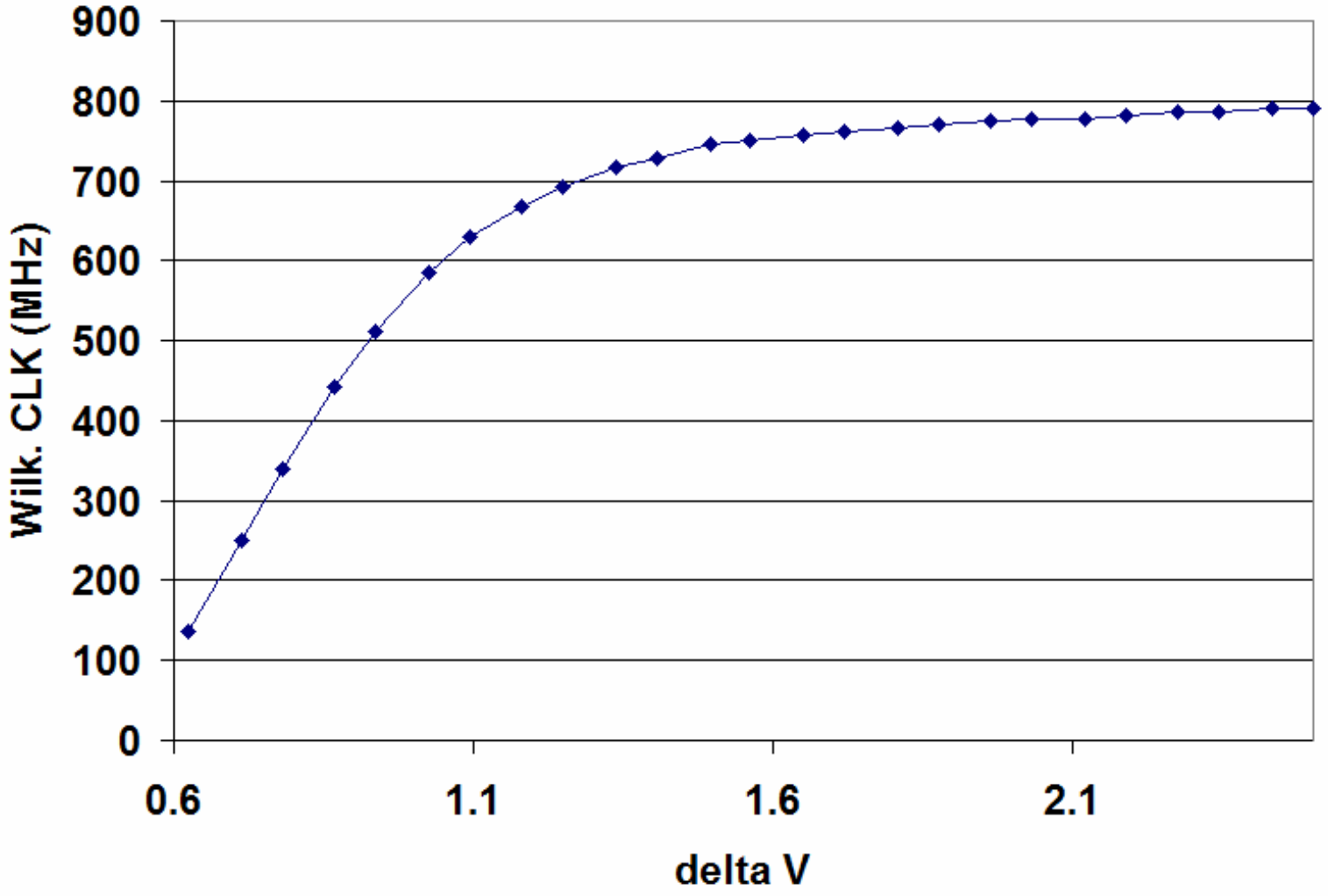




Start = start 0.5-8GHz Clock

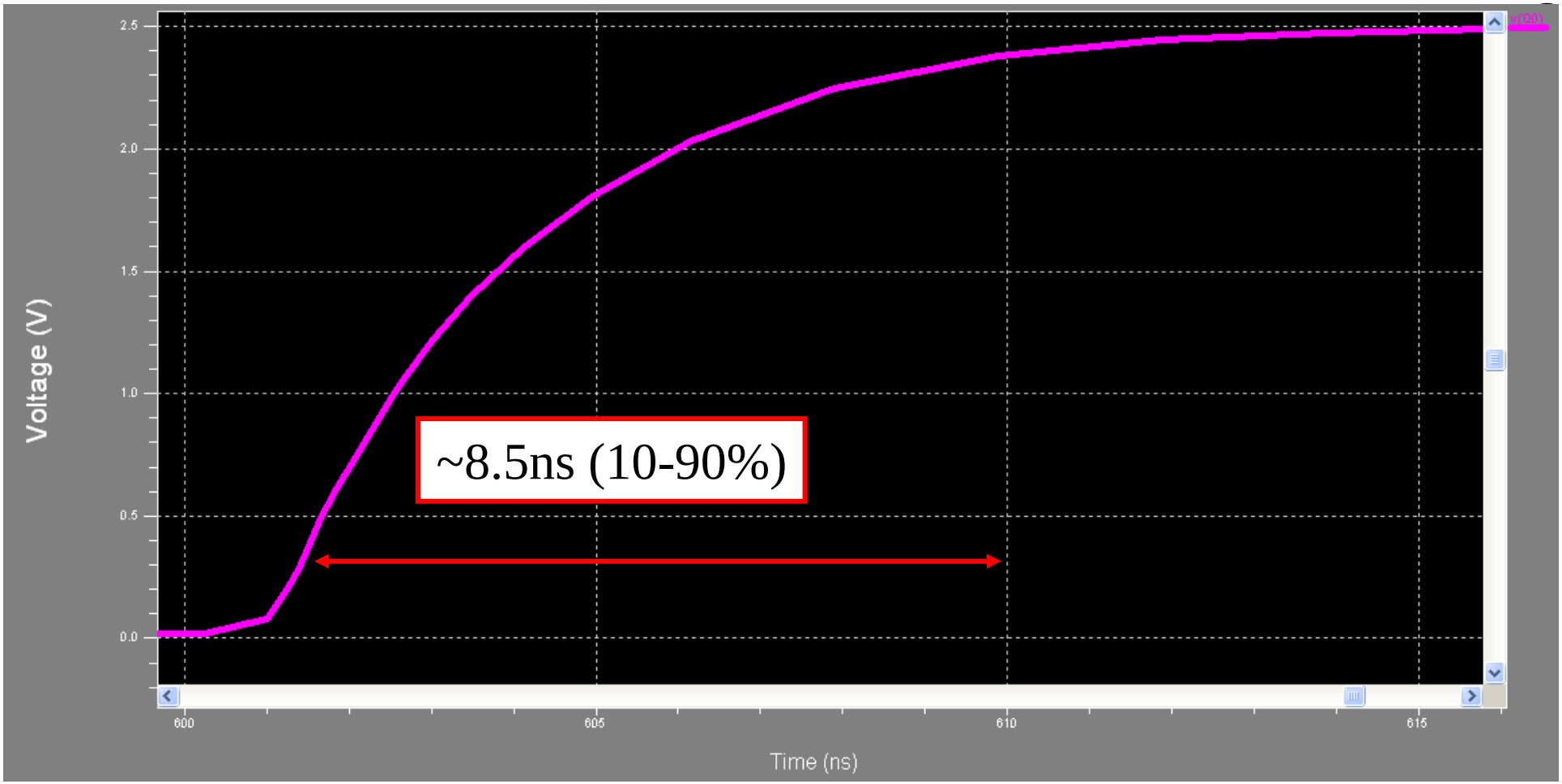
Ripple counter (run as fast as can)

Wilkinson speed measurement



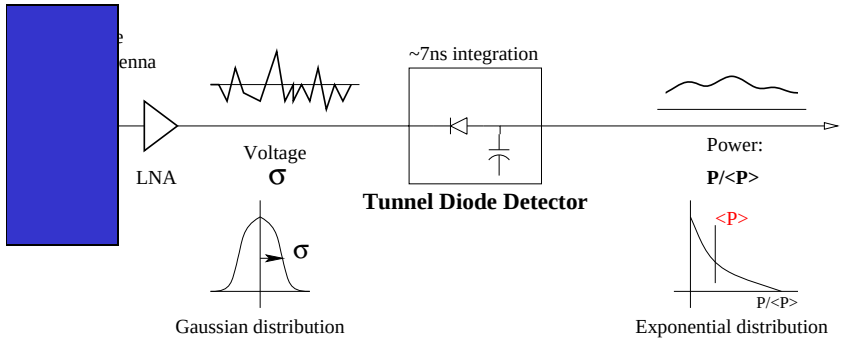
0.7 GHz ➔ 1.4us conversion to 10 bits

Output Bus Settling Time

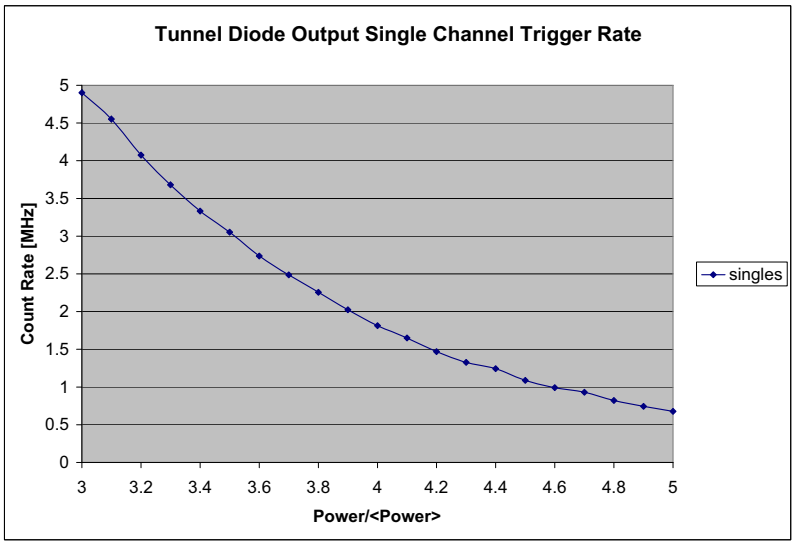


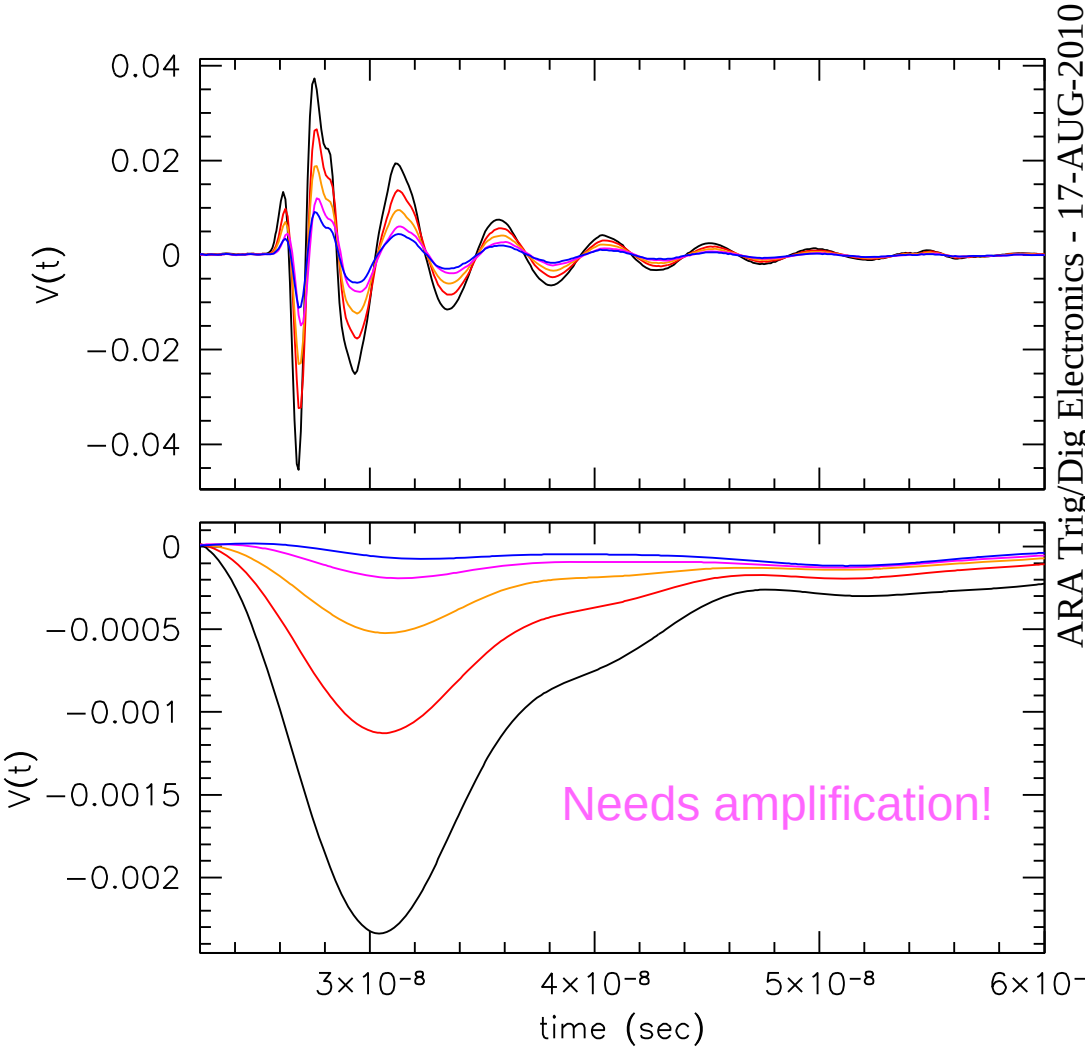
~100MHz bus operation should be possible

Diode detector Response

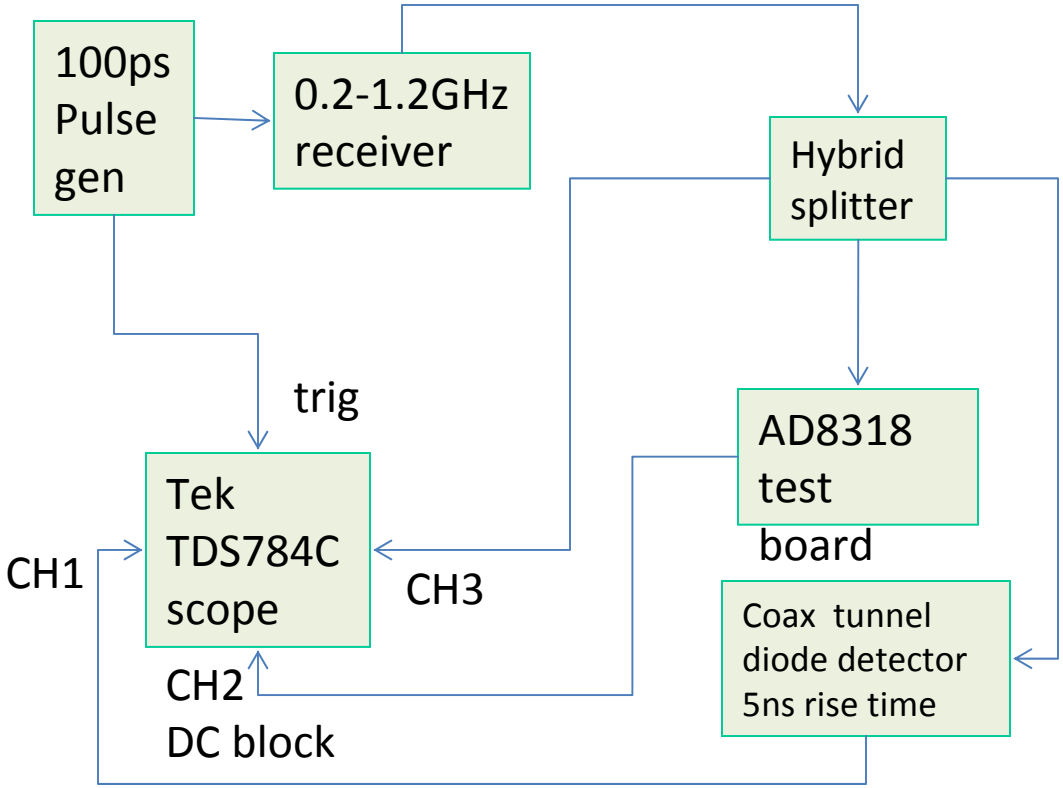


2.3σ ~= 3.9 P/<P>



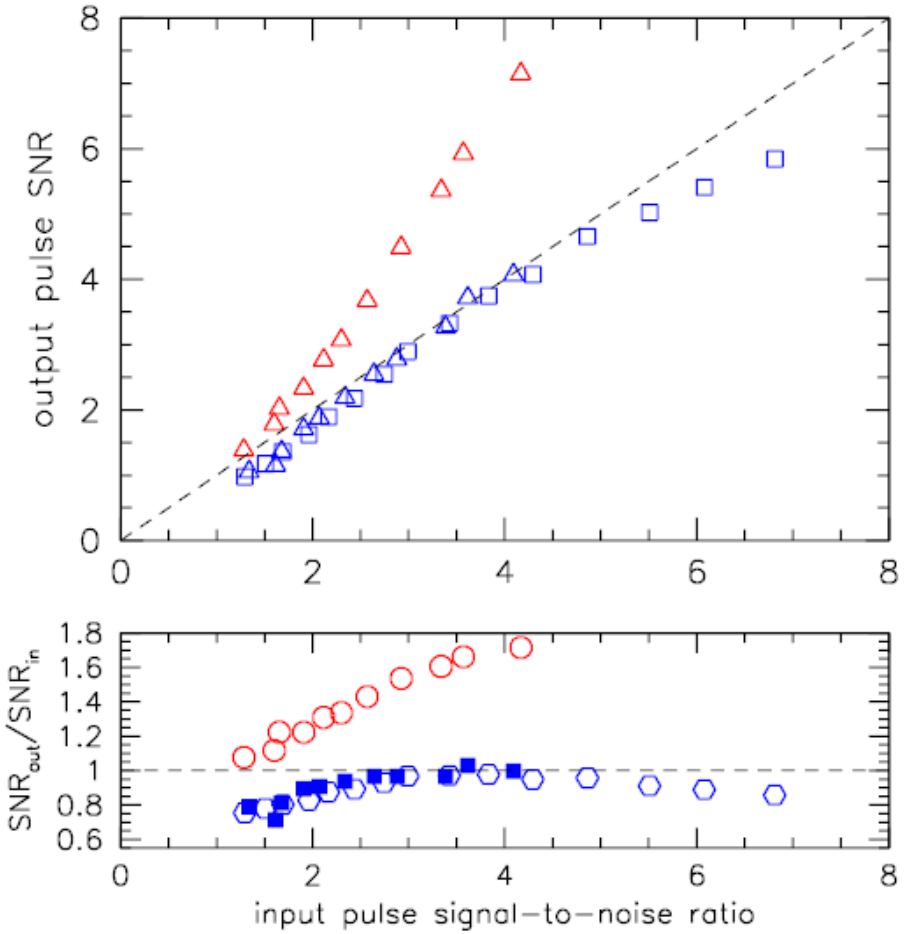


Log-amp, tunnel diode test



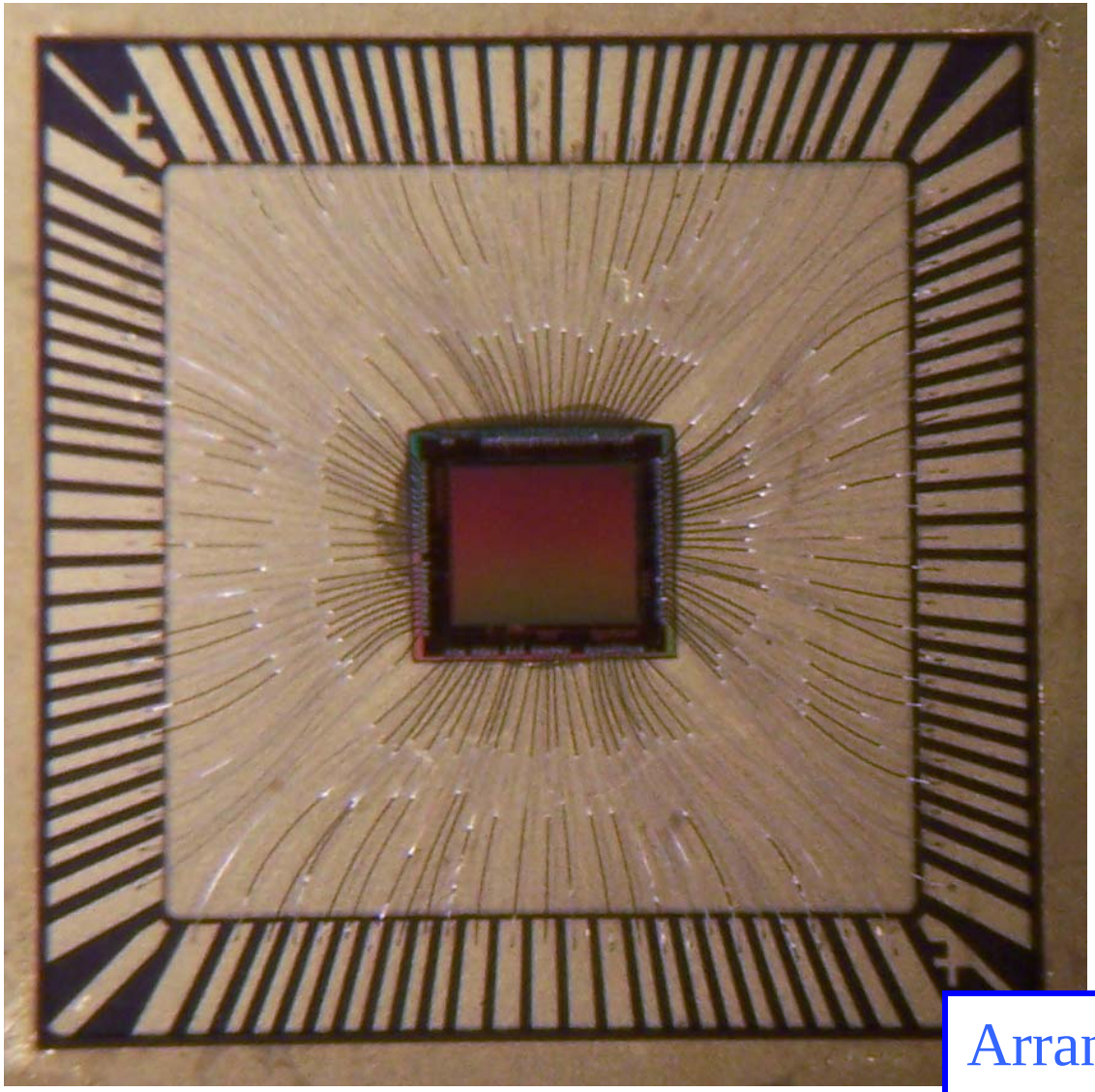
- Can fast log-amps give same SNR as TD trigger?
- Log-amp: V proportional to power
- Uses multi-stage switching to get wide “linear” dynamic range, good stability
- Tunnel-diode: square-law detector with long history in radio astronomomy & physics
  - But they are fussy to use!

Log-amp vs. tunnel diode SNR test



- Look at Vpeak to Vrms ratio for each device
- Log-amp:
  - saturation evident
  - Loss of SNR fidelity below SNR~3
- TD: square-law behavior evident
- Conclusions: log-amps may be problematic
- We really need a true trigger efficiency test

Design Basis: Buffered LABRADOR (BLAB1) ASIC

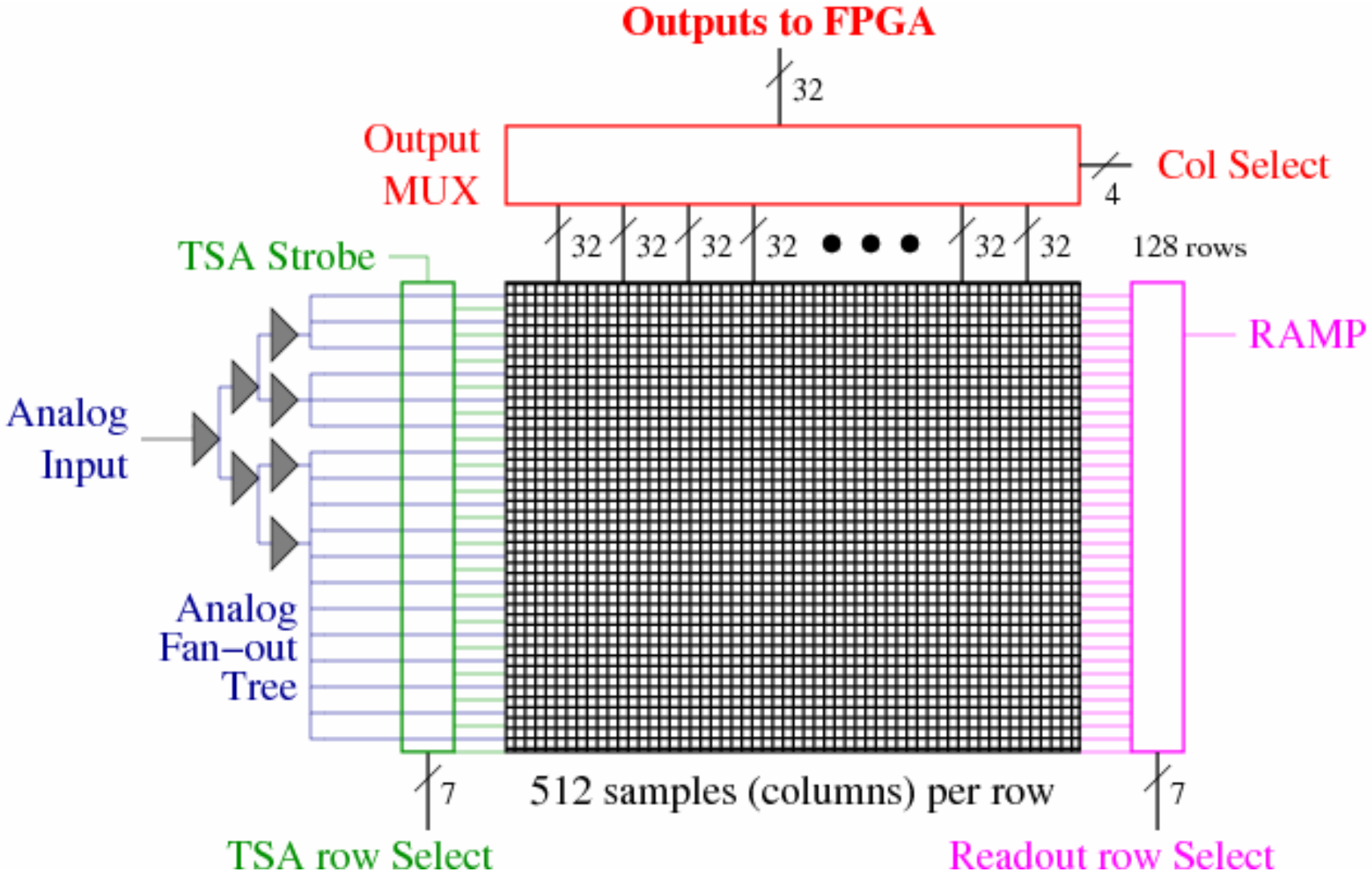


3mm x 2.8mm, TSMC 0.25um

- Single channel
- 64k samples deep, same SCA technique as LAB, no ripple pointer
- Multi-MSa/s to Multi-GSa/s
- 12-64us to form Global trigger

Arranged as 128 x 512 samples
Simultaneous Write/Read

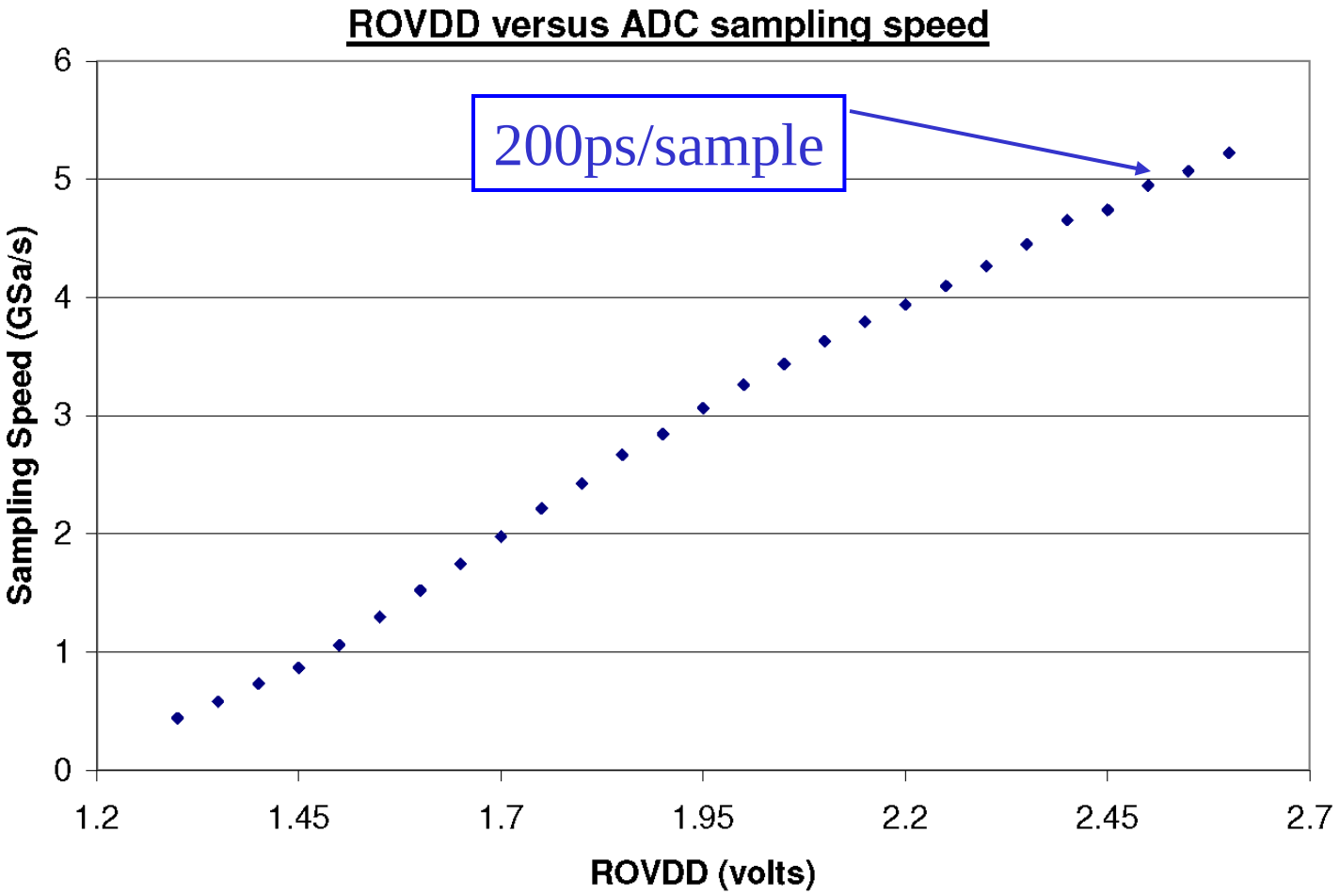
BLAB1 Architecture



FPGA-based TDC: 10-bits in 1us (300ps resolution)

BLAB1 Sampling Speed

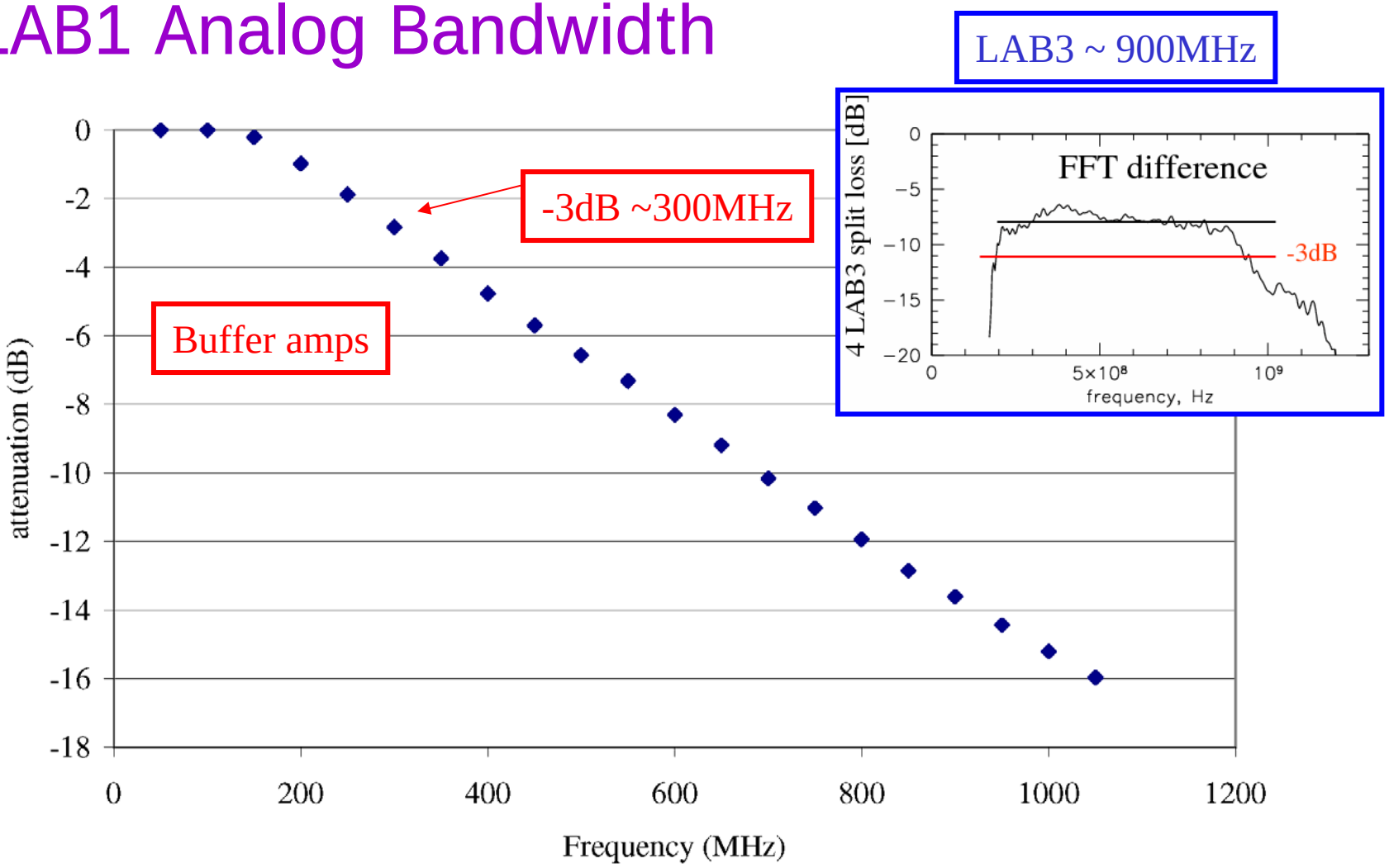
Can store 13us at 5GSa/s (before wrapping around)



Single sample:
200/SQRT(12)
~ 58ps

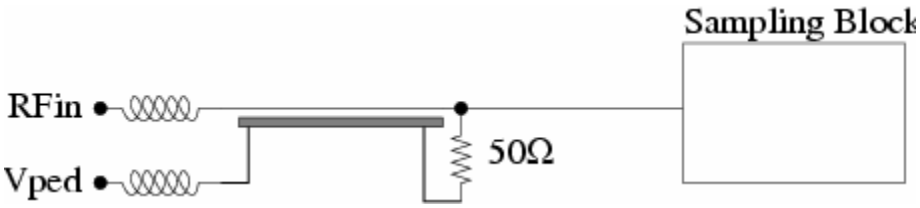
In practice, treat each row of 512 samples as independent

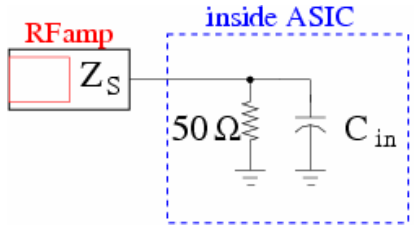
BLAB1 Analog Bandwidth

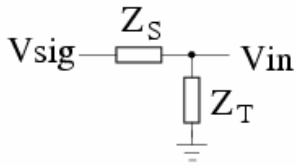


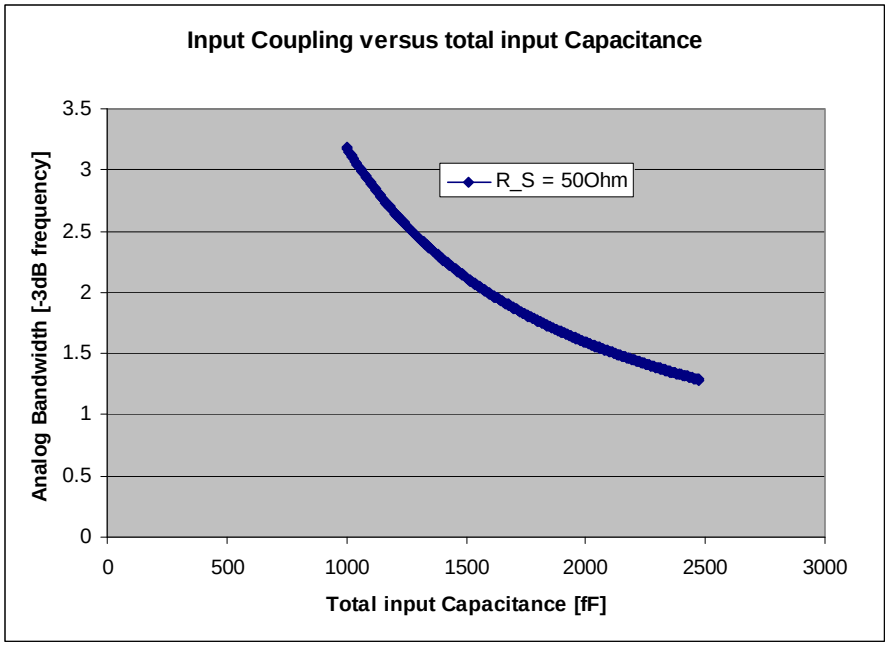
- A few fixes (lower power, higher BW)
- Multi-channel desired for BLAB2

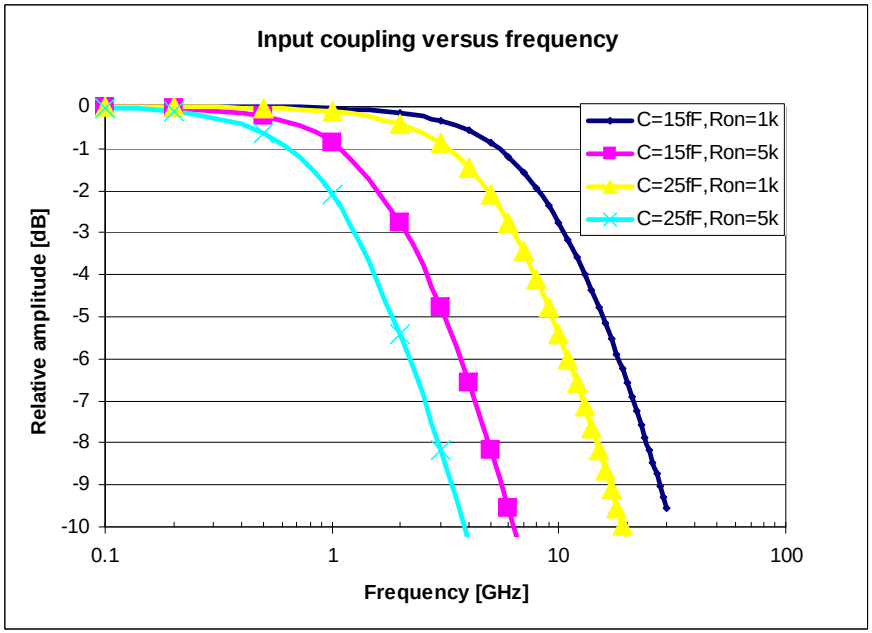
IRS Input Coupling





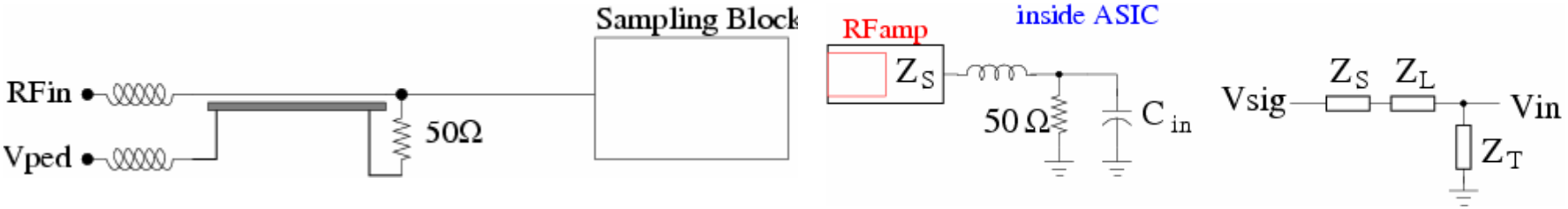


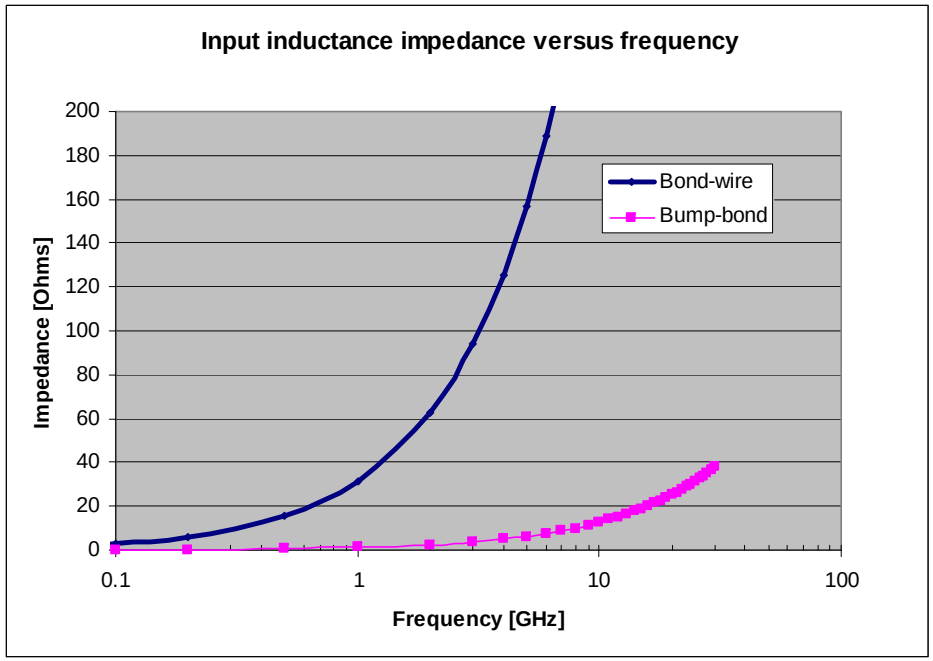


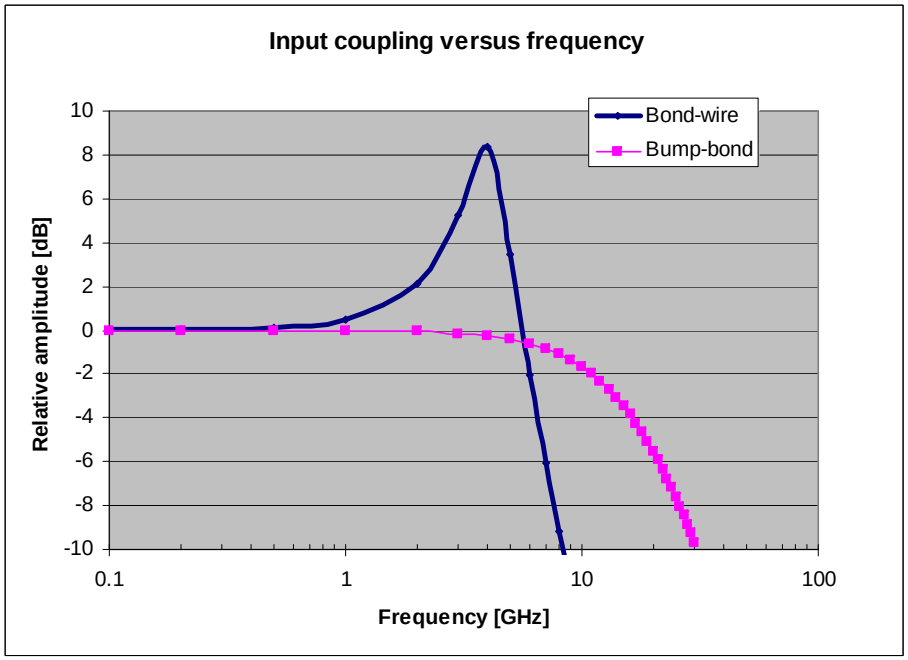


- Input bandwidth depends on 2x terms
  - $f3dB[input] = [2*\pi*Z*C_{tot}]^{-1}$
  - $f3dB[storage] = [2*\pi*R_{on}*C_{store}]^{-1}$

IRS Input Coupling

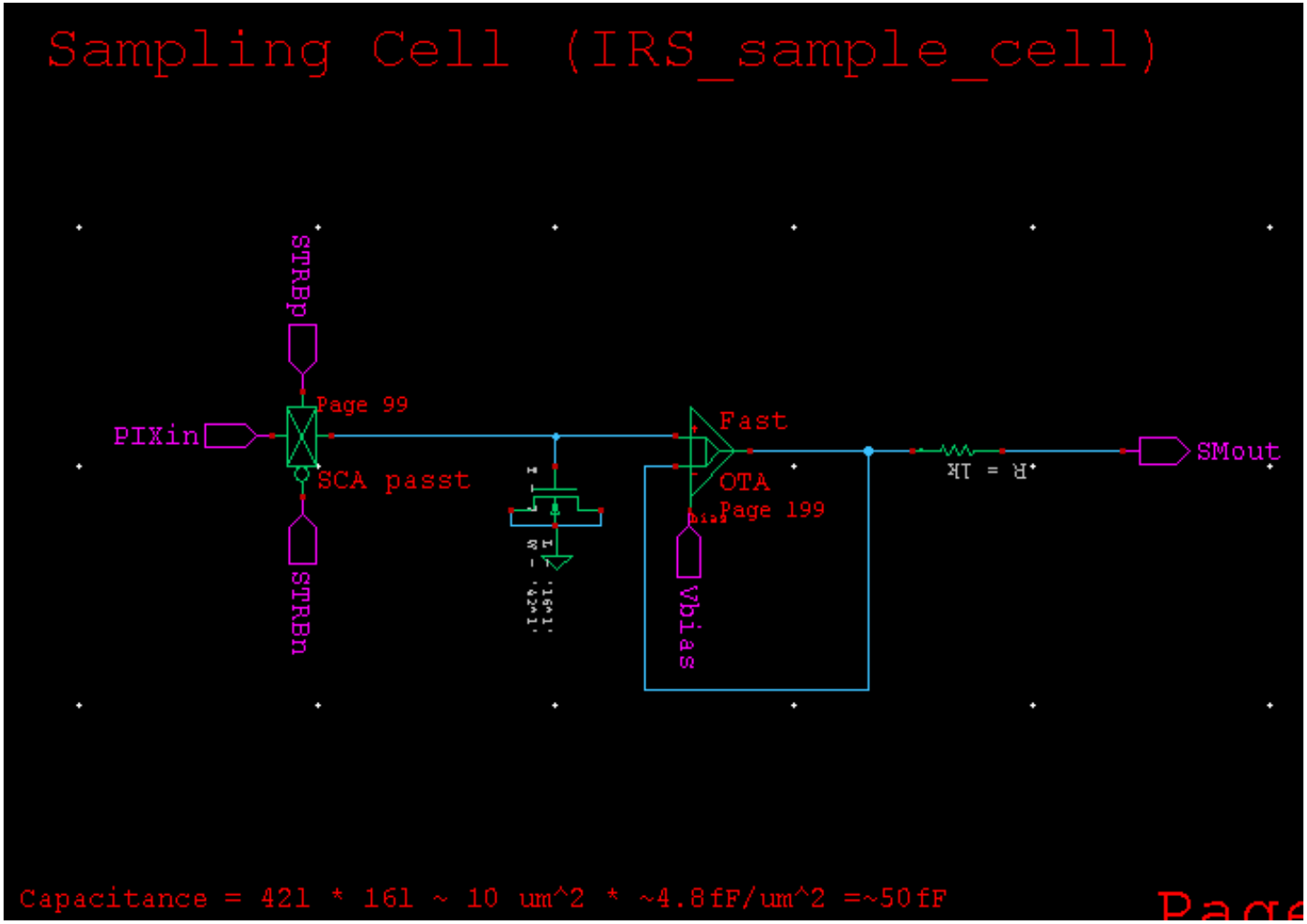


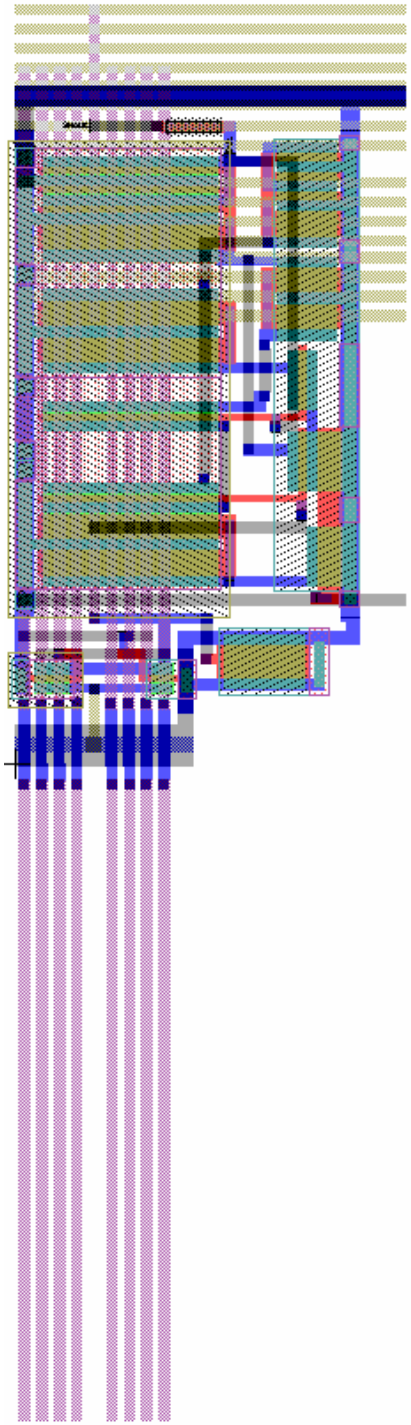




- Role of inductance

Sample Cell

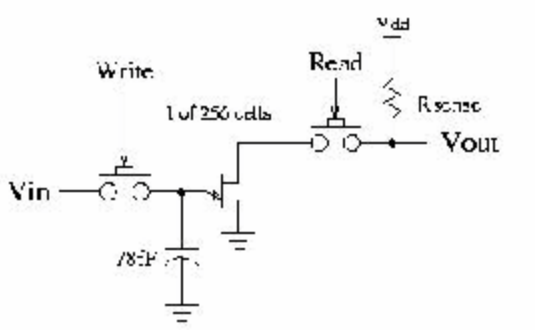




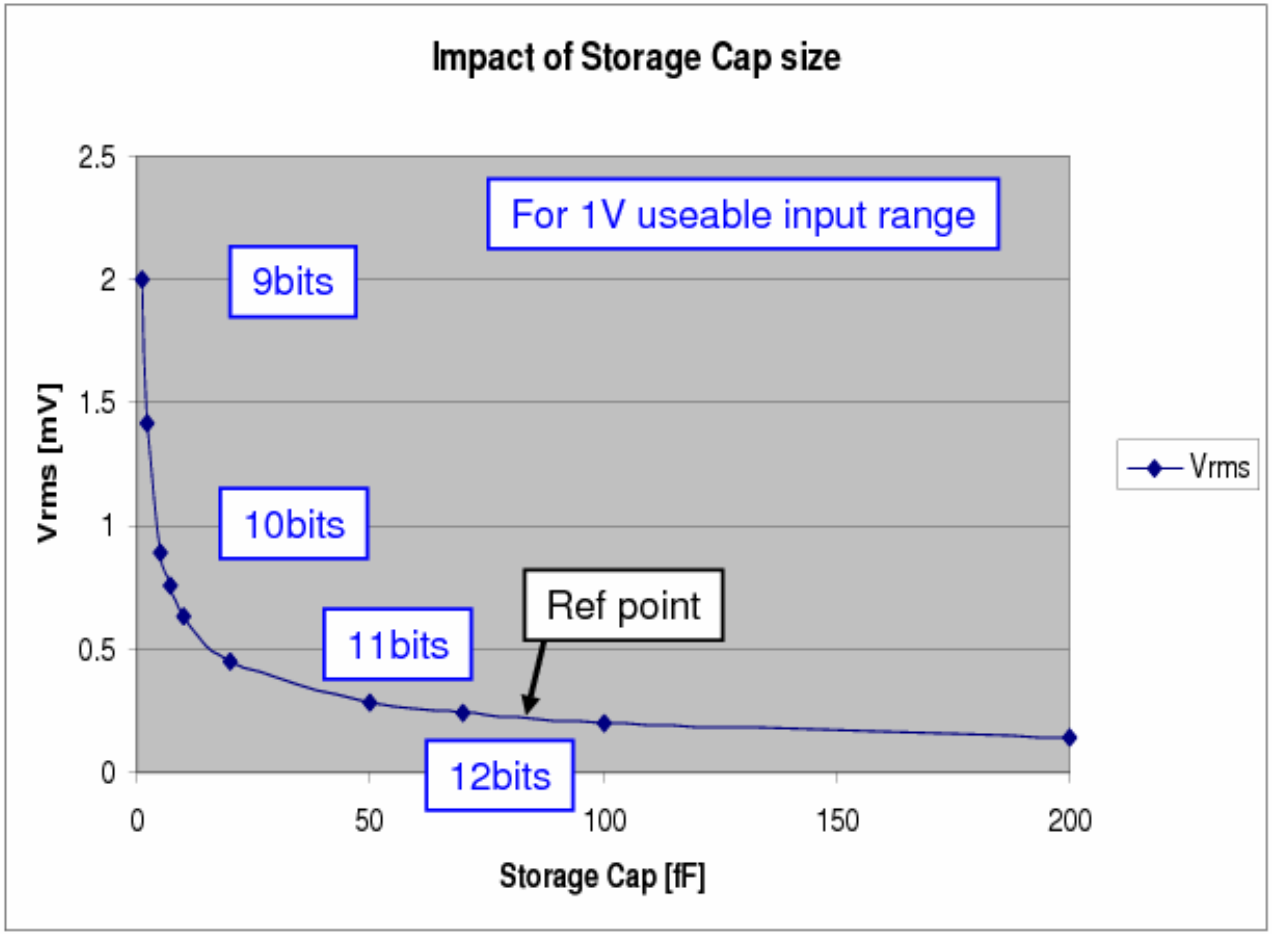
- Main element is buffer amp (OTA)
  - Relatively low current (10's uA) operation possible

Constraint: kTC Noise

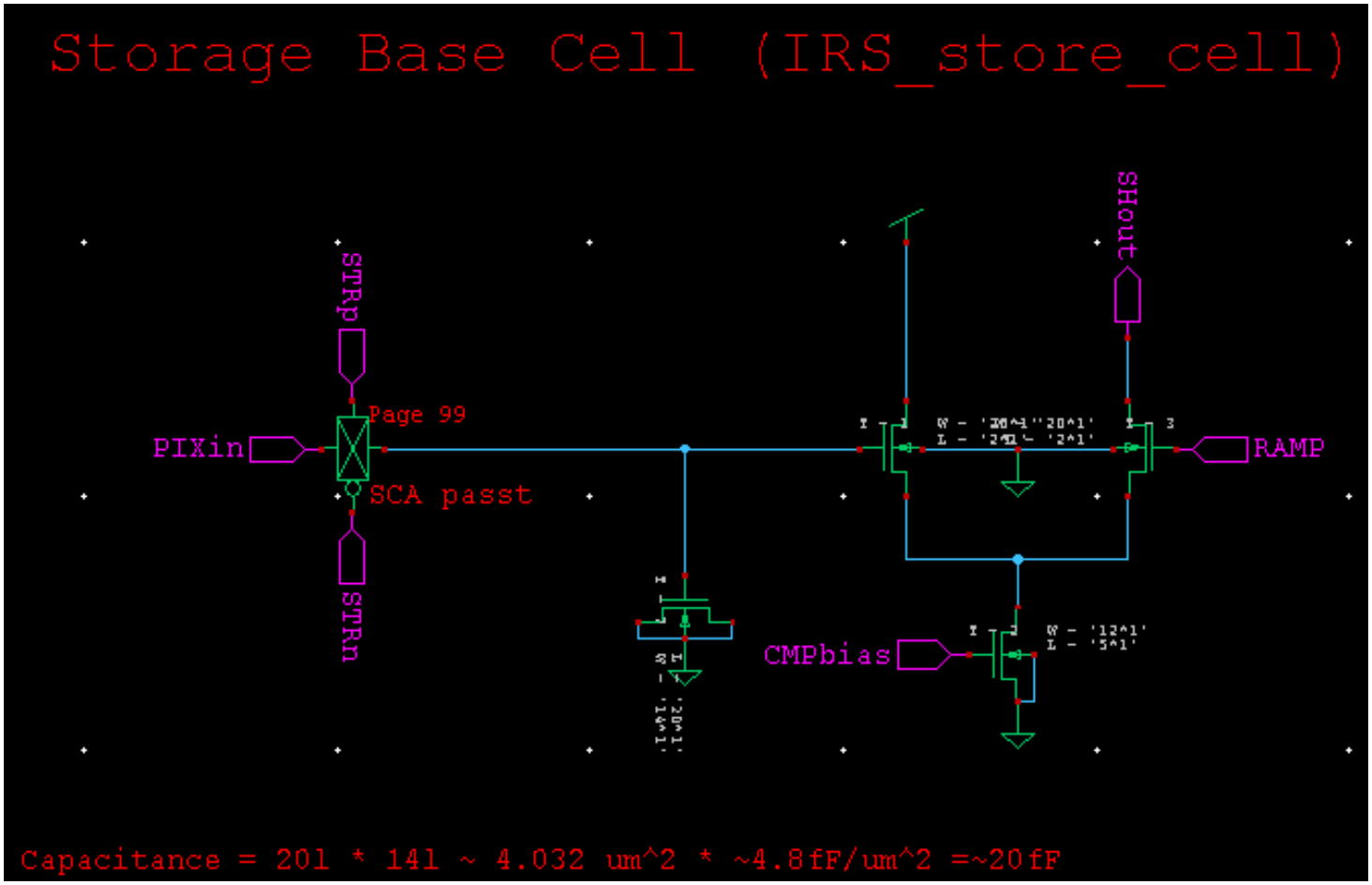
Desire small C for better Input Coupling

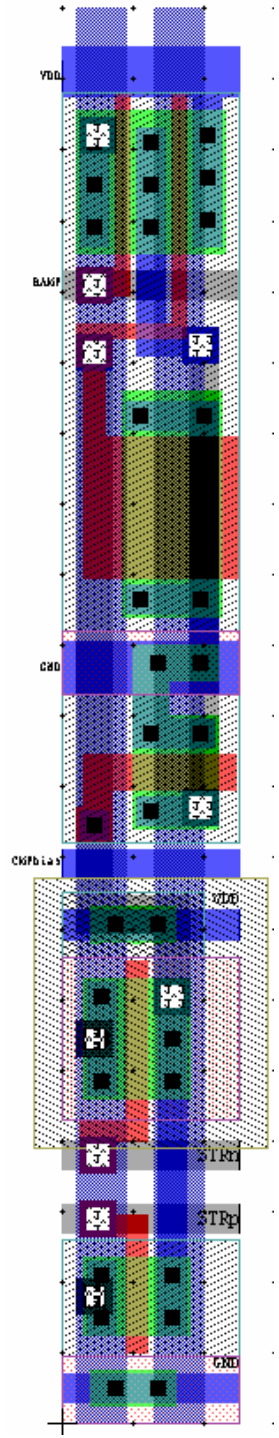


$$v_{rms} = \sqrt{\frac{kT}{C_{store}}} = 0.23mV$$



Storage Cell



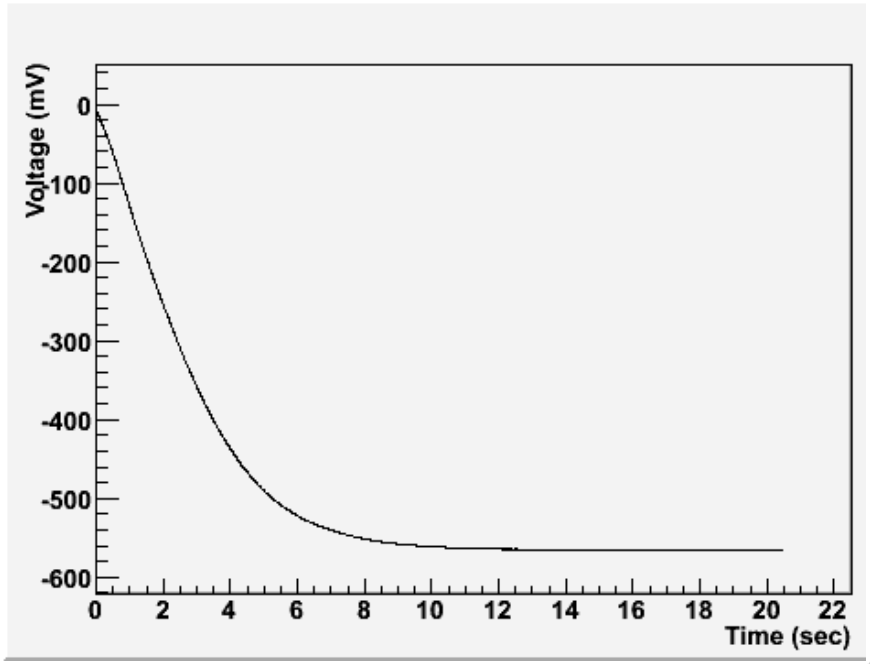


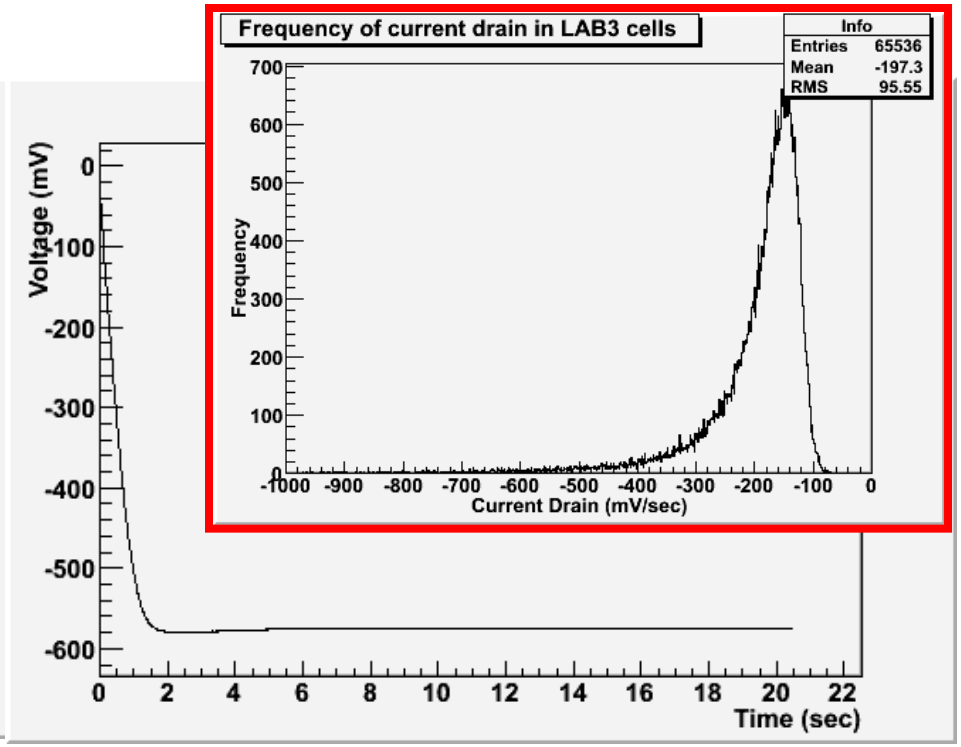
- Diff. Pair as comparator
  - Only power on selected block

Another Constraint: Leakage Current

Need small C for Input Coupling

Can Improve? (readout faster)





Sample channel-channel variation

~ fA leakage typically

Temperature Dependence