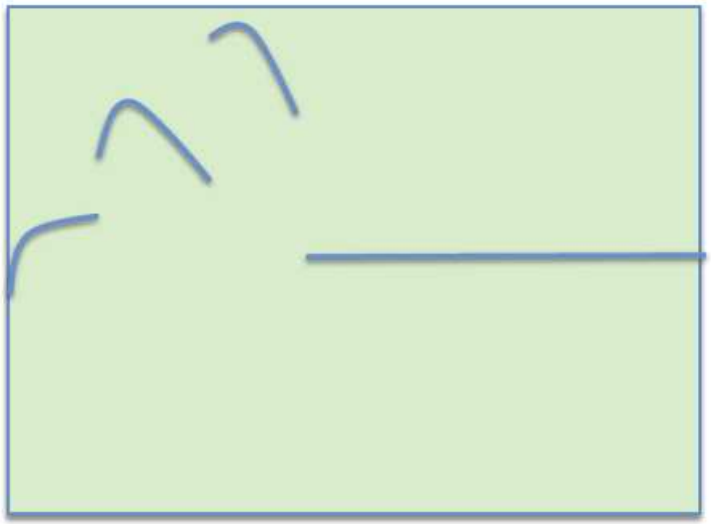
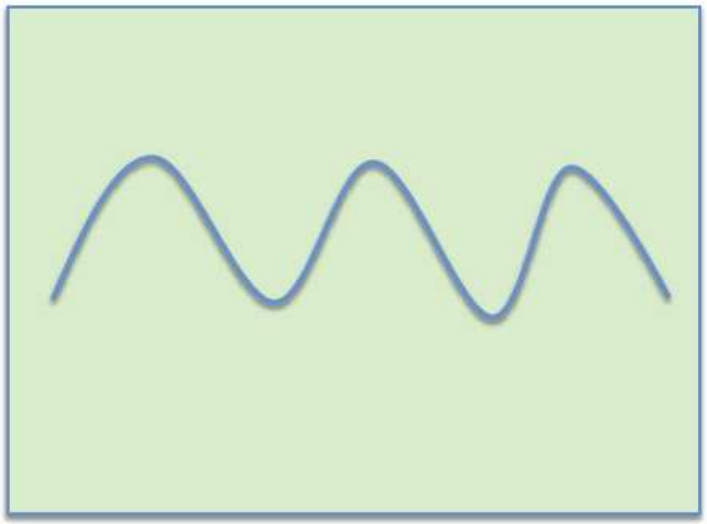
Problem on CH0

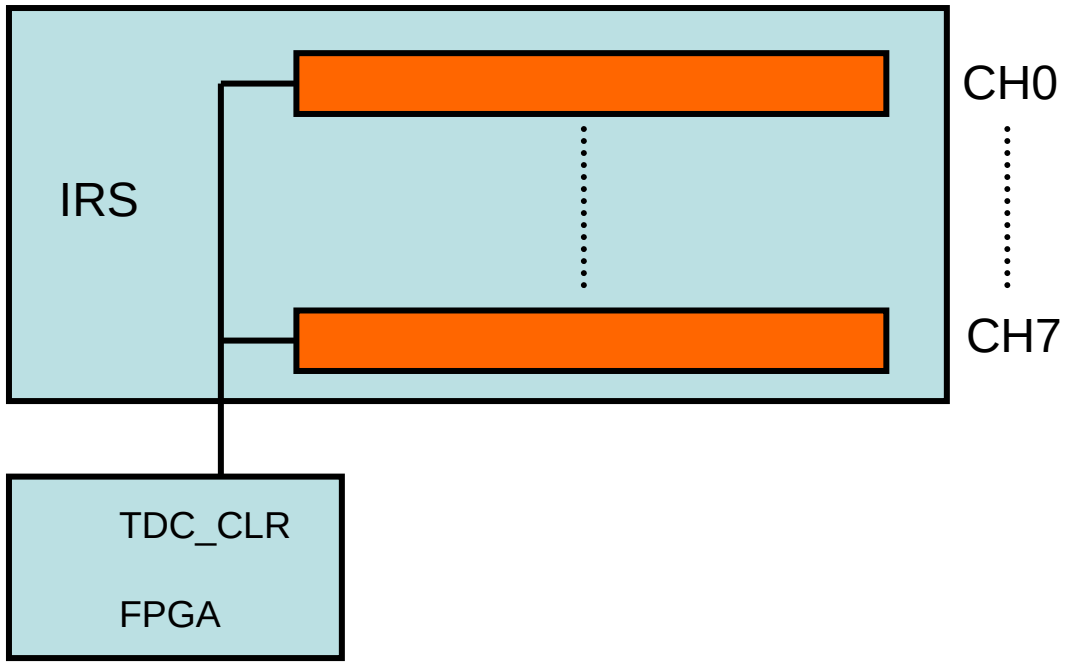
CH 0



CH 7



The Wilkinson counter in CH0 may not be reset.

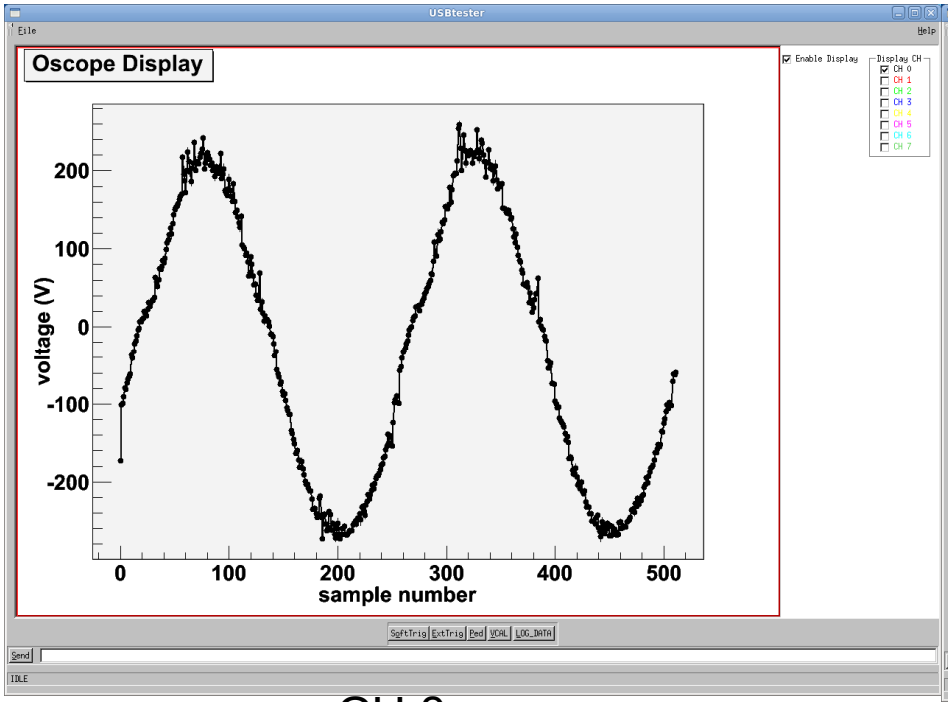


Assumption:
The path from TDC_CLR to CH0 is longer than path from TDC_CLR to CH7.
We need more time for resetting counter in CH0.

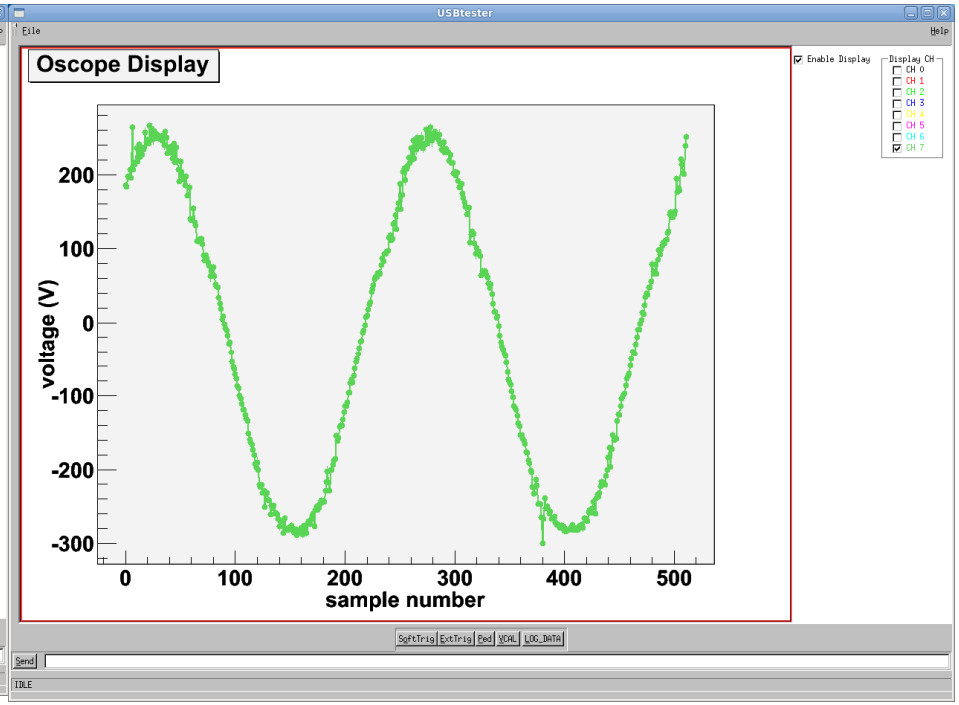
0->1 setup time of TDC_CLR $_{CH0}$ > 0->1 setup time of TDC_CLR $_{CH7}$

Solution:
Extend time of TDC_CLR on “1”
Add new variable: tdc_clr_wait=3 (8x3=24ns)

Waveform displayed on CH0 and CH7



CH 0



CH 7

Timing variable for CH0 may be set to obtain better result (waveform) on CH0

But,

1. The timing variable may not suitable for CH7.
2. Strobe width may be extended 1 or 2 ns but the minimum time unit: 8ns (125MHz) limited by working frequency of FPGA.