Pipelined Readout for Super-Belle

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On Behalf of the Belle Trigger/DAQ Group
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Current System (Nakao-san)

Key technology in 1995

Q-to-T and TDC
charge-to-time conversion
and
Time-to-digital conversion
(instead of ADC)

The greatest idea in the Belle DAQ (my opinion), because

- Unifies the readout system (hardware/software)
- All the detectors (except SVD) can use
- Even for the hit patterns/timing for trigger and KLM
- Was available in the market (minimum R&D)
- Gains high densities, reduce cables (ADC/TDC into one ch.)
Current Belle Sub-Detector DAQ

**SVD** too many channel from too small region
- serialized analog data + flash ADC

**CDC** TDC for drift time / ADC for $dE/dx$
- reduce cable / electronics by Q-to-T

**ACC** pulse height $\propto N_{pe}$ of Cherenkov light (Q-to-T)

**TOF** precise time measurement ($<< 100$ ps)
- time strecher ($\times 20$) before not-so-fast (500 ps) TDC

**ECL** three range of Q-to-T to gain dynamic range (13-bit)
- merge three range Q-to-T output
- recover by the pulse pattern (2/3/4-hit for high/mid/low $E$)

**KLM** serialize hit pattern $\Rightarrow$ multi-hit TDC

**EFC** pulse height measurement, Q-to-T and TDC

**TRG** trigger pattern and timing by TDC
Pipeline Readout

Pipeline Readout?

We know the current FASTBUS system will not work at 10 kHz (Super-B)

- Two buffers in the pipeline readout

  - Pipeline buffer
    - Keep data until trigger decision
    - Waveform analysis for pileup

  - Intelligent FIFO buffer
    - Sparsification
    - Keep data until read out
    - No delay caused by CPU

- New to Belle, but not to BaBar
- Common on many next generation experiments, and even to those of us from SSC
Conversion to Pipelined Readout

- **Current system**
  - Has worked to design specs, but getting long in the tooth
  - Even in current conditions, would benefit from upgrade

- **Pragmatic realities**
  - Manpower limitations
    - Belle has always been very undermanned
    - BaBar leveraged LHC R&D
  - Concurrent R&D with active data taking and analysis
    - Many of those involved in building/commissioning Belle in 1995-1998 were not saturated with analysis responsibilities
  - Having a “common platform” essential

- **COPPER platform**
  - All subsystems deploy sub-detector specific elements on daughter cards (FINESSE) – see Higuchi-san’s talk
  - Common to JPARC experiments – economy of scale
Active Plans

- **Vertexing**
  - Silicon strip (APV25) – Manfred Pernika [Vienna] (CMS)
  - Pixel (APS) readout – (R&D just beginning – see pixel talk)

- **Tracking**
  - Standard ADC/TDC
    - KEK Electronics (M. Tanaka et al.)

- **Particle ID**
  - Endcap RICH – (see P. Krizan’s talk)
  - Barrel PID (TOP/TOF) – (Univ. Hawaii)

- **Calorimeter**
  - Crystal readout (Aulchenko)

- **KLM System**
KEK FINESSE

• TDC Finesse
  – Purpose: Debug of Copper & Finesse system
    Replacement of Fastbus TDC
    Drift chamber tests
    Small cell drift chamber readout system (for Belle)

• FADC Finesse
  – Purpose: Test noise performance of Copper & Finesse
    Study of zero suppressing methods
    TPC readout system (for J-Parc)
    Drift chamber tests
KEK TDC FINESSE

Finesse TDC specification

- Input: 24 channels/Finesse, LVDS type
- Time conversion in AMT – “ATLAS Muon TDC”
- Dynamic range: 84µs
A caveat

AMT is not a true pipelined device – caution (simulations) necessary in new DAQ projects.

Fig. 1. Block diagram of the AMT-1 & 2
TDC Test Results

**Finesse TDC histogram**
(sample=1024)
(input tdc tester = 305.2ns)

- mean = 465.215
- sigma = 0.4224

**TDC TESTER - FINESSE TDC**

*Linear Fit*
\[ f(x) = a + bx \]
- \( a = -1.8588697 \times 10^0 \)
- \( b = +9.9938768 \times 01 \)

**Noise**

**Linearity**
KEK FINESSE ADC

- Analog Input: single-ended or differential
- Dynamic range: 2 V
- 8 channels/Finesse
- 12 bits → resolution ~500μV/bit
- Sampling Clock: 40MHz
- Type: pipeline ADC (AD9235)
- L1 buffering and control: Xilinx FPGA
ADC Response and Noise

- **Response**
  - Missing Codes not observed

- **Noise**
  - Single ended: full width (FW): 4~5 bins
    - \( \sigma \): 2~3 bins
  - Differential: FW: 3~4 bins
    - \( \sigma \): <2 bins
    - less than 1mV

**Histogram of ADC counts for sine wave input**
KEK Development

Analog memory cell (AMC)

This has been done in a collaboration with U-Tokyo group

- AMC 2GHz sampling (16 depth) was developed for evaluation.
- Dynamic range: 4V
- Noise: ~300uV
- Function: confirmed well

- 1GHz sample & 512 depth version will be submitted to the next batch.

Sampled trailing edge
PID Electronics – scenarios

- **Butterfly TOP**
  - ~5 mm position resolution: 40 Ch/counter
  - *200 counters = 1440 channels
  - Multi-hit (hidden cost) > 1440 channels

- **Focusing DIRC**
  - ~few mm x few mm: few kCh/counter
  - *=100 counters: few 100k channels

- **Bar TOP**
  - ~1 mm position resolution: 200 Ch/counter
  - *180 counters = 36,000 channels
Time Stretcher Module

- Designed with LRS
  - R&D 100 Award

16 Channels/1 per DC

Stretch factor 20x

RF clock Reference

VIPA Standard Module
MTS1 Silicon (1)
Precision Timing Update

- Two viable techniques:
  - $\sigma \sim 25$ps (system subtracted)
  - Both require calibration for high precision performance

- Both options are possible
  - Cost benefit to HPTDC solution (<$8$/channel)

Measurements from ALICE-TOF

- Without INL compensation
- After INL compensation
TDC Comparison

- **MTS + TMC Benefits:**
  - We control the design
  - Separate TS and TDC clocks

- **MTS + TMC Negatives:**
  - 2 chips
  - More expensive
  - Less well tested (many users, CERN evaluation)
  - MTS1 must be ported (competing with pixel effort)

- **HPTDC Negatives:**
  - Production order “lifetime buy” in 2004
  - Still a few bugs
  - Complexity: many, many registers...
PID Concerns

- Concern about discriminators
- Our old nemesis, TWC
- Barrel channel count uncertain

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<thead>
<tr>
<th></th>
<th>Belle</th>
<th>BESIII</th>
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</thead>
<tbody>
<tr>
<td>RF/BCO</td>
<td>Spec. &lt;35 ps</td>
<td>Spec. &lt;35 ps</td>
</tr>
<tr>
<td>uncorrected t=0</td>
<td>?</td>
<td>?</td>
</tr>
<tr>
<td>Discrim. Overdrive</td>
<td>?</td>
<td>could be calibrated</td>
</tr>
<tr>
<td>Beam bunch length</td>
<td>2.5 mm 8.3 ps</td>
<td>50 ps 15 mm</td>
</tr>
<tr>
<td>Time Encoding</td>
<td>&lt;20 ps 22 ps</td>
<td>?</td>
</tr>
<tr>
<td></td>
<td>(~42 ps)</td>
<td></td>
</tr>
<tr>
<td>TOTAL</td>
<td>&lt; 40 ps ~45 ps</td>
<td>&lt; 45 ps ? looks difficult</td>
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- GEANT/full simulator contribution:

\[ \sigma^2_{\text{fin}} \rightarrow 100 \text{ps} - \text{“known”} \sim \text{“physics”} \rightarrow 40 \text{ps} \]

From BESIII Workshop June, 2002
Applies to high resolution TOF proposal

NIM A 491 (2002) 54-68

Drift! See Mike Jones talk
TOF Counter Test

TOF Counter, FM-PMT

STRAW2 chip sampling @ 3.3 Gsa/s

@ 3.3 Gsa/s, 15 samples on 5ns risetime leading edge

STRAW2 (uncal.) vs. TDS scope

STRAW2 vs. TDS scope (4GSa/s)

Time [ns]

STRAW2 chip sampling @ 3.3 Gsa/s
Waveform Sampling

- Looks very promising:

- GHz analog bandwidth, multi-GSa/s – depth issue
- Will keep in my back pocket... other possible uses?
2004 Hawaii FINESSE Efforts

- CuEval2 (Migrate to COPPER2)
  [Belle Note “soon”]

- HPTDC

- Precise RF clock required

- STRAW3/LABRADOR
  - 8 chan. * 256 samples * 1k ADCs
  - 8x HS Analog out, 1x MUX out

- COPPER platform deployment
The Simplified (4 two-range channels) CAMAC version of ShaperADC for pure CsI.

Tested.

5 modules are prepared for testing 4x5 pure CsI matrix
- The FINESSE board receives data from one ShaperADC Endcap module (16 channels), or 64 channels per one CoPPER module.

- The FINESSE board transfer to ShaperADC Endcap module 43MHz clock, status information and L1 trigger signal to start data transfer.

- Input Data Flow ---->~ 160 14-bit words under 43MHz Clock control during ~4µs after L1 trigger signal.

- After input control data are directly stored in FIFO buffer of CoPPER module. No data storage on FINESSE board.
Near Term ECL electronics plans

First of all we should mount the pure CsI matrix and carry out it’s beam test. We hope that it will be done during nearest two months.

The 16 channel ADC board for Barrel will be implemented into the current ShaperQT module for detailed testing.

In April we hope to receive VME crate with CoPPER module, we assume to design FINESSE boards to this time, first of all for BARREL and then - for ENDCAP.
KLM Electronics (Nakano-san)

- Do we need TDC to get hit strip info?
- FastOR is necessary?
- hardware decoder on CoPPER? (This is also useful to reduce DATA trans.)
- Try to consider hardware hit decoder on FINESSE

- Some additional work required:
  - Electronics could follow technology choice
Summary

• Expect significant prototyping work this year:
  – Viable existence proof
    • FINESSE/COPPER deployments
    • Pixel Readout
  – Some “production procurement” issues:
    • APV25
      – Fall-back => design our own?
    • HPTDC
      – Fall-back => Monolithic Time Stretcher
  – Manpower very limited

Lifetime purchase in 2004
Back-up slides