DESIGN AND PERFORMANCE OF AN AUTOMATED PRODUCTION TEST SYSTEM FOR A 20,000 CHANNEL SINGLE-PHOTON, SUB-NANOSECOND LARGE AREA MUON DETECTOR

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M.S. Thesis and Final Examination

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Introduction

- Successful physics program of Belle experiment at KEK in Tsukuba, Japan
- Mission to investigate the Standard Model of particle physics, more specifically in a search for:
  - rare B and D meson decays
  - Charge Parity (CP) violation
- The SuperKEKB has a 1.86 mile (3km) circumference, compared to the 16.8 mile (27km) circumference of the Large Hadron Collider (LHC) but it is designed to deliver more than 40 times more collisions between particles than its predecessor

Fig 1: superKEKB particle accelerator ring [1].
Introduction

- Think of Belle II as a digital camera that is about 5-stories high
- Instrumentation Development Laboratory (IDLab) at University of Hawaii at Manoa (UH Manoa) is contracted to design and verify the electronics for two important sub-detectors
  - Imaging Time-Of-Propagation (iTOP) sub-detector
  - $K_L$ and Muon (KLM) sub-detector, where $K_L$ is the long-lived kaons
- Readout system for KLM

**Fig 2**: Image of Belle II spectrometer under upgrade in Tsukuba hall in Japan. The KLM readout system resides as noted in image.
The KLM Readout Electronic System

In order to get 20,000 readout channels, 136 modules are required for the KLM detector where each module covers up to 150 scintillator bars or channels, each reading an MPPC.

Each KLM Readout module, designed by Xiaowen Shi, consists of:
- 1 KLM System Control and Readout Module (SCROD) Rev A5
- 7 - 10 TARGETX Daughtercards (TXDC)
- 1 KLM Motherboard Rev C
- 1 KLM Ribbon Header Interface Card (RHIC)

Fig 3: The KLM Readout Module.
The KLM Readout Electronic System

Table 1: TARGETX ASIC, designed by Dr. Gary Varner, was fabricated in IBM 250nm process.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels per ASIC</td>
<td>16</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>1 GSPS</td>
</tr>
<tr>
<td>Sampling Array</td>
<td>2 x 32 cells</td>
</tr>
<tr>
<td>Storage Array</td>
<td>512 x 32 cells</td>
</tr>
<tr>
<td>Input Noise</td>
<td>1 - 2 mV</td>
</tr>
<tr>
<td>Signal voltage range</td>
<td>1.9 V</td>
</tr>
<tr>
<td>LVDS sampling clock speed</td>
<td>16 MHz</td>
</tr>
<tr>
<td>LVDS digitization and readout clock</td>
<td>64 MHz (16 chan)</td>
</tr>
<tr>
<td>Single Sample Resolution (bits)</td>
<td>10 - 12</td>
</tr>
</tbody>
</table>

Fig 4: TXDC (top) and TARGETX ASIC die (left). The ASIC is encapsulated in 144 LPQF package soldered on TXDC board.
The KLM Readout Electronic System

TARGETX Operation:

Fig 5: Block Diagram of the TARGETX ASIC operation
The KLM Readout Electronic System

TARGETX: Sample Rate vs VadjN

Fig 6: VadjN value can be adjusted to select the sampling speed of the TARGETX.

Fig 7: Driven by SSTin (LVDS) input, the Timing Generator provides all timing signals necessary.
The KLM Readout Electronic System

TARGETX:

Fig 7: Timing Diagram for a Calibrated TARGETX ASIC during 1 GSPS data acquisition.
The KLM Readout Electronic System

Algorithm for Calibration of TARGETX Timing Registers:

1. Control function generator to inject 40MHz sinusoid with 600mVpp amplitude and 1.5V offset.
2. Readout and construct waveform “X”
3. Scale amplitude of waveform “X” to unity.
4. Construct an expected sinusoid “E” by sampling a 40MHz sinusoid with unity amplitude at 1GSPS
5. Use matched filter to achieve synchronization for fitting with normalized waveform actual waveform “X” and expected waveform “E”
6. Plot synchronized waveforms “X” and “E” onto same plot and call it Fitting
7. Plot residuals for “X” and “E”
8. Calculate modified Chi-Squared Test score of “X” and “E” per sample: \[ \chi^2 = \sum \frac{(Observed - Expected)^2}{(Number \ of \ Samples)} \]
9. Use average of modified Chi-Squared Test scores with multiple events to determine optimum bias register value. Minimum score represents the optimized register value.
The KLM Readout Electronic System

TARGETX Calibration:

Fig 8: Optimization sweep of SSToutFB register

Fig 9: Sinusoid fit performed.
Design of an Automated Production Test System

Fig 10: Production testing flow.

- Pre-Testing stage
  - Quick test for shorts of ASICs individually before sending them to be assembled on a daughtercard
- Motherboard Production Testing stage
  - Extensive tests including “noise scan”, “optimize bias”, “sine scan”, and more.
- RHIC Production Testing stage
  - Testing done in a custom crate. Systematic tests include monitoring temperatures and currents. “Trigger scan” is also performed

Fig 11: Test setup for Motherboard Production Testing.
Design of an Automated Production Test System

Fig 12: Software Overview
Design of an Automated Production Test System

Fig 13: GUI System section.

Fig 14: GUI Tests section.
Design of an Automated Production Test System

Serial Numbering and Logging System:

- KLM Readout Module
  - KLMS_0000
- Motherboard Rev C
  - MB_C0000
- SCROD Rev A5
  - S_A5000
- RHIC Rev C
  - RHIC_C0000
- TXDC
  - 0000

Fig 13: GUI Configuration section.
Fig 14: GUI Logs section.
Design of an Automated Production Test System

Remote PostgreSQL database system

- Serial Numbers of electronics are saved
- Summary of the results from tests such as “optimize bias”, “sine scan”, and “pedestal test” are saved.

Fig 15: Displaying the calibrated SSToutFB register values saved in PostgreSQL database using command line.

Fig 16: Data Tables in PSQL.
Characterization of the Readout System

Pedestal Scan

Routine for obtaining pedestals:

AC Coupled Input
1. Turn OFF function generator
2. Generate pedestals
3. Turn ON function generator

DC Coupled Input
1. Turn ON function generator
2. Change amplitude to 1mVpp (smallest)
3. Generate pedestals
4. Turn ON function generator

Since TARGETX incorporates the Wilkinson ADC architecture for digitization, there is an offset for the digital value called ADC count.

Average of the pedestals per sample are recorded and subtracted during data collection.
Characterization of the Readout System

Linearity Test

- TARGETX dynamic range is roughly 2V
- Linearity test performed to also extract transfer function:
  - Voltage [mV] = 0.9032(ADC Count)

Fig 18: Linearity test of the TARGETX ASIC.
Characterization of the Readout System

Noise Analysis

Fig 19: Input noise histogram for a single channel.

Fig 20: Input noise for a single channel. Errorbar plot of mean and standard deviation of each sample.
Characterization of the Readout System

Waveform Quality

Fig 21: A sinusoid fit performed.

Fig 22: Residuals plot.

Fig 23: Residuals Errorbar plot with mean, min and max.
Characterization of the Readout System

Timing Resolution Analysis

\[ t_{\text{zero}} = t_1 + \frac{|A_1|}{|A_1| + |A_2|} (t_2 - t_1) \]

Where:
- \( t_{\text{zero}} \): zero crossing time value
- \( t_1 \): is 1st time value
- \( A_1 \): is voltage value of 1st time value
- \( t_2 \): is 2nd time value
- \( A_2 \): is voltage value of 2nd time value

Fig 24: Use zero crossing algorithm equation to assist in calculating the period of a sinusoid.
Characterization of the Readout System

Timing Resolution Analysis

- Input
  - 20MHz sinusoid
  - 600 mVpp amplitude
  - 1.5V Offset
- 4928 Events
- Initial results did not represent true timing error between samples.
  - Therefore, some timing corrections are needed.

*Fig 25:* Before timing corrections, roughly 200ps timing resolution was measured.
Characterization of the Readout System

Timing Resolution Analysis

**Fig 26:** Period Residuals vs Event Number

**Fig 27:** Period Residuals vs Starting Position
Characterization of the Readout System

Timing Resolution Analysis

Fig 28: Period Residuals vs Event Number

Fig 29: Period Residuals vs Starting Position
Characterization of the Readout System

Timing Resolution Analysis

83ps timing resolution achieved!

Fig 30: Before timing corrections

Fig 31: After timing corrections
Characterization of the Readout System

Production Testing

Some useful summary plots for determining pass or no fail:

Motherboard Production test:
- “Pedestal scan”
- “Sine scan”
  - May signal to retest “optimize bias”

RHIC Production test:
- “Trigger scan”

Fig 32: Used to check for unexpected pedestal offsets or any shorts.
Characterization of the Readout System

Production Testing

“Sine scan” determines retest of “optimize bias”

Fig 33: Fit of a sinusoid with ASIC not optimized.

Fig 34: Failed “sine scan”.
Characterization of the Readout System

Production Testing

“Sine scan” passed after successful retest of “optimize bias”

Fig 35: Fit of a sinusoid with ASIC optimized.

Fig 36: Passed “sine scan”.
Characterization of the Readout System

Production Testing

“Trigger scan” useful in debugging RHIC board, interconnect cables and ASIC triggering

Fig 37: Initial “Trigger scan” before corrections are not useful.

Fig 38: “Trigger scan” after corrections are useful for verifying triggers from ASICs.
Summary

- Hardware verification and testing for all 20,000 channels of the KLM sub-detector for Belle II for superKEKB particle accelerator in Japan is complete.
- Electronics are installed in Japan by Dr. Isar Mostafanezhad.
- Debugging for readout in its new environment must be done.
- Networking issues.
- Big data with data concentrator.
- Much more development needed in firmware and software.

Table 2: Production test yield summary.

<table>
<thead>
<tr>
<th>Board</th>
<th>Pass</th>
<th>Fail</th>
<th>Pass Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCROD</td>
<td>156</td>
<td>13</td>
<td>91.66%</td>
</tr>
<tr>
<td>Motherboard</td>
<td>156</td>
<td>9</td>
<td>94.23%</td>
</tr>
<tr>
<td>TARGETX ASIC</td>
<td>1464</td>
<td>108</td>
<td>92.62%</td>
</tr>
<tr>
<td>RHIC</td>
<td>156</td>
<td>4</td>
<td>97.43%</td>
</tr>
</tbody>
</table>
Acknowledgements

- Prof. Gary Varner
- Collaborators at PNNL, KEK, Indiana University and Virginia Tech
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  - Khan Le
  - Weng Lam Sio
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for who I am today

And Viewers Like You!
What am I working on today?

- Automated test for the high voltage assemblies of iTOP sub-detector in Japan - **DONE**
- Automated Production test for electronics of KLM sub-detector in Japan - **DONE**
- Automated Production test for electronics of miniTimeCube project at NIST in Maryland - **DONE**
- Picosecond 5 Prototype (P5P) Waveform Sampling/Digitizing ASIC - **Currently working on**
  - 10 - 20 GSPS

![Fig 39: PSEC4 die as an example.](image)