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A new multi-hit Time-to-Digital Convertor (TDC) ASIC for the Deep Underwater Muon and Neutrino Detector (DUMAND)

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The DUMAND II Digitizer

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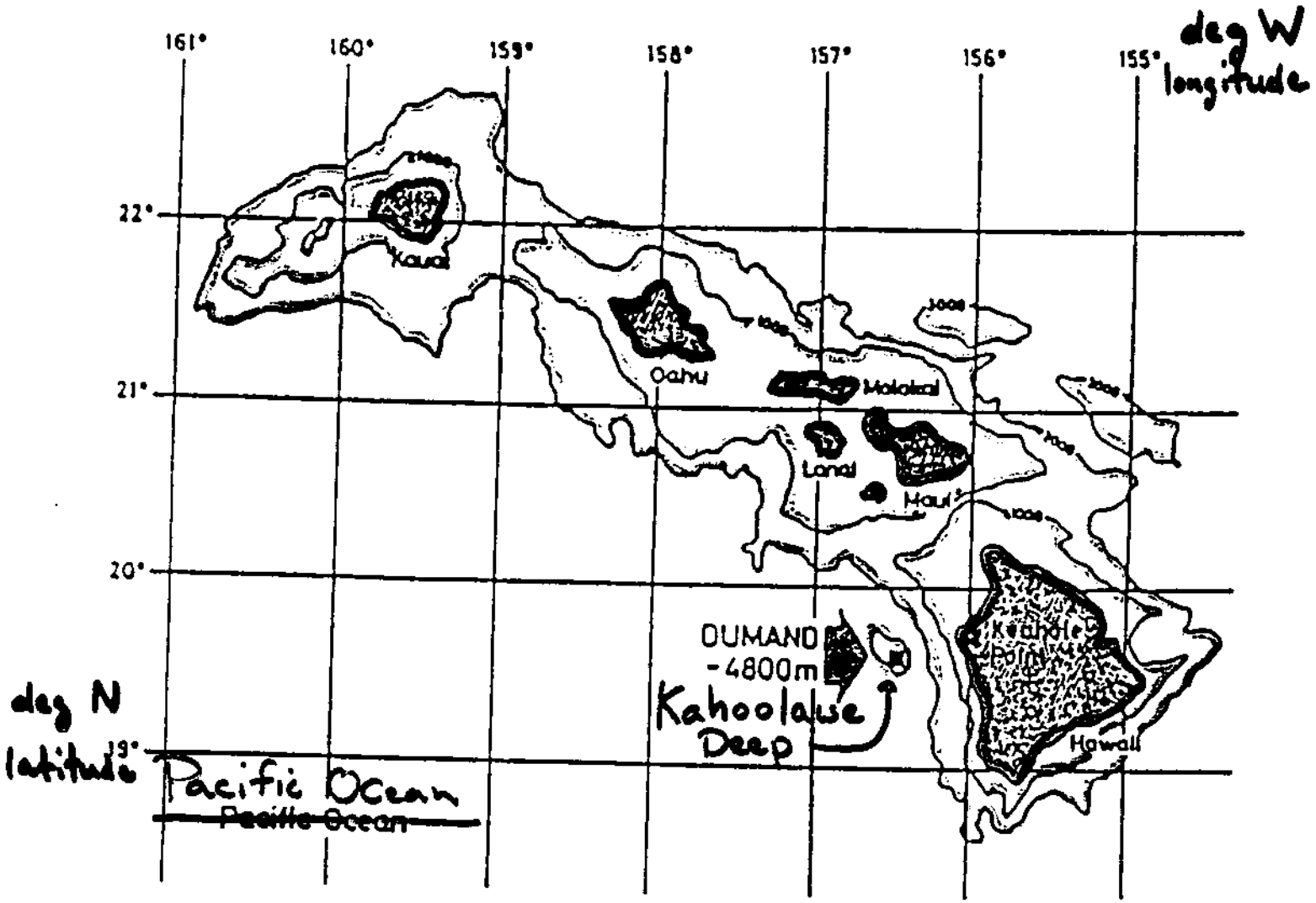
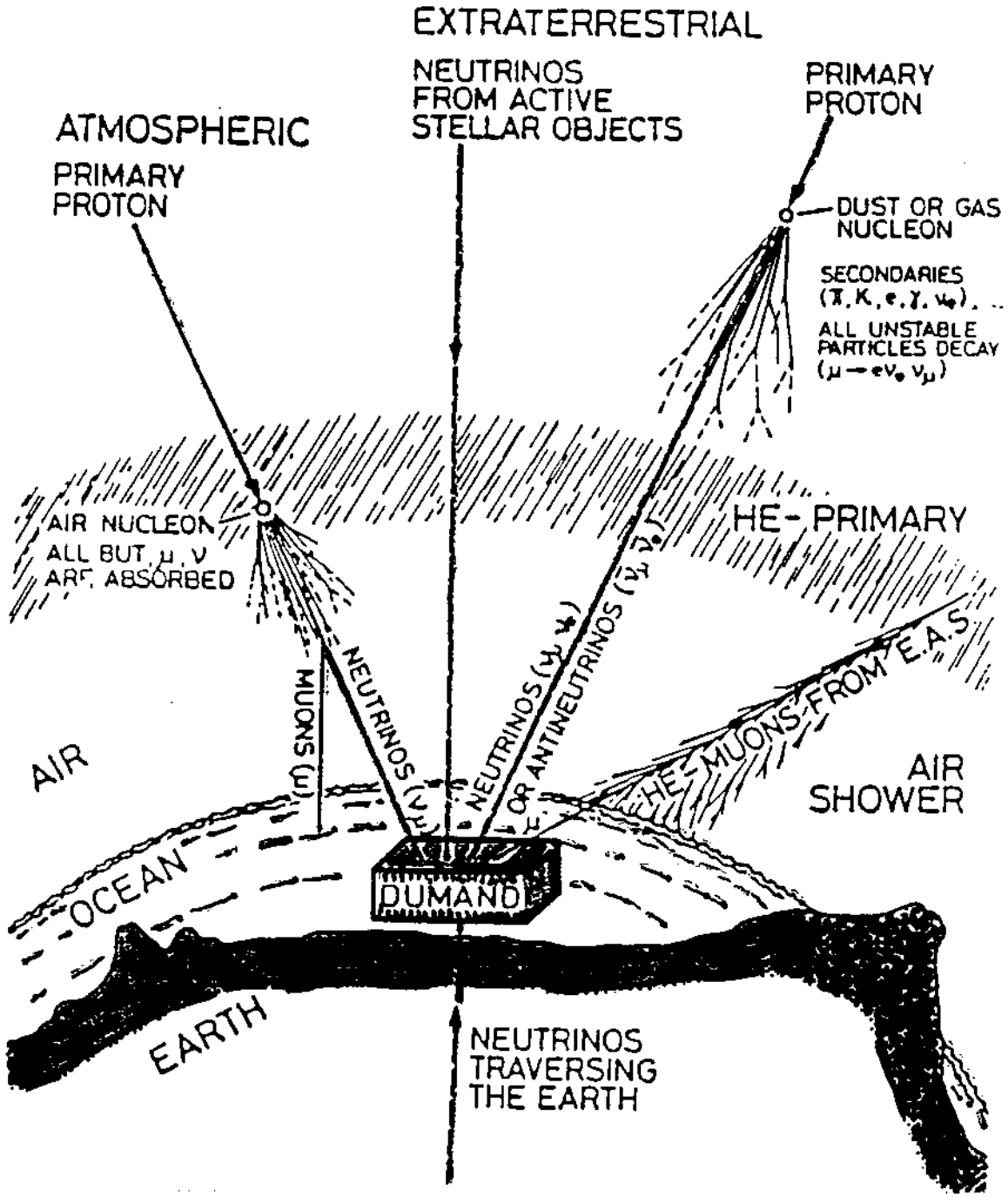
Deep Underwater Muon and Neutrino Detection

The DUMAND Site

Physical Characteristics

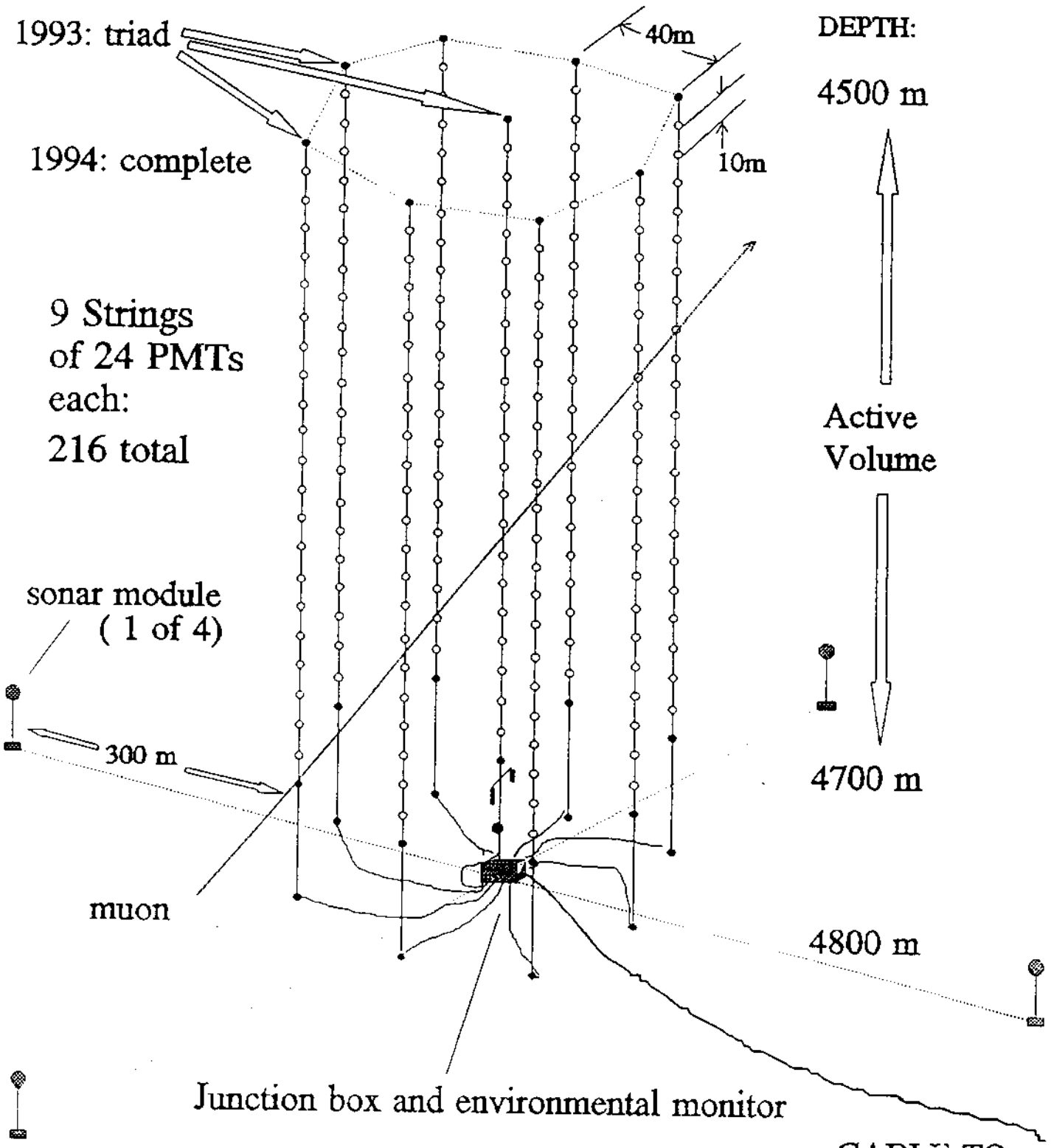
- 8 oceanographic cruises 1980 - 1986
- bottom sediment flat to 1m in 1km
- current velocity, max < 11 cm/s, avg ~2 cm/s, typical ~4-5 cm/s
- biofouling/sedimentation negligable for 1.5 yr test
- water clarity $\lambda \sim 40$ m
- background light (biolumin, K^{40}) understood & managable




EXTRATERRESTRIAL
NEUTRINOS FROM ACTIVE STELLAR OBJECTS
PRIMARY PROTON
ATMOSPHERIC
PRIMARY PROTON
DUST OR GAS NUCLEON
SECONDARIES
ALL UNSTABLE PARTICLES DECAY
AIR NUCLEON
ALL BUT μ, ν ARE ABSORBED
HE-PRIMARY
MUONS (μ)
NEUTRINOS (νμ)
NEUTRINOS (νμ)
OR ANTINEUTRINOS
HE-MUONS FROM E.A.S.
AIR
AIR SHOWER
OCEAN
DUMAND
EARTH
NEUTRINOS TRAVERSING THE EARTH

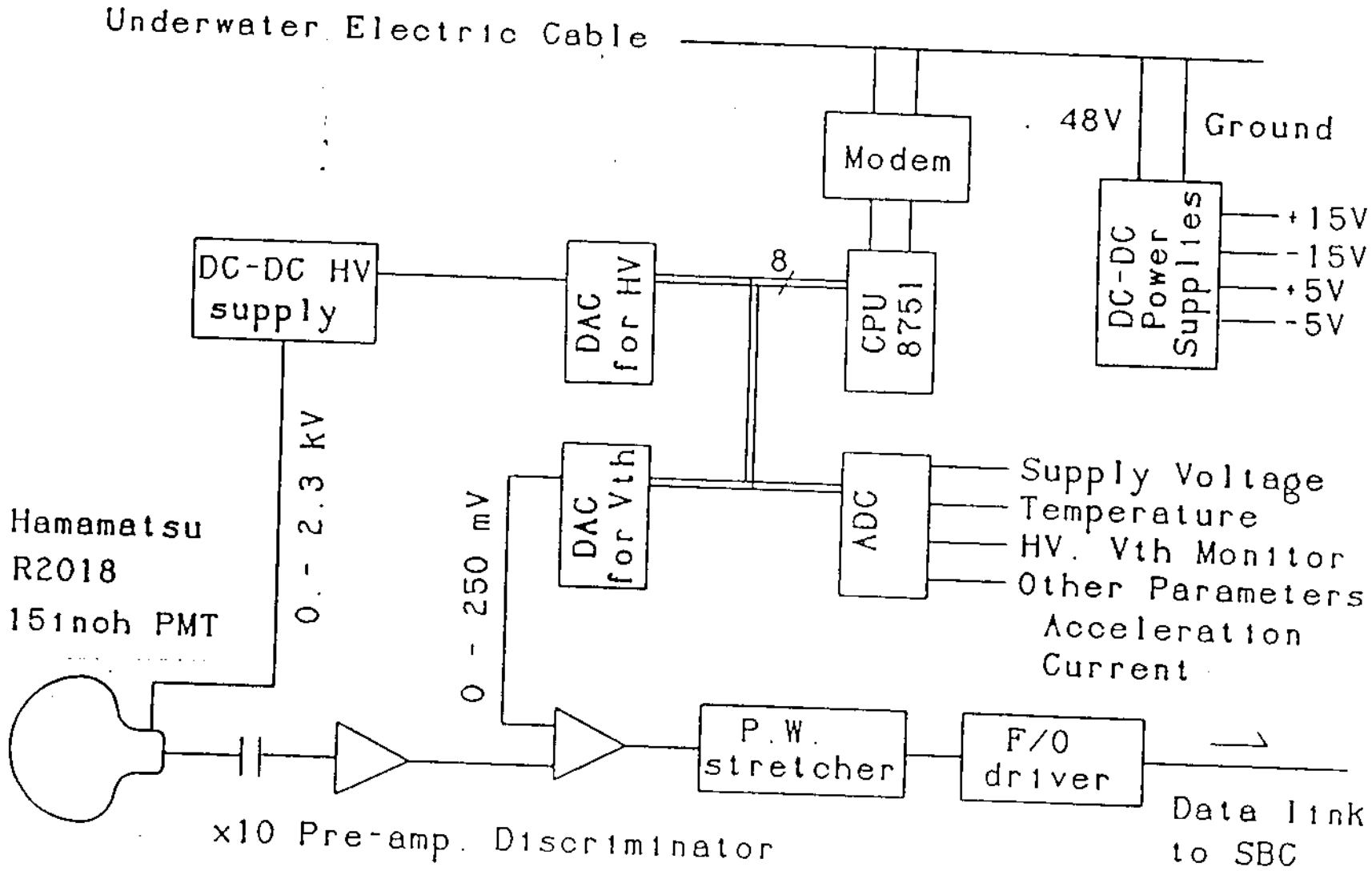
DUMAND II Astrophysical Neutrino Telescope

Active volume dimensions: 200 m high, 100m diameter



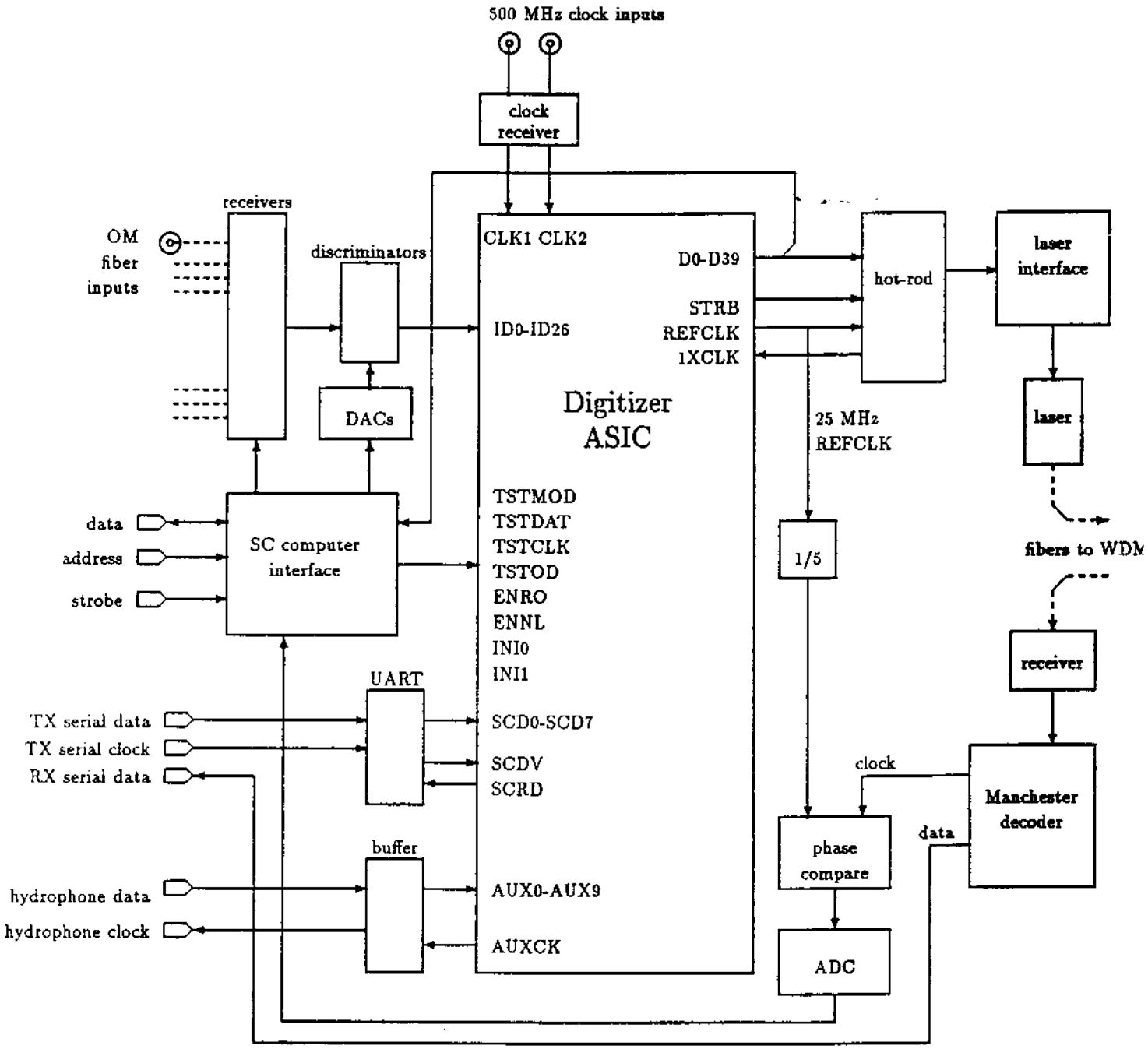
(not to scale)

OM Circuit Block Diagram



DUMAND SC Digitizer PC Board

BLOCK DIAGRAM

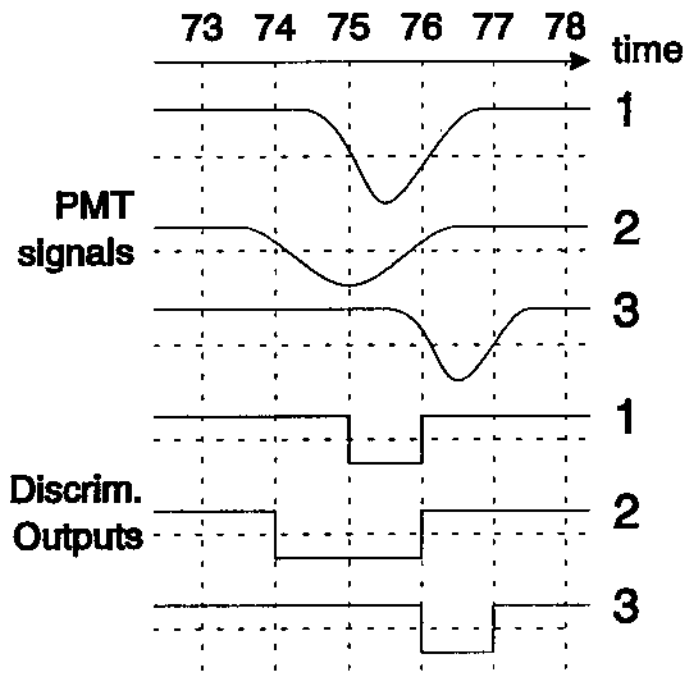


SC Digitizer PC Board Block Diagram

Digitizer Specifications

Resolution	1 ns least count
Number of Channels	27 → TIME-ORDERED
Readout	Continuous, Deadtime-less
Peak Input Rate	500 MHz Instantaneous
Sustained Input Rate	50 MHz (readout limited)
On-Chip Buffering	50 Hits (2 edge times/hit)
Package	415 Pin PGA (0.050" pitch)
Power Requirements	+3.3V, 160 mA -2.0V, 7.5A
Inputs	Differential ECL
Outputs	40 Bit TTL word
Clock	0-500MHz, diff ECL
Base Array	Vitesse VGFX200K, GaAs 200K raw gates, DCFL logic

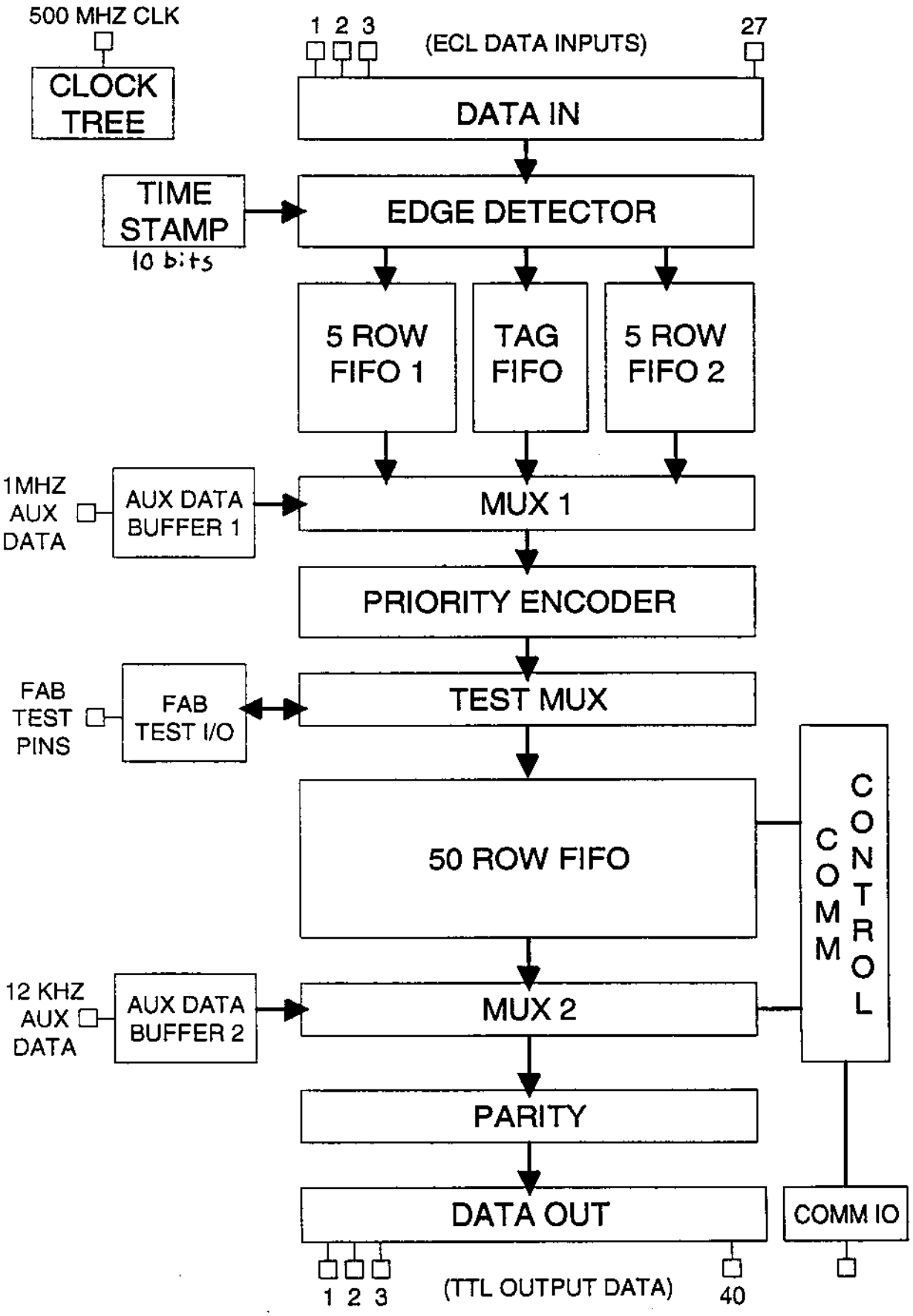
The Multichannel Digitizer Chip



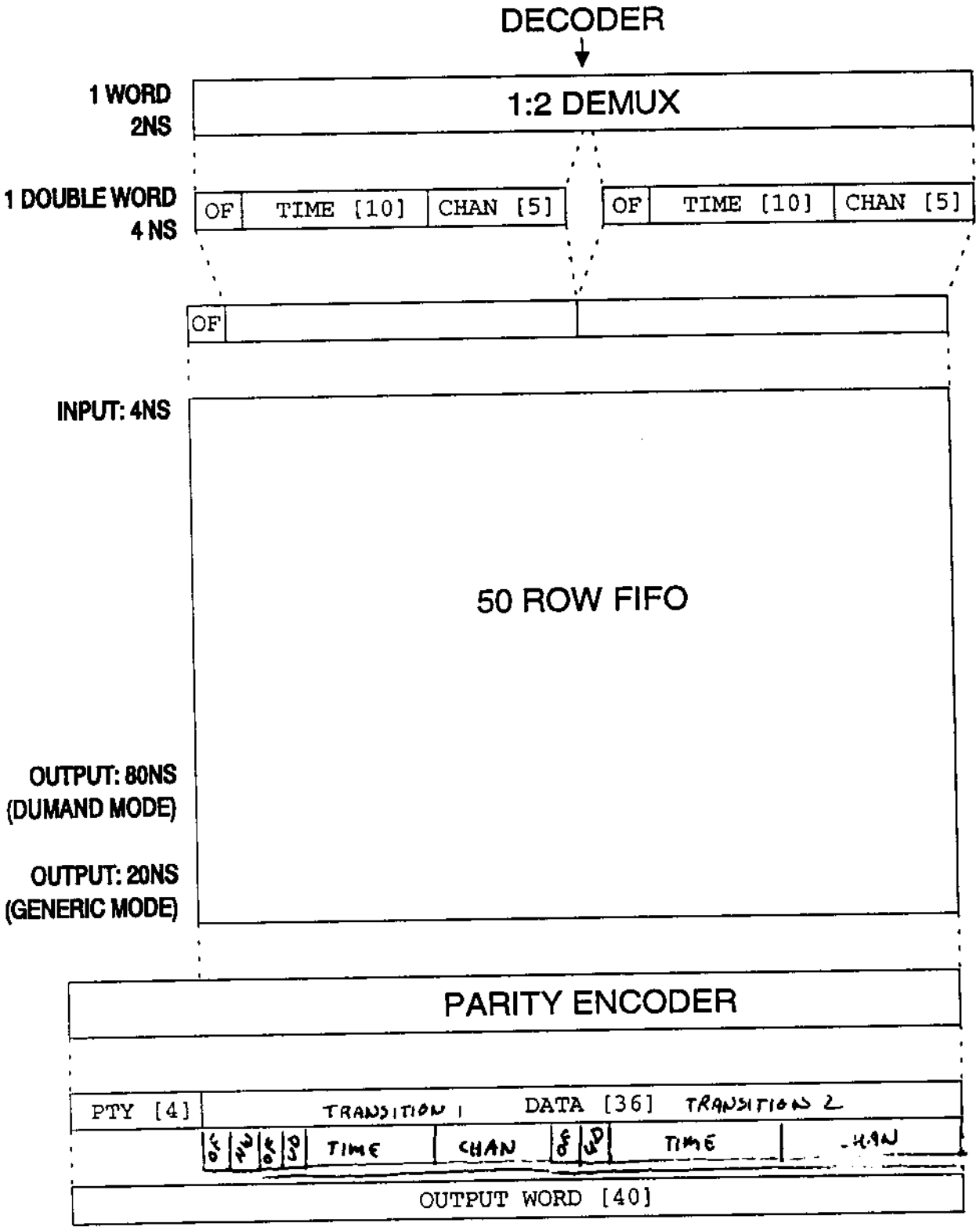
DIGITIZER
edge detectors
priority encoder
queueing

channel number	change bit	time in ns
2	0	74
1	0	75
1	1	76
2	1	76
3	0	76
3	1	77

DIGITIZER ASIC BLOCK DIAGRAM



OUTPUT BUFFERING



ASIC OUTPUTS (TTL)

ASIC TECHNOLOGIES

(as of 1990)

technology	*DELAYS (ps)*		*Max recom.*	*complexity*	*estimated*
	Gate	*Flip-Flop*	*clk speed*	*(gates)*	*speed*
1. ECL (1.5 μ)	200ps	400ps	1.2 GHz	30K	660 MHz
2. ECL (0.8μ)	100ps	200ps	2 GHz	80K	1.3 GHz
3. GaAs (SCFL)	100ps	200ps	2 GHz	6K-10K	1.3 GHz
4. GaAs (DCFL)	175ps	500ps	1 GHz	200K	650 MHz
5. CMOS (0.8 μ)	500ps	1ns?	200MHz?	>100K	260 MHz
6. Bi-CMOS	? (too new)				

Technology notes:

1. Silicon Emitter-Coupled Logic. Old technology, power-hungry. Proven.
2. Gallium Arsenide Source-Coupled FET Logic. Relatively new; somewhat lower power than ECL. Electrically quite similar to ECL.
3. Fastest production ASIC technology.
4. Gallium Arsenide Direct-Coupled FET Logic. Substantially lower power than ECL, but not as fast.
5. Silicon Complimentary Metal-Oxide Semiconductor. Old technology, but specs given are for state-of-the-art .8 micron feature size. Still not quite fast enough for us.

Speed

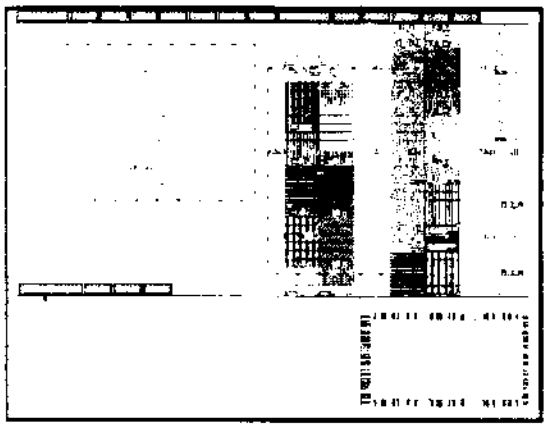
Estimated operating speed for our application, caculated as:

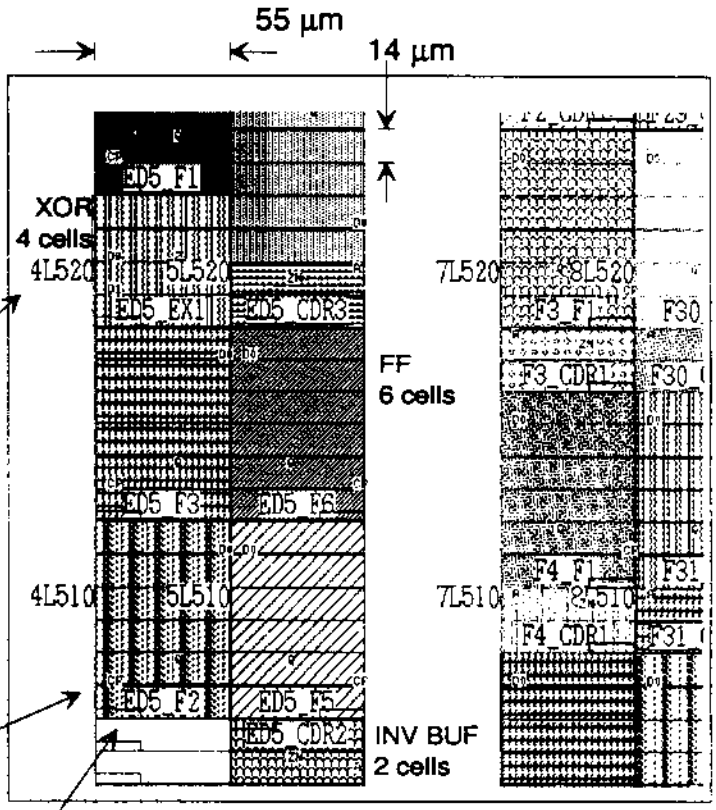
$$F_{\max} = \frac{1}{1.5 \cdot (3t_{gate} + t_{SU} + t_H)}$$

t_{gate} = typical gate delay
t_{SU} = FF set-up time
t_{PROP} = FF CK → Q

This assumes that a maximum of 3 levels of combinatorial logic are required between flip-flops. The 1.5 derating factor is for IC manufacturing process variations, operating temparature variations, etc.

Vitesse VSCGPRE graphical preplacement tool



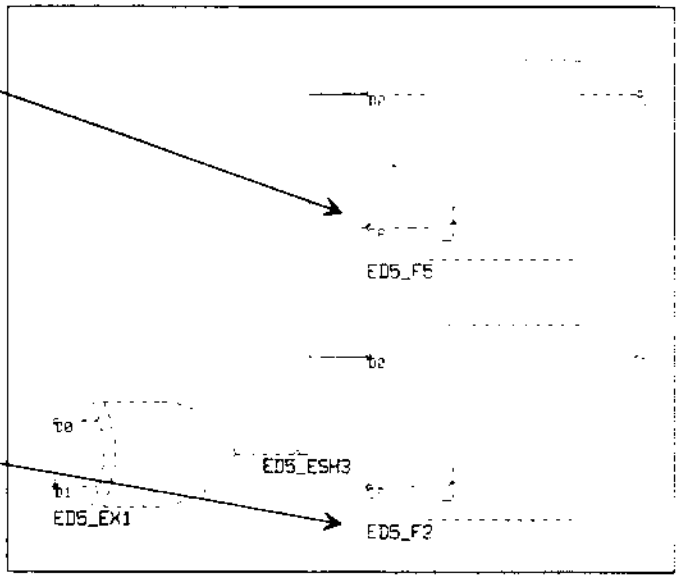


Cell Placement View

Cell address
(col 4, row 20)

Pin location
(CP = clock input)

Cell reference name
(ED5_F2)



Schematic View

Data inputs (FIFO)

Priority encoder

DUMAND TDC Pin Description 22NOV92-GSV

Data Inputs

DIN(1:27)	Data Input Negative (ECL)	1-24 Optical Data
DIP(1:27)	Data Input Positive (ECL)	25-26 Calibration
		27 Null Word arrival

Clock Input

CLKN	Negative Clock phase (ECL)
CLKP	Positive Clock phase (ECL)

Computer Interface

NW(1:9)	Null Word Data (TTL inputs)
NWDSBL	Null word Disable (H) (TTL)
NWS	Null word Strobe (TTL, latch on rising edge)
RW(1:10)	Rollover word data input (TTL)
RWDSBL	Rollover Word Disable (H) (TTL)
RWS	Rollover Word Strobe (TTL)

Control Signals

GRAY	Convert time to Gray code (TTL active high)
RSE	Reset Sync Error (TTL active high)
RST	Major Chip Reset
SD(1:3)	Select REFCLK Rate (TTL) (50MHz Steps)
SYNERR	Synchronous Logic Error Detect (TTL)

High Speed Test Pattern Input

CLK24	Clock IN for SIN (ECL)
SIN	24 bit Serial Input
TRIG	Triggers Serial Loaded Test Pattern (ECL)
TST	Enable Test Mode (TTL)

Performance Test Pins

ACI	a.c. test input (ECL)
ACO(1:3)	a.c. test outputs (ECL)
DCO	d.c. test output (TTL)

Hot Rod Interface (All TTL)

FCODO(1:5)	Channel# for first hit
FOVFO	First Word, 5 Row FIFO Overflow
FSOVFO	50 Row FIFO Overflow
FSTO	First Word, up-down Transition
FTMO(1:10)	First Word, time of hit
NWTO	Null Word I.D. bit
REFCLK	Reference Clock for Hot Rod
FTY(1:4)	Parity Out (1=1,5,9,...); (2=2,6,10,...); etc.
RSD	Reset Hot Rod clock Divider (Active high)
SCODO(1:5)	Channel # for second hit
SOVFO	Second Word, 5 Row FIFO Overflow
SSTO	Second Word, up-down Transition
STMO(1:10)	Second Word, time of hit
STRB	Hot Rod Strobe
XCLK	Hot Rod division of Refclock

DUMAND/g-2 Operation Pins

G2DMP_	g-2 dump word input (ECL active low)
G2DVO	g-2 data valid output (ECL active high)
G2E_	DUMAND/g-2 Mode Select (TTL) H = DUMAND L = g-2

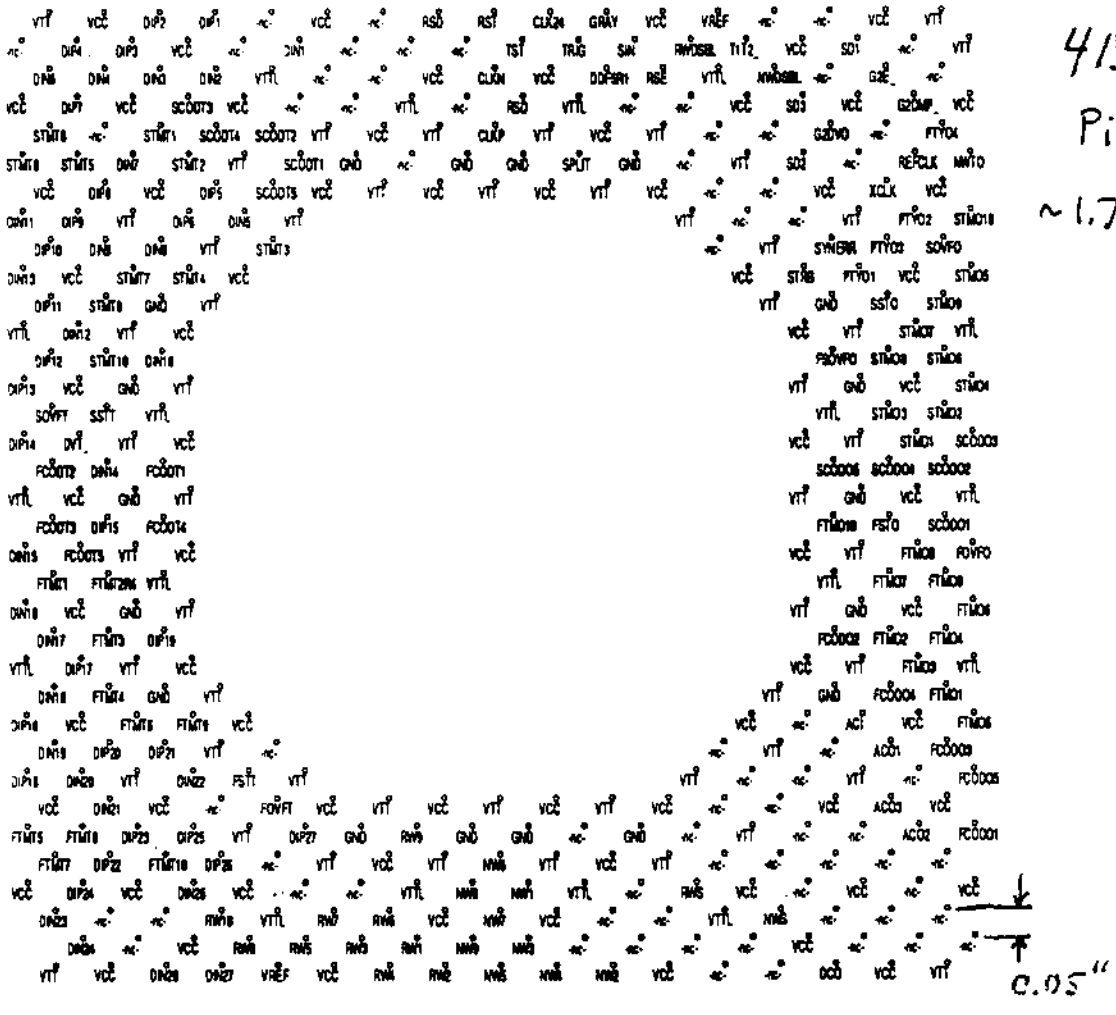
Fab. Test Pins (normally n.c.'s)

DDF5R1	Disable 5 Row FIFO 1 (TTL) (H=Normal Op.)
DVT_	ECL I/O
FCODT(1:5)	FCODO test
FOVFT	FOVFO test
FSTT	FSTO test
FTMT(1:10)	FTMO test
SCODT(1:5)	SCODO test
SOVFT	SOVFO test
SPLIT	Enable Fab. Test pins (TTL) (H = Normal Op.)
SSTT	SSTO test
STMT(1:10)	STMO test
T1T2_	Time test (TTL)

POWER:
$V_{CC} = 0V$
$V_{TT} = -2.0V$
7.5A
$V_{TTL} = +3.3V$
.2 A
$V_{REF} = -1.35V$

415 PGA Pinout

~1.7"x1.7"



0.05"

Some Conclusions

ASIC runs very well! Exhaustive testing, including full DUMAND String Controller system is currently underway. All run up to 500MHz (1ns resolution), although some fail very shortly above that. Some evidence of clock attenuation through package at higher rates.

Vitesse Semiconductor has produced ~60 dies and are ready to package.

Investigating observed 1 in 10^6 errors. Not clear if the ASIC or the test bench. Could be a metastability issue in the Edge Detector and so will continue to investigate.

Current/future applications:

3 DUMAND Strings in final assembly for deployment in 4 weeks. Remaining 6 strings of phase II in 1995.

muon g-2 (BNL E-821) will use ~30 ASICs packaged in custom VME modules. Scheduled for installation in mid-1994.

Proposed Intelligent low energy trigger scheme for Super-Kamiokande. This "SMART" trigger scheme proposes to use 16 or 41 ASICs to allow efficient triggering at < 5 MeV energy threshold.

?? You tell us. At ~$1k/per in small quantities, we feel there are many applications where this chip could be used cost effectively. The continuous readout feature provides a strong complement to the LeCroy MTD132.