DUMAND SC Digitizer ASIC Specification

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1 General Description

This note describes the Digitizer ASIC for the DUMAND (Deep Underwater Muon and Neutrino Detector) SC (String Controller). ***This specification is preliminary, and is subject to revision as the logic design proceeds.***

The digitizer system comprises a single large ASIC (application-specifc integrated circuit), described here, and various supporting circuitry. We plan to fabricate the ASIC using Vitesse Semiconductor's VGFX100 GaAs gate-array technology. The logic design is being done at Boston University on our Mentor Graphics CAE system.

This digitizer measures arrival time of both leading and trailing edges of 27 ECL inputs (24 Optical Modules and 3 Calibration Modules). When any input changes state, the time is recorded to 1nS. The time, along with a binary channel (input) number is output as a parallel word. Internal buffering is provided for at least 100 events to accomodate fluctuations in input rate. The output of the digitizer is a 40-bit TTL double word, designed to be compatible with the Gazelle "Hot-Rod" high-speed serial communications chipset, but can be interfaced to other devices.

2 ASIC Specifications

2.1 Clock

The ASIC operates at 500MHz, using an external two-phase clock. This clock will be provided by a separate clock (CSG) module. The clock frequency and phase will be adjustable using two DACs controlled through the SC computer.

2.2 I/O pins

Following is a list of the I/O pins. Test pins are not included.

number	Name	I/O	*type*	*description*
2	CLK1	I	ECL Diff	500 Mhz clock ϕ 1
2	CLK2	I	ECL Diff	500 Mhz clock ϕ 2
27	ID0..ID26	I	ECL Diff	fast data inputs
2	INI0, INI1	I	TTL?	chip initialization
1	TSTMOD	I	TTL	test mode selection
1	TSTDAT	I	TTL	test data
1	TSTCLK	I	TTL	test clock
1	TSTOD	I	TTL	hot-rod output data enable
10	AUX0..AUX9	I	TTL	aux data inputs
1	AUXCK	O	TTL	aux data clock
8	SCD0..SCD7	I	TTL	SC data
1	SCDV	I	TTL	SC data valid flag
1	SCRD	O	TTL	SC read data pulse
40	D0..D39	O	TTL	parallel data out
1	REFCLK	O	TTL	Hot-Rod transmitter clock
1	1XCLK	I	TTL	1X word clock from Hot-Rod
1	STRB	O	TTL	TX strobe to Hot-Rod
1	ENRO	I	TTL	enable roll-over words
1	ENNL	I	TTL	enable null words

3 Design Details

3.1 Operation

For each input transition, a 10-bit *time field*, 5-bit *channel number*, and 1 bit *up/down flag* are transmitted. Every 1μS (when a carry occurs from the 10th time bit), a roll-over word with *channel number* = 0 is transmitted.

The *time field* of roll-over words is by definition zero, so the 10 time bits and *up/down flag* are available for auxiliary data. An overflow bit is set to indicate lost data if any of the FIFO buffers overflows.

3.2 Block-by-Block Description

Refer to the attached block diagram, and data format table.

3.2.1 Input - Edge Detector

Each of the 27 inputs is sampled by two edge-triggered flip-flops, one driven by each clock phase. The resulting signals (F1 and F2) are XORed, producing a signal Z which identifies when a change of state takes place. The Z's are logically ORed to produce a TRIGGER signal, which indicates that data should be recorded. The output of this block is two sets of 27 sampled data bits (F1 and F2), two sets of 27 change bits (C1 and C2), and a TRIGGER signal.

3.2.2 Clock

The clock is a 9 bit synchronous counter, clocked at 500MHz. Its outputs are latched by the TRIGGER signal from the input block. The carry output of the counter itself sets a flag, resulting in an extra ("roll-over") word being inserted in the data stream every 1024nS.

3.2.3 Primary FIFO Buffers

The data is then written to two FIFO buffers, one driven by each clock phase. Data is only written when a TRIGGER is recieved from the front-end. A new word may be written to each FIFO every 2nS.

If a FIFO is full when a write is attempted, a reserved bit (OF) is set in the top word to indicate an overflow condition, and the data is not written.

These FIFOs are designed to have zero latency; that is data written in on one clock cycle is available at the output immediately without any time required for "fall-through".

3.2.4 "Tag" FIFO and Data Selector

The "Tag" FIFO contains four extra bits, which keep track of the order in which words were written into the two primary FIFOs. Another bit flags

the occurrance of clock roll-overs. Based on the contents of the Tag FIFO, the read logic generates roll-over words when necessary, and reads words out of the two primary FIFO buffers in time order.

3.2.5 Encoder

The encoder scans the FIFO outputs, and looks for state changes. Each state change produces an output word with time and channel number.

The data bits (F1 and F2) of the FIFO output words are XORed, producing 27 signals (Z), which are latched. A Z=1 represents an input which has changed state. The Z's are stored in 27 flip-flops, each with it's own reset input.

The Z's feed a 27-input priority encoder. Each clock cycle (every 2 nS) it produces as output a 5-bit binary number for the lowest-numbered active input. This becomes the channel number in the output data stream. The priority encoder also resets the corresponding latch.

3.2.6 Clock Roll-Over and Aux Data

Roll-over words require special treatment by the encoder. A roll-over word (with *channel number* = 31) is output first, followed by normal data words for any valid data in the word.

When a roll-over word is generated, the 10 bits of clock data in the phase 0 data are replaced by 10 bits of external "slow" data (from hydrophones in DUMAND). A pulse is provided on the AUXCK pin to tell external circuitry that the hydrophone data has been read.

3.2.7 Secondary FIFO Buffer

The encoded data is stored, two words at a time, in the **Secondary FIFO**. The depth of the **Secondary FIFO** is not known exactly at this time, but will be at least 50 double words. Data may be written to the **Secondary FIFO** at a rate of one double word every two clock cycles (every 4nS).

The FIFO is a true "fall-through" FIFO. Data written at the "top" (input) is clocked downwards to the last unoccupied location.

Data may in principle be read from the FIFO at a rate of one double word every two clock cycles (4nS). In normal DUMAND operation, one double word is transmitted off-chip every 80nS to the Gazelle Hot-Rod laser encoder chip. Data may be clocked out of the chip faster using an external circuit

(see section 3.2.12). The rate is limited only by the external hardware (in practice probably 20nS per word).

3.2.8 Overflow Conditions

The digitizer contains three FIFO buffers (the two primary FIFOs corresponding to two clock phases, and the secondary FIFO). Each of the three may report an overflow condition, if no free location is available for incoming data. Three overflow bits are used to flag this. Each of the two data fields in the secondary FIFO has an overflow bit, which is set if the primary fifo overflowed, and another overflow bit is added in the secondary FIFO if it overflows.

3.2.9 Output Encoding

The output of the **Secondary FIFO** is 34 bits (two 17-bit data words). Six bits are added to form a 40 bit output word (the Gazelle Hot-Rod chip expects 40 bit words). One extra bit flags a "null" word (see below). Four parity bits are added, one for each 9 bits in the data. An overflow bit completes the 40 bits.

3.2.10 Null Words

A **Null word** is inserted in the output data every 81.92uS ($80nS \times 1024$). This may be used in DUMAND by on-shore circuitry which measures and corrects for clock drift. **Null words** bypass the FIFOs, so null word transmission is exactly synchronized with both the 1024 nS digitizer clock rollover and the 80 nS hot-rod word rate. **Null words** may be disabled by a LOW level on the ENNL input pin.

8 bits of control data (from the SC computer in DUMAND) may be inserted in **Null words**. The input pins SCD0..SCD7 accept the input data. SCDV is an additional input which should be set to '1' when valid data is present. An 80 nS wide read pulse is output on SCRD when the data is read, and the external circuit should hold it's data stable until the end (falling edge) of SCRD.

3.2.11 Output Word Format

The 40-bit output words are formatted as follows:

Data Words

bit numbers	*description*
0–16	first data field
17–33	second data field
34	second FIFO overflow flag
35	null/data flag (zero for data)
36	parity for bits 0, 4, 8...
37	parity for bits 1, 5, 9...
38	parity for bits 2, 6, 10...
39	parity for bits 3, 7, 11...

Data Fields

bit numbers	*description*
0–4	channel number
5–14	clock
15	UP/DOWN
16	primary FIFO overflow

Null Words

bit numbers	*description*
0–8	zeroes
9–16	SC data *(changed)*
17	SC data valid flag
18–34	not used (zero)
35	1 (flags null word)
36	parity for bits 0, 4, 8...
37	parity for bits 1, 5, 9...
38	parity for bits 2, 6, 10...
39	parity for bits 3, 7, 11...

3.2.12 Output Handshaking

The output handshaking is designed to interface directly to the Hot-Rod serial transmitter. Normally, one word is output every 80 nS. Control signals for the Hot-Rod transmitter are provided. REFCLK is a 25 MHz reference clock output to the Hot-Rod transmitter. 1XCLK is a 12.5 MHz word clock returned by the Hot-Rod. This is NANDed with an internal transmit strobe

to produce STRB, which is the transmit strobe output to the Hot-Rod. The Hot-Rod is forced to transmit a SYNC word every 81.92 μS by omitting a STRB pulse.

If a Hot Rod is not being used, The REFCLK output may be ignored and data clocked out of the chip by applying pulses or a symmetrical clock to the 1XCLK input. The rising edge (of 1XCLK) is synchronised with internal clock to produce an internal DUMP signal for reading the FIFO. If the data is valid, the inverted 1XCLK will appear on the STRB output. If the data is invalid, STRB does not rise on the falling edge of 1XCLK. Rising STRB on falling edge of CLK tells that the current data is valid.

3.3 *in situ* Testing

Four test inputs (TSTMOD, TSTDAT, TSTCLK, TSTOE) allow for limited testing of the installed digitizer. A 27-bit test pattern may be serially loaded into a shift register, and asserted on the 27 data inputs. The digitizer will respond in the usual way to the test inputs. In addition, the hot-rod output data transmission may be disabled, to allow the internal FIFOs to be completely filled for test purposes.

Each new 27-bit test pattern is asserted simultaneously on all 27 digitizer inputs. When TSTMOD is asserted, an internal counter is reset to zero. The counter increments once for each TSTCLK pulse, and when the count reaches 27, the data from the test shift register is asserted on the digitizer inputs. Another test word may be loaded by clocking in 27 more bits.

Each of the test pins and their function is described below:

- TSTMOD - A LOW level enables normal operation. A HIGH level enables test mode, where data may be clocked into the test shift register on the TSTDAT input.
- TSTDAT - Serial input for test data.
- TSTCLK - Serial input clock. The internal shift register advances to the next bit on a rising edge on this input.
- TSTOD - Test output disable. A HIGH level disables the transmission data off-chip. Note that NULL words are still transmitted, if the ENNL input is active (HIGH).

3.4 Initialization

The digitizer chip must be initialized at power-up by the following sequence on the INI0 and INI1 pins:

- INI0 and INI1 both high for $\geq 1\mu$S.
- INI0 low for $\geq 20nS$.
- INI0 and INI1 both low – normal operation.