DUMAND String Controller Digitizer System Design Specification

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Abstract

This specification describes the design of the DUMAND String Controller digitizer system. It includes (or will include) mechanical and electrical descriptions of the clock module, digitizer board, ASIC and other associated information. ***Last updated on 1/30/92 after DUMAND collaboration meeting at Hawaii***

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1 SC Digitizer System

The DUMAND SC digitizer system receives signals from 24 Optical Modules (OMs) and up to 3 Calibration Modules (CMs) and measures the arrival time of pulses to 1nS precision. The time is transmitted to shore over an optical fiber. The digitzer system is composed of two modules, the clock generator and the digitizer PCB. In addition, the digitizer is connected to the SC computer system.

Figure 1 shows the logical interconnection of the SC digitizer system.

Table 1 lists the signals shown in Figure 1 and gives a description of each. See Section 3.10 for detailed information on the connectors on the SC PC board.

Count	Name	Type	From	To	Description
1	CKALIVE	TTL(OI)	Clock	SCC	Clock heartbeat
16	CKDATA	TTL(OI)	SCC	Clock	data for clock DACs
1	CKFREQ/	TTL(OI)	SCC	Clock	strobe to set clock frequency
1	CKPHASE/	TTL(OI)	SCC	Clock	strobe to set clock phase
1	CKP0	SMA Coax	Clock	Dig	500MHz clock phase zero
1	CKP1	SMA Coax	Clock	Dig	500MHz clock phase one
8	DCD0..DCD7	TTL(OI)	SCC	Dig	Digitizer control data
1	DCA0..DCA6	TTL(OI)	SCC	Dig	address
1	DCWR	TTL(OI)	SCC	Dig	write strobe
1	DCRD	TTL(OI)	SCC	Dig	read strobe
1	HPCLK	TTL(OI)	Dig	SCC	1Mhz clock for hydrophone data
10	HPDATA	TTL(OI)	SCC	Dig	hydrophone data
1	SCCTX	TTL(OI)	SCC	Dig	serial C&C data to shore
1	SCCCK	TTL(OI)	SCC	Dig	serial 16X transmit clock
1	SCCRX	TTL(OI)	Dig	SCC	serial C&C data from shore

Table 1: SC Inter-Board Signal List

2 Clock Signal Generator Module (CSG)

This module is a self-contained unit which generates a two-phase 500 MHz clock for the digitizer. It consists of a single PCB, with a commercial 500 MHz crystal oscillator module[1], a phase splitter and voltage regulators. The module is electrically shielded, and all signals (except power supplies and 500 MHz outputs) are optically-isolated.

The oscillator output is split into complimentary (2-phase) clocks by a GigaBit Logic 10G010 clock fanout buffer chip. On the prototype, the relative alignment of the two clock phases is adjustable by means of a DAC. Depending on prototype test results, this DAC may be removed in the production module.

The Vectron oscillator is specified to be initially within $\pm$10ppm of 500MHz at 25°C, with a $\pm$0.2ppm/°C temperature coefficient. It ages up to $\pm$5ppm the first year, and $\pm$3ppm per year thereafer. Over a 10-year deployment period, this adds up to as much as $\pm$50ppm. Thus, we may need frequency adjustment. On the prototype, the oscillator frequency may be adjusted over a $\pm$100ppm range by means of a $\pm$5V control voltage, supplied by a monolithic DAC on the PCB. One LSB of the DAC corresponds to a frequency change of $\pm$0.4ppm.

Because of the $\pm$0.2ppm/°C temperature coefficient of the oscillator, the operating temperature of the module must be kept relatively constant. The production clock module should be designed to provide good coupling between the oscillator and the housing, and a separate heatsink should be provided for the module.

The CSG provides a "heartbeat" output at about 2Hz to indicate that it is operating properly. This output may be connected to an LED for bench testing, and may be monitored by the SC computer.

[1] a Vectron Labs CO275HGB35N was used in the prototype

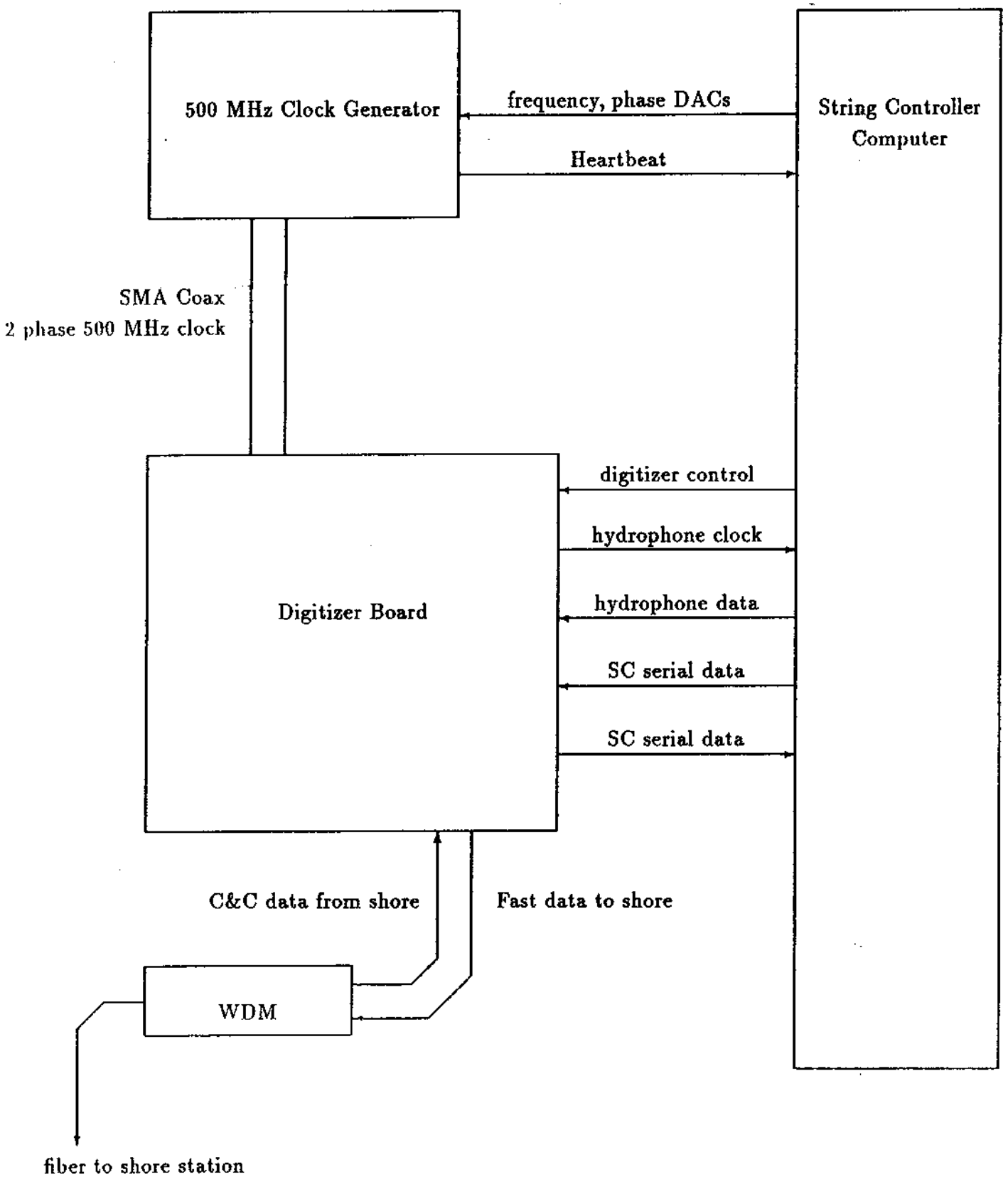

Figure 1: SC Digitizer Interconnections

The prototype clock module derives all it's power from external ±24VDC supplies with on-board voltage regulators. We anticipate the same scheme in the production module.

3 SC Digitizer PCB

The SC Digitizer PCB will be 24[2] inches long and 6.5 inches wide. Figure 2 shows the PC board dimensions. A spring-loaded side rail type heat sink will cover the middle 18 inches of the board. The board will be multilayer, and contain surface mount components.

Figure 4 shows an electrical block diagram of the board, while Figure 3 shows a mechanical detail of the central portion of the board, which contains the ASIC and digitizer electronics. A block-by-block description of each functional block on the PCB follows.

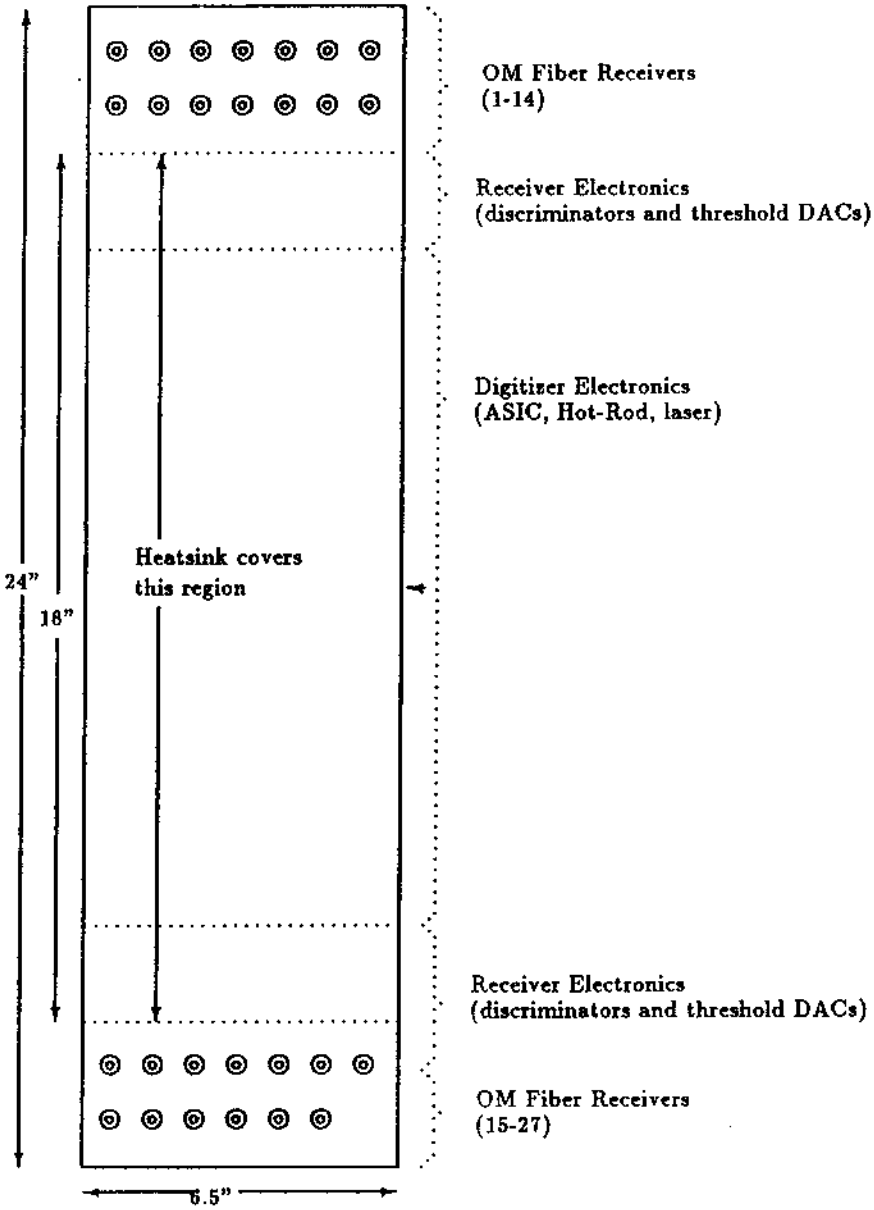

Figure 2: SC Digitizer PC Board

[2]may be reduced to 22 inches for ease of fabrication

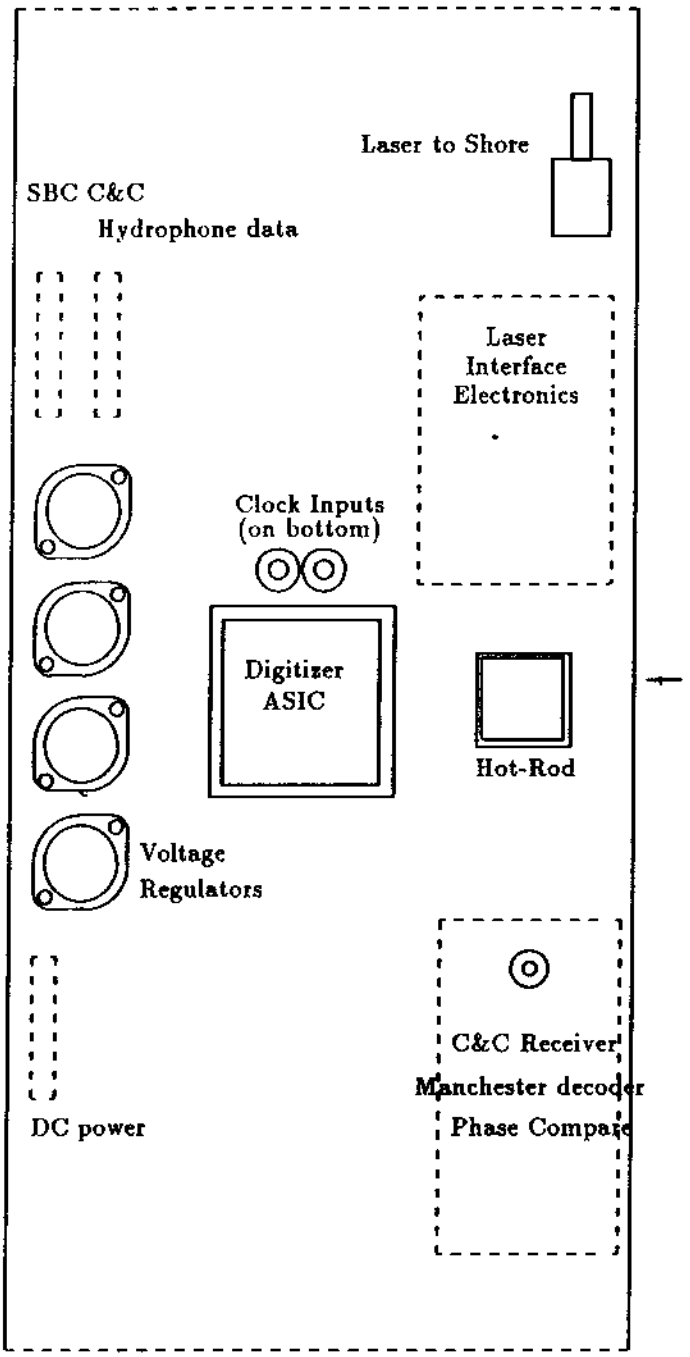

Figure 3: SC Digitizer PC Board, central region

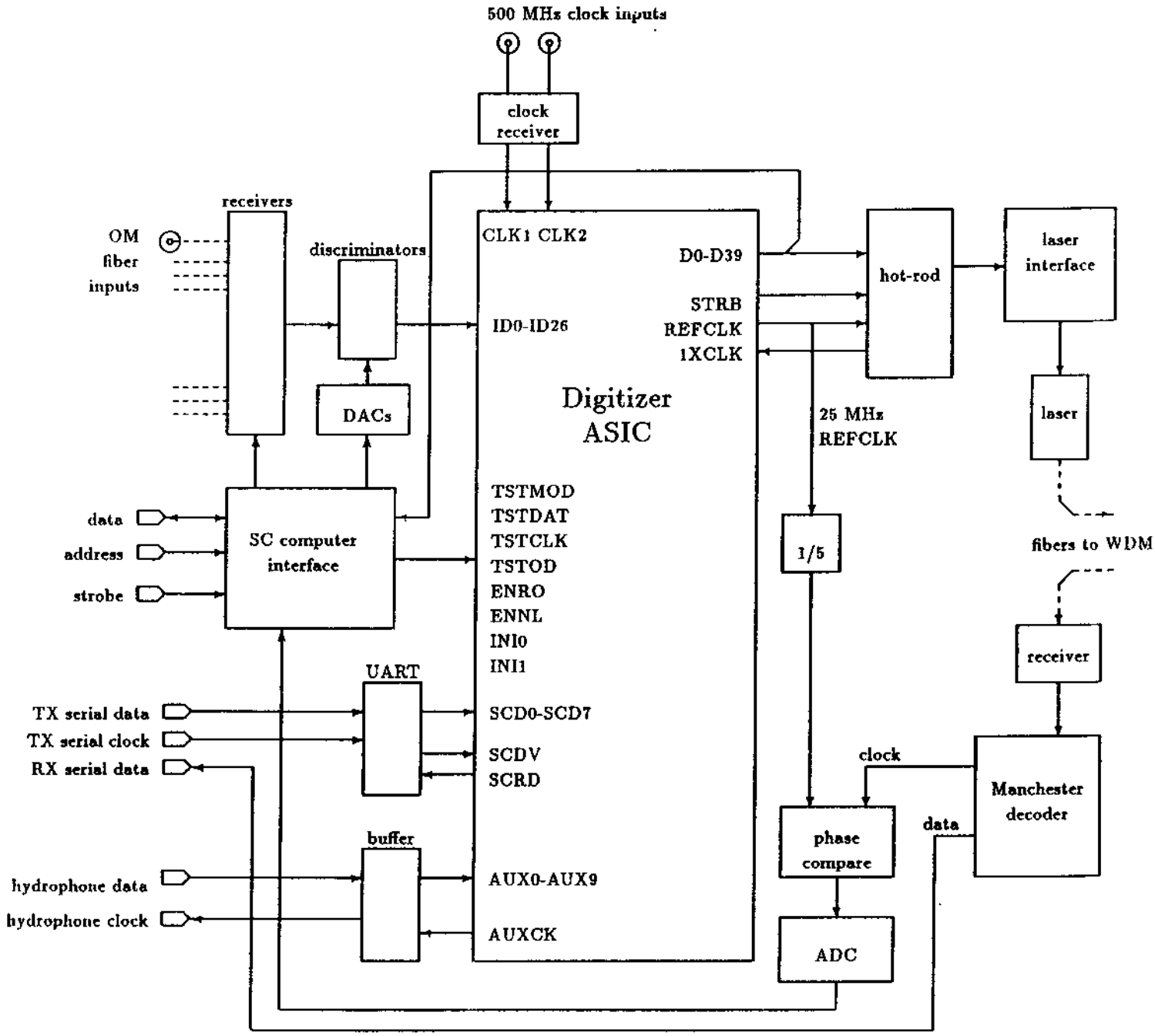

Figure 4: SC Digitizer PC Board Block Diagram

3.1 Power Supplies.

Most voltages will be regulated off-board with DC-DC converters. Optional power-conditioning modules will be used for analog power to reduce switching ripple. Remote-sense lines from the DC-DC converters will be connected near the load point on the digitizer PCB. Table 2 lists power supply requirements.

Block		-12V	-5.2V	-2.0V	+3.3V	+5.0V	+12V
ASIC				≈7.5A	yes		
Hot-Rod						350mA	
OM inputs							
	receivers	?	?	?	?	?	?
	discriminators		1.0A			700mA	
	DACs	?	?	?	?	?	?
Output to shore							
	Laser	?	?	?	?	?	?
	Driver ckt	?	?	?	?	?	?
C & C input							
	receiver	?	?	?	?	?	?
	decoder ckt	?	?	?	?	?	?

Table 2: SC Board Power Requirements

3.2 Optical Recievers.

27 Hewlett-Packard optical receivers sense signals from the OMs and CMs, with outputs fed to MAX9685 discriminators. Thresholds will be set with 4 octal DACs. Latch enable inputs on discriminators will be used to disable malfunctioning channels.

3.3 Digitizer ASIC.

The digitizer is a Vitesse VGFX100K GaAs gate array customized as described elsewhere[?]. It is packaged in a 211 pin PGA, which can be socketed on prototype boards. Inputs to the chip are: power, 500 MHz clock, ECL signals from OM discriminators, Hydrophone data and control signals from the SC computer. The chip ouput drives the Hot-Rod laser serializer chip directly.

3.4 SC computer interface.

Several registers are accessible from the SC computer by means of a simple bus, with address lines, data lines, and two strobes. The bus uses 7 address lines, so the registers would normally occupy 128 locations in the SC computer address space. The data lines are bi-directional. Table 3 lists the functions and their addresses. A detailed description of each register follows.

OM Reciever Threshold DACs. Each address controls the threshold for one OM optical receiver input. The threshold is adjustable over a range of ??V (DAC setting 0) through ??V (DAC setting 255 decimal). At DAC setting 0, the discriminator should always be 'on', and at DAC setting 255 it should always be 'off'.

Fast data spy port. This allows the SC computer to read, on-the-fly, a subset of bits from the most recent pair fast data words. The bits are shown in the table below.

Addresses (HEX)	*no. bits*	*direction*	*Function*
$00–$1A	8	WR	OM receiver threshold DACs
$20	8	RD	Spy port LSB
$28	8	RD	Spy port MSB
$30	8	RD	clock phase ADC data
$38	1	RD	clock phase error sign bit
$40–$5A	1	WR	OM receiver enable
			ASIC control functions
$60	1	WR	(TSTMOD) enable test mode
$61	1	WR	(TSTDAT) test data
$62	1	WR	(TSTCLK) test clock
$63	1	WR	(TSTOD) FIFO output disable
$64	1	WR	(ENRO) enable roll-over words
$65	1	WR	(ENNL) enable null words
$66	1	WR	(INI0) initialization
$67	1	WR	(INI1) initialization

Table 3: SC digitizer control functions

bits	*description*
LSB	
0–4	channel number 1
5	up/down flag 1
6	primary FIFO overflow 1
7	NULL word flag
MSB	
0–4	channel number 2
5	up/down flag 2
6	primary FIFO overflow 2
7	secondary FIFO overflow

Table 4: Fast data spy port bit assignments

Clock phase ADC. This is an 8-bit ADC which measures the phase difference between the shore-station 5MHz clock sent down the fiber, and a local reference clock output by the digitizer. Reading from address $30 (Hex) retrieves the ADC data, and initiates a new ADC conversion. The exact mapping between phase and ADC value is not defined at this time.

OM receiver disable. Each of the 27 OM input receivers may be independently enabled or disabled. A single address controls each receiver. The receivers power up in a '0' (enabled) state; writing a '1' will disable a receiver.

ASIC control. Several bits control the digitizer ASIC operation. Note that all bits are reset to '0' at power-up.

- Digitizer testing: Writing '1' to TSTMOD enables test mode, where data from a 27-bit shift register replaces the normal OM input data. One bit is loaded from TSTDAT into a 27-bit shift register on each rising edge of TSTCLK. Every 27 clock cycles the contents of this shift register is asserted on the OM inputs. A '1' in the shift register corresponds to an active (on) OM input.
- ASIC initialization (INI0, INI1). Two signals are required to initialize the ASIC after power-up. Both signals must be set to '1', then INI0 set to '0', then both set to '0' for normal operation.
- Output FIFO Data Enable (TSTOD). This bit controls the loading of data words out of the chip into the Hot-Rod chip. Writing a '1' disables data output to allow the on-chip FIFO buffers to fill. Note that this bit *does* disable roll-over words along with the data words, but *does not* affect null words (see ENNL).
- Roll-Over Disable ($\overline{\text{ENRO}}$). The digitizer normally emits "Roll-Over" words every 1 μS containing Hydrophone data. These may be disabled by setting this bit. Data words and null words are not affected.
- Null word disable ($\overline{\text{ENNL}}$). The digitizer normally emits "Null" words every 81.92 μS. These may be disabled by setting this bit.

3.5 Hot-Rod.

The data from the digitizer is encoded and serialized by a Gazelle Hot-Rod chip. The Hot-Rod requires a 25MHz clock, which is provided by the digitizer. The output of the Hot-Rod is a 625MBaud serial data stream, which drives a laser, transmitting the data to the shore station via an optical fiber at 1550 nm.

3.6 Laser and Interface Circuit.

The laser[3] is biased by a small discrete analog circuit contained on the PCB.

3.7 C&C Fiber Receiver, Decoder, Phase Comparator

Command and control data to the SC computer is received from the shore station on the same fiber at 1300 nm. The data is manchester encoded with a 5 MHz clock rate. The 5 MHz clock is recovered, and phase compared with a 5 MHz clock derived from the Hot-Rod reference clock from the digitizer. The phase measurement is digitized locally with an 8-bit ADC. This phase measurement in principle allows the digitizer clock to be synchronized with the shore station clock.

The recovered serial data is sent to the SC computer.

3.8 SC Serial Data Interface

The SC computer transmits serial data to the shore station at 9600 baud. This data is converted to 8-bit parallel words, and inserted in the fast data stream by the digitizer ASIC. The SC PC board contains a UART to accomplish the serial-to-parallel conversion. The UART parallel output is interfaced directly to the digitizer ASIC.

[3] ??? mfgr, type

pair no.	*name*	*description*
1	D0	bidirectional data bus LSB
2	D1	.
3	D2	.
4	D3	.
5	D4	
6	D5	
7	D6	
8	D7	bidirectional data bus MSB
9	A0	address bus LSB
10	A1	.
11	A2	.
12	A3	.
13	A4	
14	A5	
15	A6	address bus MSB
16	$\overline{\text{RD}}$	write data strobe
17	$\overline{\text{WR}}$	read data strobe

Table 5: J1 - SC computer interface connector

pair no.	*name*	*description*
1	D0	hydrophone data input LSB
2	D1	.
3	D2	.
4	D3	.
5	D4	
6	D5	
7	D6	
8	D7	
9	D8	
10	D9	hydrophone data input MSB
11	CLK	hydrophone clock output

Table 6: J2 - Hydrophone interface connector

3.9 Hydrophone Input

Hydrophone data is multiplexed onto the same fiber as the fast data. This multiplexing is performed by the digitizer ASIC, by inserting hydrophone data into the 10 otherwise unused "time" bits in roll-over words. These roll-over words are transmitted every 1.024 μS.

10 TTL data inputs are provided for Hydrophone data. In addition, a clock pulse ??? nS wide is output to signal that the data has been read.

3.10 Connector Pinouts

The digitizer PCB has many connections to other parts of the SC system. These are listed here. All connectors except J3 (power) and J4 (clock) will carry differential signals, conforming to the RS-422 specification. J1 and J2 will be standard locking ribbon cable headers.

conductor no.	*name*	*description*
1	-12V	analog power
2	-12V_GND	analog power return
3	-5V	analog power
4	-5V_GND	analog power return
5	+5V	analog power
6	+5V_GND	analog power return
7	+12V	analog power
8	+12V_GND	analog power return
9	GROUND	shield
10	GROUND	shield
11	-2V	digital power
12	-2V_GND	digital power return
13	+5V	digital power (also regulated to +3.3V)
14	+5V_GND	digtal power return

Table 7: J3 - DC power connector

pin	*name*	*description*
1	CLK1	500MHz clock phase 1
2	CLK2	500MHz clock phase 2
shield	GROUND	signal ground (ref to clock module)

Table 8: J4 - Clock input connector (twinax or two SMAs)

pin no.	*name*	*description*
1	SCCRX	C&C data from shore
2	SCCTX	C&C data to shore
3	SCCCK	16X transmit clock

Table 9: J5 - Serial data I/O to SC computer