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The DUMAND II Digitizer

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1. Abstract

A monolithic multi-hit digital TDC (time-to-digital converter) has been developed for the DUMAND II experiment. It has a pipelined archetecture, 27 channels and 1ns least count. An overview of the performance requirements and implementation in a GaAs gate array is described here.

2. Introduction

A deep-ocean laboratory for the study of neutrino astrophysics and particle physics is under construction. Phase II of the Deep Underwater Muon and Neutrino Detection (DUMAND) experiment is scheduled for initial deployment during the summer of 1993. The experiment detects Cherenkov radiation from high energy muons, and hadronic and electromagnetic cascades, using a volume array of photomultiplier tubes (PMTs) buoyed off the ocean bottom. Event energies and muon trajectories are reconstructed using timing and pulse-height information from the PMTs. To achieve angular resolution of one degree, timing accuracy of one nanosecond is required.

The array will consist of 216 optical modules (OMs), arranged in 9 strings of 24 modules each. Each OM contains a 40 cm hemispherical PMT, housed in a 1.5 cm thick pressure-tolerant glass sphere. An electronics package within the sphere provides readout of time, pulse charge, and operational status. Fast PMT pulse information is provided on a multi-mode digital optical fiber output, with the output pulse width proportional to the PMT pulse charge. Data from 24 PMTs is collected in the string controller (SC) where it is digitized, multiplexed, and transmitted to shore on single-mode fibers at 500 Mbps.

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Digitization and multiplexing are performed by a single monolithic custom digitizer integrated circuit (IC) which is described here.

3. Requirements

The basic requirements for the DUMAND II digitizer are:

No. of channels	27 (24 PMT, 2 calibration, 1 timing)
Time resolution	1ns least count
Readout	continuous, deadtime-less, time-ordered
Buffering	≥48 pulses (two per PMT)
Data rate to shore station	100kHz per PMT maximum
Reliability	mean time between failures ≥10 yr.

The reliability and speed requirements made a monolithic digitizer an obvious choice. The requirement of continuous operation eliminated conventional ramp-type TDCs. We studied several all-digital solutions involving various combinations of custom and off-the-shelf ICs, and finally decided to attempt an implementation based on a single large IC, containing the entire digitizer, multiplexer and memory. We estimated that the IC would require about 60,000 two-input equivalent gates, consistent with available application-specific IC (ASIC) technology.

4. Technology

We studied several digital IC fabrication techniques: full-custom, standard cell and gate arrays[1]. In a full-custom design, an experienced IC design team is required, as all details of the layout must be specified to the manufacturer. This option is quite expensive. A standard-cell design is built from complex pre-tested circuit elements, too expensive and not appropriate to our design. A gate-array design is built of pre-placed transistors configured for easy use as logic gates. The designer is provided with a library of "macros", pre-configured simple logic elements such as ANDs, ORs and flip-flops. The gate array is relatively inexpensive, as only the metal interconnection layers are custom. We found this to be a good fit to our design.

We considered CMOS, ECL (emitter coupled-logic) and GaAs IC technologies. CMOS is too slow unless one resorts to complex multi-phase clocking schemes, although it has been used in a successful commercial digitizer, the LeCroy MTD132. ECL and GaAs both met our speed requirements. The substantially higher power consumption of ECL led us to opt for a GaAs device. One manufacturer, Vitesse Semiconductor, provides DCFL (direct-coupled FET logic) gate arrays with high speed, modest power requirements and the required size. After much research, we chose the Vitesse VGFX200K DCFL gate array[2].

5. Design

The digitizer processes 26 PMT signals in parallel and packages the information in compressed form for transmission to shore. The one nanosecond least-count would suggest a 1GHz clock, but this is impractical with today's IC technology for several reasons. Currently available large IC packages attenuate high-frequency signals excessively. Even using GaAs, the propagation delay between logic levels is excessive for a 1ns clock period in a complex design. Also, distributing a 1GHz clock over a large IC introduces significant uncertainty in clock timing across the device. This phenomenon has been studied extensively by M. Jenko of our group and presented elsewhere[3]. Thus we selected a two-phase approach. The master clock runs at 500 MHz, and both edges are used. This significantly increases the complexity of the total circuit, as the rising and falling edges are handled in parallel. Additional circuitry ensures the preservation of event chronology, so that the data arrive at the shore in time order. Figure 1 shows the essential blocks of the digitizer chip.

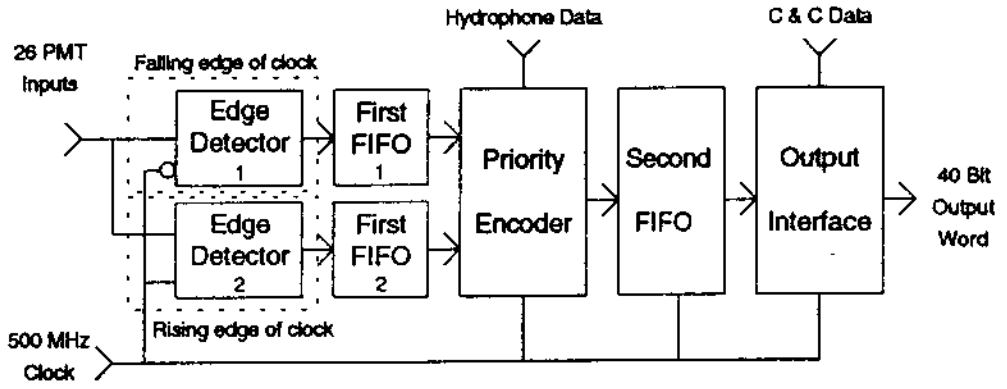

Figure 1. – Digitizer ASIC Block Diagram

Edge Detector. This block assigns the asynchronous signals coming from the optical modules to discrete time bins. The edge detector also provides zero-suppression by triggering the circuit only when a transition occurs on an input. Both rising and falling edges are recognized, using separate circuits.

Time Stamp (not shown). A ten bit time stamp is recorded for each clock nanosecond containing valid data. The ten-bit time will roll over every 1,024 ns, and a special word is inserted in the data stream when this occurs. This allows the trigger processor on shore to accurately reconstruct event timing.

Hydrophone Inputs. The roll-over words mentioned above are used to transmit auxiliary data to the shore station, including hydrophone data for sonar location of optical module positions.

First FIFO. This block provides buffering for bursts of input data. The priority encoder services one channel per 2 ns clock cycle, which implies a need for queuing if transitions arrive in bursts. For the expected time distribution of input data, ten words in front of the priority encoder are sufficient. Two separate FIFOs store data recorded on rising and falling clock edges.

Priority Encoder. This block identifies those channels where a transition took place. If there is more than one transition within the same nanosecond, the priority encoder emits a separate word for each transition, in order from low to high channel numbers. Since this is a true priority encoder, no scanning of empty bit locations is required, and each transition requires only 2ns to encode.

Second FIFO. The priority encoder generates data in bursts, but the bandwidth of the communication channel to shore need only suffice for the average speed of data generation if there is sufficient buffering in front of it. Simulation with *Monte Carlo* event data showed that a 100-word buffer was sufficient.

Output Interface. The digitized data are transmitted by optical fiber to shore at 500 mega-bits/second, using a commercial GaAs transmitter-receiver chipset called the Hot-Rod[3]. The output interface delivers data to the Hot-Rod in the format it expects (one 40-bit word every 80 ns). Each PMT input transition (rising or falling edge) generates a 16-bit word in the data stream, with five bits for the channel number, ten bits for the time, and a single bit to indicate the direction of the transition. Two transitions are packed into a 40-bit output word, the remainder of the word (8 bits) is occupied by error flags. The data format is as follows:

6. Implementation

A complete model of the design was constructed in software and simulated on a SUN workstation for functional correctness using DUMAND II *Monte Carlo* simulation data. The lengths of the FIFO buffers were optimized through these simulations. Simulated events were chosen which resulted in worst-case data streams for digitizer queuing; that is, events where large numbers of PMT pulses arrive simultaneously at the digitizer.

The detailed logic design was developed on a Mentor Graphic CAE system, and verified for correct operation and correct timing using Mentor's Quicksim™ logic simulator. Vitesse provided a family of macros which were compatible with the Mentor system. The final design was quite complex (200,000

transistors or about 66,000 2-input equivalent gates), and required many hours of CPU time on an Apollo DN5500 workstation for a simulation run. The final task in the ASIC design was to design a set of test vectors to verify that the fabricated devices operate correctly.

An eight layer PC board was designed to house the ASIC and associated circuitry. The design was quite complex due to the high frequencies involved. A block diagram of the PC board is shown in Figure 2. The PMT signals enter the board on optical fibers from the OMs, and are converted to electrical signals by optical receivers. The signals are then carried to the ASIC on impedance-controlled microstrips. The digitized data is then serialized by the Hot-Rod transmitter and sent to shore. The board also contains an interface to the SC computer, which allows various diagnostic and control functions to be activated from the shore station. The OM receivers may be individually adjusted to compensate for changes in fiber attenuation, or to keep signals from malfunctioning PMTs from overloading the system. Self-test features on the ASIC itself may be activated for remote debugging.

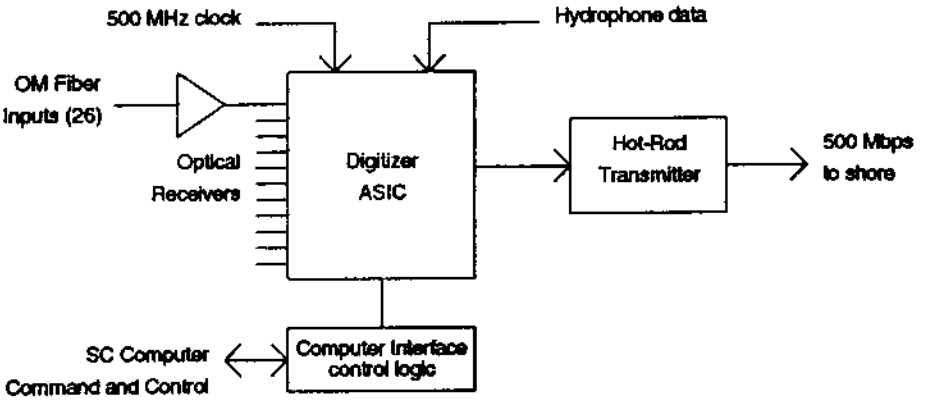

Figure 2. – Digitizer PC Board Block Diagram

7. Testing

Four prototype ASICs were delivered in Jan. 1993. Preliminary testing has shown correct operation at 500MHz. A microprocessor-controlled test setup was designed, as shown in Figure 3. A set of test patterns is loaded into a 26-bit by 8K word memory on the test board. On command the test data is clocked out to 26 optical transmitters to simulate PMT data, and carried to the digitizer board on 26 optical fibers. The output data stream is received by a Hot-Rod receiver, collected in another buffer on the test board, and then transmitted to an IBM-PC for analysis. We will continue with an extensive testing and burn-in program.

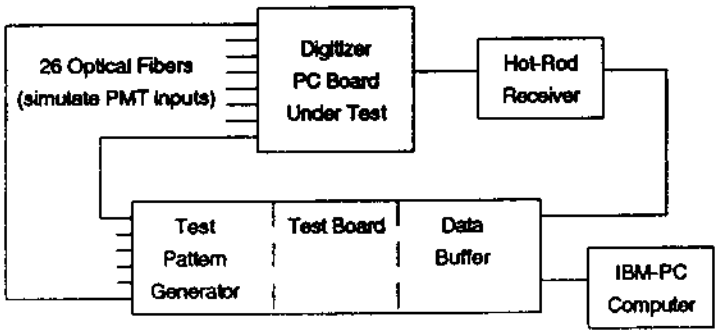

Figure 3. - Test System Block Diagram

8. Summary

A new multi-channel digital TDC has been developed for the DUMAND II experiment, and in the process it has been shown that the development of large GaAs gate arrays is within the capabilities of a well-equipped university facility. The completed ASIC (1.4 x 0.8 cm) has perhaps the largest (speed x area) product of any currently in production. It is hoped this device and experience will prove useful to others.

Acknowledgements

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