

Development of the Orthogonal-Transfer Array[†]

Barry E. Burke^{*a}, John L. Tonry^b, Michael J. Cooper^a, Douglas J. Young^a, Andrew H. Loomis^a,
Peter M. Onaka^b, and Gerard A. Luppino^b

^aMIT Lincoln Laboratory, 244 Wood Street, Lexington, MA 02420;

^bInstitute for Astronomy, U. of Hawaii, 2680 Woodlawn Drive, Honolulu Hawaii'i 96822

ABSTRACT

The orthogonal-transfer array (OTA) is a new charge-coupled device (CCD) concept for wide-field imaging in ground-based astronomy based on the orthogonal-transfer CCD (OTCCD). This device combines an 8×8 array of small OTCCDs, each about 600×600 pixels with on-chip logic to provide independent control and readout of each CCD. The device provides spatially varying electronic tip-tilt correction for wavefront aberrations, as well as compensation for telescope shake. Tests of prototype devices have verified correct functioning of the control logic and demonstrated good CCD charge-transfer efficiency and high quantum efficiency. Independent biasing of the substrate down to -40 V has enabled fully depleted operation of 75- μ m-thick devices with good charge PSF. Spurious charge or “glow” due to impact ionization from high fields at the drains of some of the NMOS logic FETs has been observed, and reprocessing of some devices from the first lot has resolved this issue. Read noise levels have been 10 – 20 e⁻, higher than our goal of 5 e⁻, but we have identified the likely sources of the problem. A second design is currently in fabrication and uses a 10- μ m pixel design resulting in a 22.6-Mpixel device measuring 50×50 mm. These devices will be deployed in the U. of Hawaii Pan-STARRS focal plane, which will comprise 60 OTAs with a total of nearly 1.4 Gpixels.

Keywords: orthogonal transfer array, OTA, OTCCD, Pan-STARRS, focal-plane array

1. INTRODUCTION

The concept of the OTA was introduced a few years ago to address the need for a large imager that combined rapid readout (few seconds) with orthogonal-transfer CCD technology for wide field-of-view (FOV) sky surveys.¹ Out of this work a program called Pan-STARRS (Panoramic Survey Telescope and Rapid Response System) was begun to develop the OTA technology and build a set of four telescopes, each with a gigapixel focal-plane array of 60 OTAs.² An initial description of the OTA design and its packaging have been reported previously.³ This paper is an update on the device development and describes test data from the first lot of wafers.

The main features of this device are reviewed in Figure 1. The OTA comprises a two-dimensional array (8×8 for the current version of the device) of cells, each cell in turn consisting an OTCCD of roughly 500-600 pixels on a side. The right side of Figure 1 illustrates the two pixel layouts that can be used in the OTCCD, identifying the four phases which control the horizontal and vertical shifting of charge. These pixel designs are referred to as type 1 (upper drawing in Figure 1) and type 2 (lower). In the OTA these phases are under the control of a small logic block which is addressed and loaded with control bits from off chip. This feature is essential in enabling independent shifting of the image-charge field in response to the random image motion, both temporal and spatial, in astronomical images. The logic also controls the multiplexing of the video out of each cell onto a column video bus shared by all cells in a given column.

This architecture addresses a number of shortcomings in current scientific imager technology as well as introducing new capabilities to the astronomy community. One of the major problems with conventional CCD imagers is long read times, an issue that has to be addressed for rapid sky surveys. This device is read out one row of cells at a time through

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* bburke@ll.mit.edu

eight video channels. The output amplifier of each cell is a wideband, two-stage amplifier capable of output rates of 1.0 MHz or more. We expect read times of <5 s, a time that is small compared to the expected integration time of 30 – 60s in Pan-STARRS. Another virtue of this device is reduced vulnerability to fatal defects, since such defects, if located within cells, can be isolated from the remainder of the device by the logic.

A unique and important feature of the OTA is the use of OTCCD technology to provide electronic tip-tilt corrections for enhanced SNR and image resolution. This device, through the use of individually controlled cells, can be used to measure the image deflection field over the sensor FOV and perform spatially varying adaptive imaging.

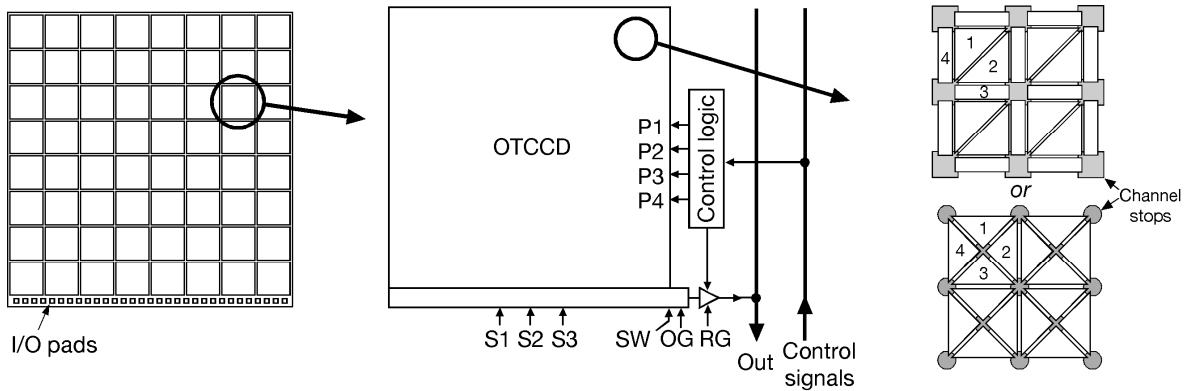


Figure 1. Principal elements of the OTA. Left: the overall chip layout comprising an 8x8 array of OTCCD cells; center: the OTA cell with its control logic; right: two OTCCD pixel geometries used in the prototype designs (upper is type 1, lower is type 2).

The first prototype lot was completed mid-2004, and used high-resistivity, 150-mm float-zone wafers for maximum depletion depth. Figure 2 shows a wafer photograph on the left and a packaged device (front-illuminated to show the cell array) on the right. The OTCCD fabrication requires four levels of polysilicon, and the extensive network of control lines for this device necessitated two levels of metallization. Because of the novel nature of this device and the compressed schedule for device deliveries, a large number of design and process splits were incorporated in lot 1 in order to have the widest choice of successful features to incorporate in the subsequent lots for the first Pan-STARRS Gpixel focal plane. The four OTAs in Figure 2 represents the matrix of two pixel sizes (10 and 12 μm) and the two OTCCD pixel styles shown in Figure 1. In addition, small 2x2 mini-OTAs (MOTAs) contained various experiments of interest for future designs.

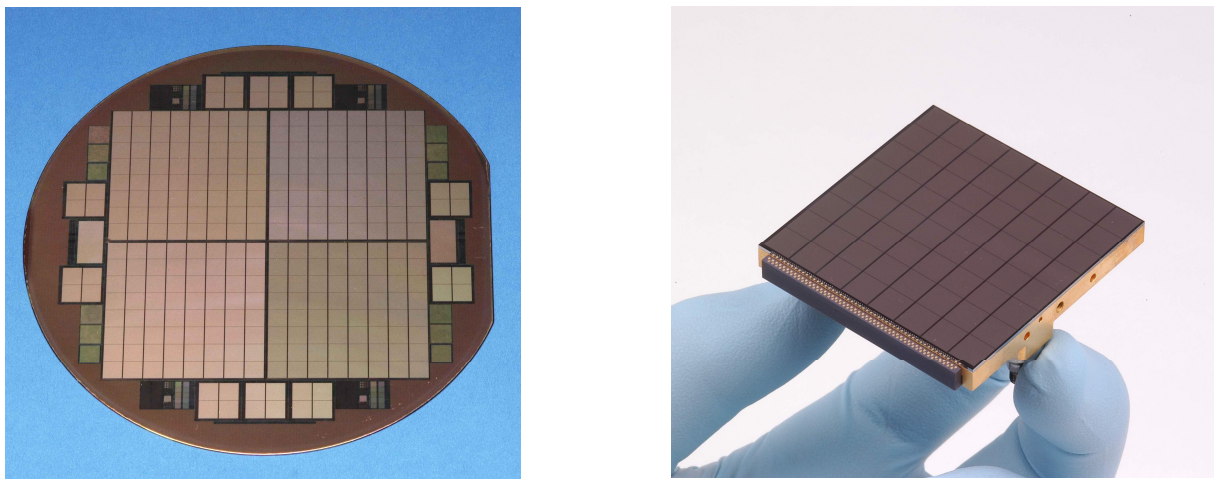


Figure 2. Left: 150-mm wafer with four 50x50-mm OTAs and ten smaller mini-OTAs (MOTAs), each with a 2x2 array of cells. Right: photograph of a packaged OTA.

In the next section we review some of the test results of the lot-1 devices, some of which have been reported at a recent workshop.⁴

2. RESULTS FROM LOT-1 DEVICES

2.1 First images

Devices from the first lot performed all the basic functions expected, and examples of imagery are shown in Figure 3. On the left is an image from a front-illuminated device under wafer probe demonstrating the 2D shifting capability. A fixed light spot was focused onto a small group of pixels, while the CCD clocks were shifted to “paint” the image onto the cell. The device was at room temperature so that the dark-current accumulation was noticeable. Overflow drains on three sides of the cell and the serial register on the fourth provide a sink for charge that is shifted beyond the boundaries of the pixel array. This prevents an undesirable charge pileup in the outermost pixels. The various gray shades in the background reflect the differing integration times for charge packets in the center versus those around the perimeter, which dumped their charge for part of the integration time during the shifting. The image on the right was taken on a back-illuminated device at $T=-70^{\circ}\text{C}$ with monochromatic illumination ($\lambda=500\text{ nm}$).

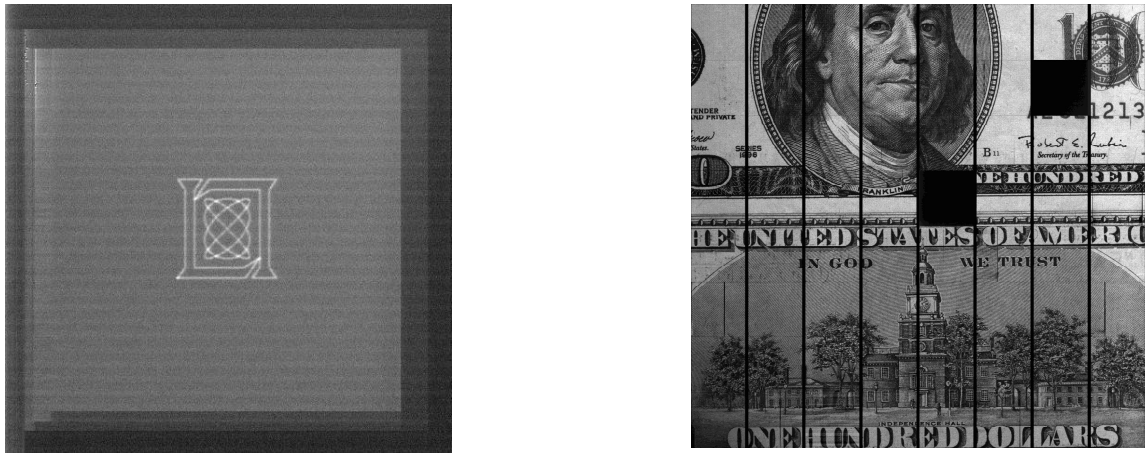


Figure 3. Left: image from a single OTA cell obtained by focusing a light spot on the device and programming a shift pattern into the parallel clocks. Right: image from an OTA.

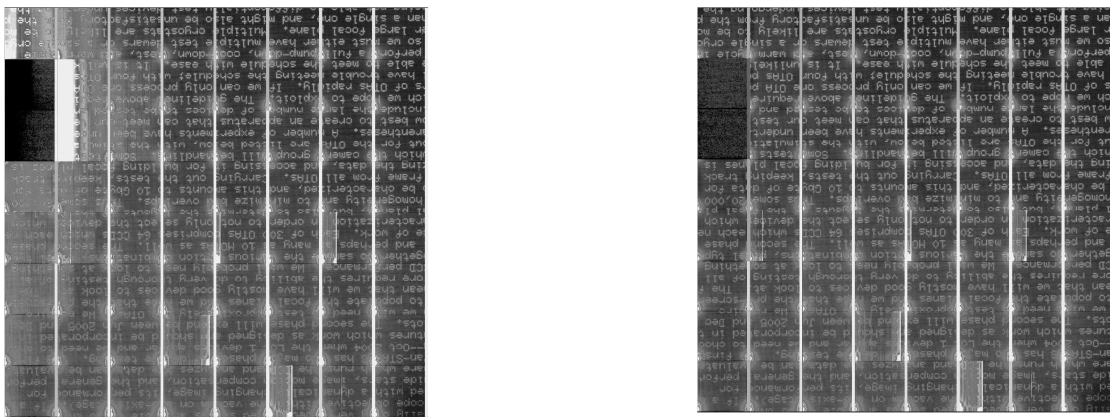


Figure 4. Image from an OTA with two defective cells showing operation with all cells driven (left) and with the defective cells disabled (right).

One of the attractive features of this architecture is the programmed excision of defective cells. More specifically, we can set the cell logic to disconnect the parallel gates and the output video of any cell from the respective bus lines and

allow them to float. This can be effective, for example, in dealing with gates that are shorted to substrate. Under bias such gates inject large amounts of charge into the device, and this charge can spread over a major portion of the imager. An example is shown in Figure 4, which shows an imager with two bad cells in the leftmost column. By programming these cells off, several nearby cells become cleared of spurious charge. From these images, one can conclude that the injected charge has apparently spread across distances of more than a centimeter.

2.2 Pixel size and performance

One design choice that needed to be made before proceeding to the second design was the style and size of the pixel. The pixel size has important processing implications because this type of device requires four phases per pixel and uses four levels of polysilicon. The gate layout and routing of the phases from pixel to pixel leads to a more complex structure than that of a conventional CCD. Unless carefully laid out, the pixel can have stacks of as many as four polysilicon layers in some areas. This is undesirable from a process point-of-view because of stress issues and because we use a two-level metal process with planarized oxide layers for interlevel dielectric isolation. Topologically prominent features such as stacks of three or four poly layers are not desirable in such a process for obvious reasons, especially, as we will see later, when metal lines must run over the pixels.

A pixel size of 10 μm , or 0.26 arcsec using the Pan-STARRS plate scale of 38.5 $\mu\text{m}/\text{arcsec}$, was deemed a desirable goal. However, given the complexity of the pixel and lack of prior experience with OTCCD pixels of this size, we elected to try both 10- μm and a more conservative 12- μm version of the OTA. Pixel style was less important, but given that the layouts were quite different it was decided to try both in the event one proved to yield better. Photos of the 12- μm versions of both styles are shown in Figure 5. Pixel sizes below 10 μm are likely to be very difficult with current processing.

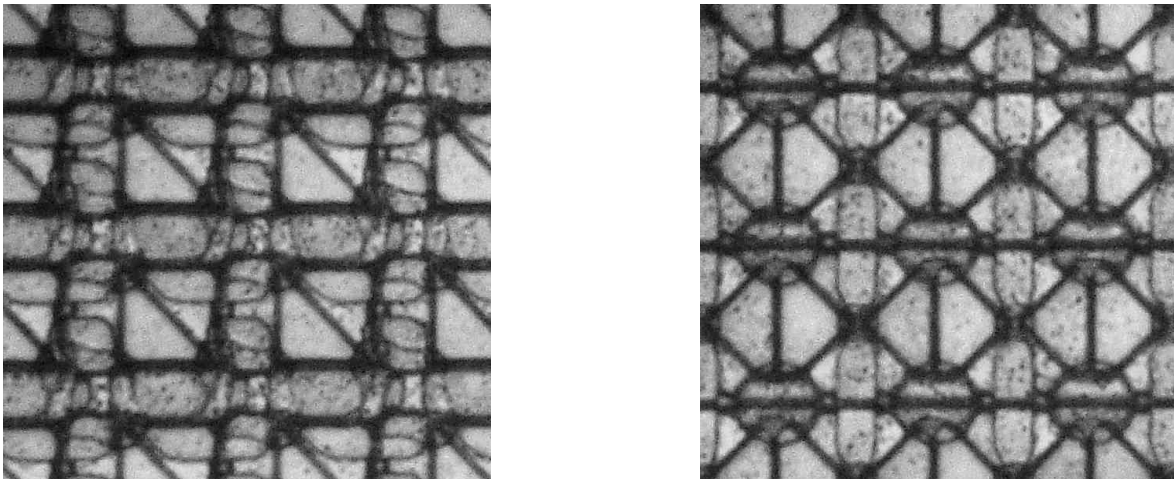


Figure 5. Photographs of 12- μm versions of the two pixel styles, with type 1 on the left and type 2 on the right.

Test data showed that both pixels sizes and pixel styles worked well, and that there were no obvious differences in yield. The 10- μm , type-2 pixel did require higher clock swings ($>8\text{ V}$), probably due to a marginal overlap of the poly gates in some regions of the pixel. With a pixel redesign this issue could likely be resolved.

2.3 Spurious charge (“glow”)

One of the issues that emerged from early testing was “glow” or spurious charge, which can be seen in the corners of the cells in Figure 4. More detailed imagery revealed the spatial location of the sources to be a set of inverters that drive the pass transistors for the parallel clocks, as well as the output amplifier. These inverters translate the low-voltage (0 – 5 V) logic levels to higher levels (0 – 12 V or more) to enable adequate turn-on of the pass transistors T_p . The inverter circuit and pass transistor are depicted in Figure 6. The inverter-related glow is strongly dependent on the high rail voltage V_{DDH} , and has a threshold at around $V_{DDH} \approx 12\text{ V}$.

The origin of this problem lies at the drain of the NMOS depletion load T_L of the high-voltage inverters, as illustrated in Figures 6 and 7. When T_D is on, the output of inverter is low, and V_{DDH} is dropped almost entirely across the load FET T_L . This leads to a high-field region at the drain of T_L (Figure 7, upper). Electrons flowing across this region undergo impact ionization, and the electron-hole pair generation further leads to light emission from carrier recombination. This problem does not occur when the drive transistor T_D is turned off and sustains the full V_{DDH} across it. This is because no current is flowing through T_D when it is turned off, and therefore no carrier multiplication takes place near the drain.

One of the most sensitive and convenient ways to monitor this phenomenon is to measure the substrate hole current generated by the impact ionization. This current is several orders of magnitude smaller than the total drain-source current and thus much easier to detect than looking for a small increase in the drain current. Figure 9 shows an example of the substrate current for depletion-mode MOSFETs used as the active load in the inverter. For the original design the substrate current (curve labelled non LDD) shows a well-defined increase at a drain bias of about 11 – 12 V. This is approximately the value at which the glow first becomes visible in the device imagery.

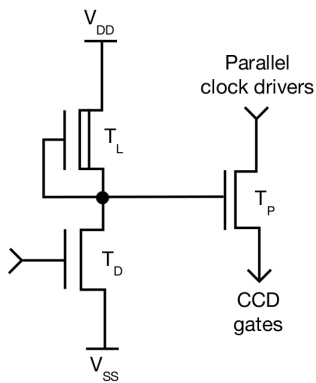


Figure 6. Schematic of a high-voltage inverter driving the pass transistor that controls the parallel clock phases.

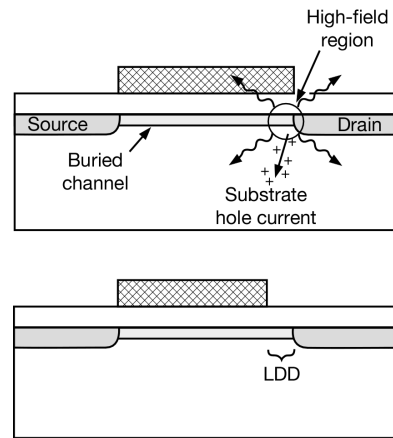


Figure 7. Upper: Light emission is the result of high fields at the drain of the load transistor T_L in Figure 4. Lower: Drain field can be lowered by inserting a region of reduced doping (LDD) next to the drain.

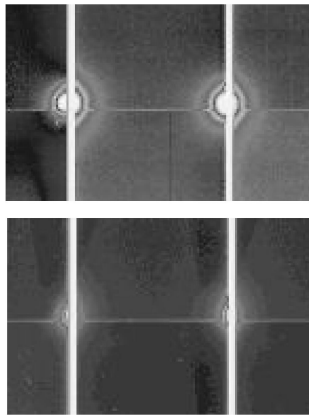


Figure 8. Upper: Glow at the corners of two cells without (upper) and with (lower) the LDD feature in the inverters that drive the pass transistors; $V_{DDH} \approx 14.5$ V.

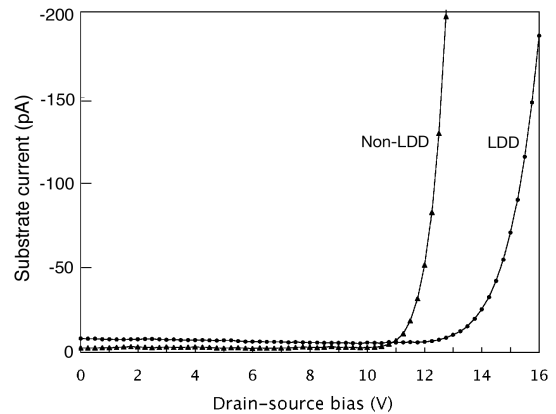


Figure 9. Measurements of substrate hole current in non-LDD and LDD versions of the active load as a function of the drain-source bias.

The standard method for dealing with the ionization effects is to modify the doping in this portion of the device to reduce the high fields at gate-drain edge. In the method called lightly doped drain (LDD) a region of reduced n-dopant

is introduced between the n^+ drain and the MOSFET channel. In our case the channel is already lightly doped n-type by the buried-channel implant, and a simple and expedient way to mimic the LDD process is to pull the n^+ drain away from the gate edge by about $1.5 \mu\text{m}$.

This technique was applied to some lot-1 wafers that had been held back in the process prior to metallization. Because the polysilicon gates for the logic had already been patterned our only option was to etch a small region of polysilicon next to the drain. This foreshortening of the gate had no adverse affect on the performance. However, it did reduce the high field at the drain, as is evident in the curve labeled “LDD” in Figure 9. The onset of carrier multiplication has been moved out by almost 3 V, and this extra operating margin for V_{DDH} enabled better turn-on of the pass transistors.

A comparison of imagery taken under identical conditions on devices with and without this feature is shown in Figure 8. The integration time here was 500 s, and the intensity scaling was 0 – 2000 e^- . Some glow is still evident in the non-LDD case, but we believe this originates in the output amplifier where two of the FETs have the same hot-carrier issue. On these transistors the problem could not be fixed as simply as on the high-voltage inverters, but in the device redesign for subsequent lots the issue can be addressed in a straightforward way.

2.4 Substrate bias and quantum efficiency

One of the design variants that was incorporated as a split in lot 1 was a feature that enables biasing of the substrate independently of the active circuitry. This is possible because the devices are fabricated on high-resistivity, float-zone wafers, and with such material it is possible to decouple the back surface p^+ layer from the frontside circuitry via the depletion zone. The special design considerations for such an approach are described elsewhere.⁵ The material in lot 1 included 4000- $\Omega\text{-cm}$ wafers from Wacker and 14,000- $\Omega\text{-cm}$ material from Topsisil. Substrate bias allows thicker devices to be made while maintaining not only full depletion but enhanced depletion-layer fields for a smaller charge PSF.⁶

One of the major benefits of this is improved quantum efficiency (QE) in the near IR. Figure 10 below shows QE data from a 45- μm -thick back-illuminated OTA with no substrate bias compared with a 75- μm -thick OTA with a substrate bias of -40 V. In both cases the back-surface treatment was an ion implant annealed by a pulsed excimer laser. A two-layer anti-reflection coating was deposited on the device. Of note in these data is the QE of >30% at $\lambda=1.0 \mu\text{m}$.

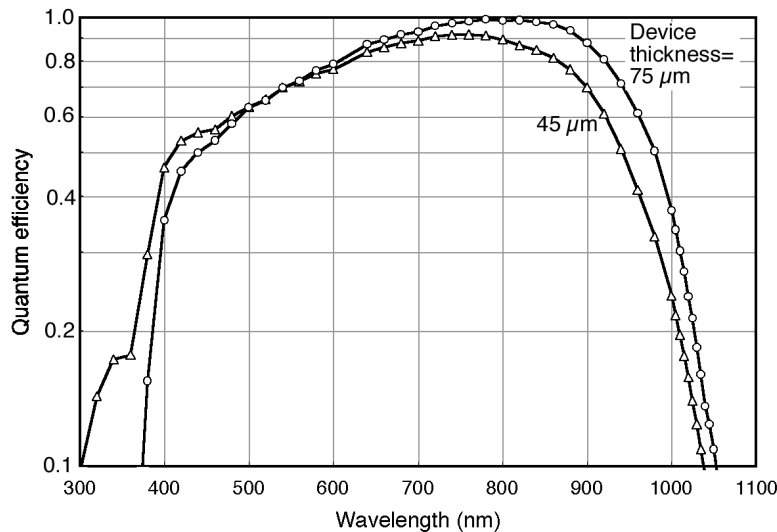


Figure 10. Measured quantum efficiency at -70°C of a 45- μm thick OTA without substrate bias and a 75- μm -thick device with -40 V substrate bias.

2.5 Metallization

An extensive set of metal control lines is needed to supply the I/O of this device. Conventional scientific CCD imagers do not generally face this problem, unless the need for high speed drives the designer to make use of extensive metal

strapping over the pixels for the parallel clocks. The OTA, on the other hand, has many features in common with active pixel sensor (APS) devices and can be viewed as a cross between CCDs and APSs. The latter are strapped with multiple metal lines running across every pixel for address, reset and readout functions. In the prototype OTA, these lines were all routed along the horizontal and vertical “streets” between cells, as can be seen in Figure 11. This approach was chosen for reasons of process conservatism, but a consequence is that the dead space between cells can be significant. A relatively large percentage of this dead space results from the lines running vertically between columns of cells and amounts to 350 μm .

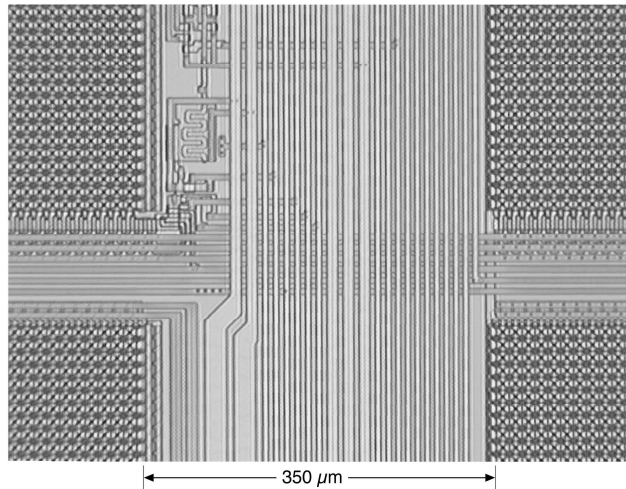


Figure 11. Photograph of a portion of the OTA showing the horizontal and vertical metal lines that crisscross the device.

One design variant that was tried on some wafers in lot 1 was to place the logic-related lines over the pixel arrays of the cells, while leaving the lines associated with the output video in the streets. The cell pitch was not changed, only the two metal layers were altered for this test, so that the devices with this split had unused space between cells. However, as shown in Figure 12 (right) this could lead to improved fill factor in a device redesign where the cells could be pushed closer. The issue to be resolved, however, was the reduced yield (due to shorts between the metal lines and the pixels) versus the improved fill factor.

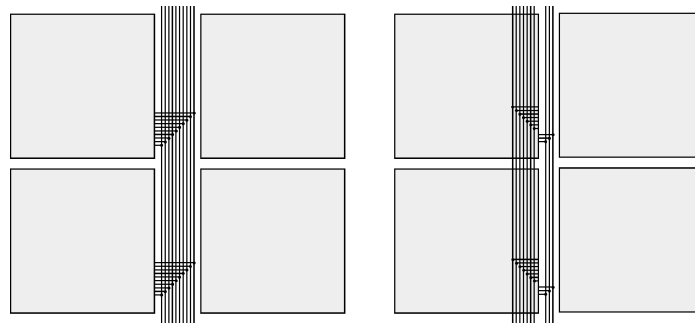


Figure 12. Depiction of the metal control lines which run vertically along the streets between cells. In the design on the left all the lines lie in the streets, while the design on the right places the digital-related lines over the pixels while leaving the analog-related lines in the streets.

The results from lot 1 showed no significant increase in shorts when the digital lines were routed over the cells. This may be attributable to the use of relatively thick interlevel oxide films ($\sim 2 \mu\text{m}$) in the two-level-metal process used for this device. This result has allowed the street width to be reduced from 350 μm to 180 μm , so that the overall device fill factor, originally 89%, can be modestly increased to 91%. Probably the most important outcome is that the metal lines

over the pixels can be made very much wider with no impact on fill factor. This has proved to be valuable in reducing the resistance of some of the lines and addressing some RC delay issues in the first design.

2.6 Noise

Noise levels of the lot-1 OTAs lay roughly in the 10 – 20 e⁻ range for read rates of a few hundred kHz. This is above our goal of 5 e⁻, which is the point at which sky noise would dominate. We have identified two likely suspects. The first is a hot-carrier issue with the second stage source follower of each output amplifier, and the application of the LDD technique should alleviate this problem. The other was the use of a surface-channel FET for the second-stage drive FET, a choice that, had it not introduced significant noise, would have shifted the output video voltage down sufficiently to enable dc coupling to the downstream video chain. In the redesign this will be changed to a buried-channel FET.

3. SUMMARY AND FUTURE PLANS

The first lot of prototype OTAs have proven to be successful on the whole. The major issues that need to be resolved are glow from some transistors and the read noise. Both are well enough understood so that we are confident that the redesigned device will not have these problems and will meet the Pan-STARRS requirements.

The lot-1 testing revealed several attractive design variants that have been incorporated in the next OTA design. This redesign is in fabrication and will supply the OTAs for the first Pan-STARRS gigapixel focal plane (GPFC1) in mid-2006. Some of the key features are:

- Pixel size and style: 10 μm, type 1
- Cell size: 590(H)×598(V)
- Substrate-bias capable
- Digital metal lines over cells

4. ACKNOWLEDGMENTS

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