

# Phys 476: Modern Electronics for Scientists

Spring semester 2026

## 1. Instructor

- **Name:** Prof. Keisuke Yoshihara
- **Email:** kyoshiha@hawaii.edu
- **Office Hours:** Available by appointment. Please send an email to schedule a meeting.

## 2. Class Information

- **Classroom/Lab:** WAT415A
- **Class Hours:**
  - **Tuesday:** 1:30 PM – 4:50 PM [Lecture + Lab]
  - **Thursday:** 1:30 PM – 3:20 PM [Lecture + Lab]

## 3. Course Format

This course combines lectures and laboratory work to provide a comprehensive understanding of electronics in experimental physics.

In the first half of the course, lectures focus on digital circuit fundamentals—introducing logic design, state machines, and timing—while laboratory sessions provide hands-on FPGA programming using FPGA training boards.

In the second half of the course, students transition to project-based learning that mirrors real applications in modern particle physics experiments. Students will design their own artificial intelligence (AI) and machine learning (ML) algorithms, and use High-Level Synthesis (HLS) tools to implement these ML/AI models directly on FPGA hardware.

All lecture notes will be available in an online shared folder, and all example code, lab templates, and reference projects will be shared via GitHub.

## 4. Programming

- **Experience Required:**
  - No prior programming experience is required. However, familiarity with Python or any other programming language will be helpful.
- **Languages Used:**
  - **Verilog:** Primary hardware description language used for FPGA design in lectures and labs.

- **C/C++:** Used for embedded system development and High-Level Synthesis (HLS) workflows.
- **Python:** Used for developing AI/ML algorithms, data processing, and simulation tasks.
- **Tools and Environments:**
  - **Xilinx Vivado:** Main tool for FPGA logic design, synthesis, and implementation.
  - **Vitis IDE:** Used for embedded system development on FPGA platforms.
  - **Vitis HLS / hls4ml:** Tools for implementing AI/ML models on FPGA hardware using C/C++.
  - **Python Environments:** Work will be done primarily using Jupyter Notebook or the terminal.
- **Operating Systems:**
  - Although Vivado and Vitis do **not** support macOS, all required FPGA development will be done on the classroom PCs. Students may use their personal computers for Python-based AI/ML work later in the course, and any OS (Linux, Windows, macOS) is acceptable for that portion.
- **AI Tools:**
  - Students may use AI tools such as ChatGPT to support their coding, debugging, and conceptual understanding.
  - A free ChatGPT account accessible via a web browser is recommended.

## 5. Prerequisite

- It is recommended that students have taken PHYS475. PHYS476 is suitable for students who are interested in digital circuits, AI/ML, or who are motivated to start research in these related fields. A willingness to actively engage with hardware design and programming is essential. If you are uncertain about your preparedness for the course, please consult with the instructor directly.

## 6. Textbook

- **Recommended Textbook:** Russell Merrick, *Getting Started with FPGAs, Digital circuit design, verilog, and vhdl for beginners*
- (optional electronics Bible) Horowitz and Hill: *The Art of Electronics*

## 7. Course Goals

This course aims to develop practical, research-ready skills in digital circuit design and modern AI/ML implementation for physics experiments. Students will learn to design and verify digital systems using Verilog, build embedded applications with C/C++, and apply AI/ML techniques using Python. A central goal is to equip students with the ability to integrate these tools—combining FPGA-based logic design, embedded systems, and AI/ML algorithms—to solve real problems encountered in modern particle physics instrumentation.

## 8. Learning Outcomes

By the end of this course, students will be able to:

- **Programming & Tool Proficiency:**
  - Write and understand Python, Verilog, and C/C++ code used in FPGA and embedded-system development.
  - Use key development tools including Vivado, Vitis IDE, Vitis HLS, and hls4ml.
- **Digital circuit designs:**
  - Understand the core principles of digital logic, state machines, timing, and hardware architecture.
  - Design, simulate, synthesize, and implement digital circuits on FPGA hardware.
  - Debug and validate designs through simulation environments and on-board testing.
- **Machine Learning & AI Integration:**
  - Understand basic ML algorithms and implement them in Python.
  - Develop simple AI/ML models and optimize them for real-time inference.
  - Translate ML/AI models to FPGA using HLS tools and validate their functionality through hardware tests.
- **Research-Oriented Problem Solving:**
  - Apply digital design and ML/AI tools to solve physics-oriented problems.
  - Analyze real or simulated experimental data and train ML models to improve performance.
  - Integrate FPGA logic, embedded software, and ML models into a unified system similar to those used in cutting-edge physics experiments.

## 9. Grading Policy

Grades will be based on a total score composed of:

- **[10%] Attendance:**
  - Because this is a project-based course with significant hands-on laboratory

work, attendance is required. If you must miss a class for unavoidable reasons, you must contact the instructor in advance. Unexcused absences will result in a deduction from the attendance grade.

- **[30%] Homework Assignments:**
  - Short homework assignments will be given intermittently throughout the semester. These may involve small design tasks, simulations, or short coding exercises, and may require brief written summaries or figures. Homework supports the in-class lab work and prepares students for their projects.
  
- **[30%] Midterm Project:**
  - The midterm project focuses on FPGA-based digital circuit design. Students will design, implement, and test a working digital system using Verilog and/or C/C++ (HLS), and submit both a short technical report and an in-class presentation.
  
- **[30%] Final Project:**
  - The final project integrates the full skillset of the course—digital logic, embedded systems, and AI/ML algorithms.

For midterm and final projects, students may choose their own topic, and evaluation will consider:

- difficulty of the chosen project,
- quality and completeness of the design and implementation,
- clarity and technical depth of the final presentation.

## 10. Timetable

A	B	C	D
Week	Date	Lecture Topics	Lab Activities
1	Jan14	Lecture 1: Course Introduction and Overview <ul style="list-style-type: none"> <li>• Course objectives, materials, and setup explanation</li> </ul> Lecture 6: Combinational Circuit Design (Part 1) <ul style="list-style-type: none"> <li>• Boolean algebra and basic logic gates</li> </ul> Lecture 7: Introduction to Verilog (Basic) <ul style="list-style-type: none"> <li>• Syntax, modules, and combinational logic implementation</li> </ul> Lecture 9-1: Vivado Basics (Hands-on) <ul style="list-style-type: none"> <li>• Vivado software overview</li> </ul>	Vivado Design Flow, Combinational Circuit
1	Jan16	Lecture 3: Transistors <ul style="list-style-type: none"> <li>• MOSFETs, CMOS basics, and transistor-level logic</li> </ul> Lecture 9-2: Vivado Basics (Hands-on) <ul style="list-style-type: none"> <li>• Debugging and simulation of basic circuits</li> </ul>	Continued
2	Jan 21	Lecture 4: Basics of CMOS Technology <ul style="list-style-type: none"> <li>• Characteristics and power efficiency in CMOS circuits</li> </ul> Lecture 8: Combinational Circuit Design (Part 2) (Lecture + Hands-on) <ul style="list-style-type: none"> <li>• Multiplexers, decoders, encoder, Comparator, Adder</li> </ul>	Testbench design, Simulation
2	Jan 23	Lecture 5: Introduction to FPGA <ul style="list-style-type: none"> <li>• FPGA internal architecture and configurable blocks</li> </ul> Lecture 8: Combinational Circuit Design (Part 2) (Lecture + Hands-on) <ul style="list-style-type: none"> <li>• Multiplexers, decoders, encoder, Comparator, Adder</li> </ul>	Continued

3	Jan 28	Lecture 10: Combinational Circuits (Part 3) • Adders, Subtractors, Complementer Lecture 11: Vivado Simulation (Hands-on) • Debugging and simulation of basic circuits	
3	Jan 30	Lecture 12: (Lecture + Hands-on) Sequential Circuits Design (Part 1) • Flip-Flops, Latches, Ripple Counter	Sequential Circuit: RSFF, DFF, and TFF
4	Feb 4	Lecture 13: (Lecture + Hands-on) Sequential Circuits Design (Part 2) • Flip-Flops, Shift Registers, Binary Counter Lecture 14 (Hands-on): Sequential Circuit in Vivado • Implementation of Binary Counter	Sequential Circuit: binary counter, external clock usage
4	Feb 6	Lecture 2: Data Acquisition Techniques in HEP • Overview of DAQ systems and experimental apparatus	Continued
5	Feb 11	Lecture 15-1 (Lecture + Hands-on): Advanced Circuits • Decimal Counter, Timer, Chattering Effect, Asynchronous to syn	Counter and Timer
5	Feb 13	Lecture 15-2 (Lecture + Hands-on): Advanced Circuits • Decimal Counter, Timer, Chattering Effect, Asynchronous to syn	Continued
6	Feb 18	Lecture 16 (Lecture + Hands-on): Memory and FIFO • Memory and FIFO	FIFO design
6	Feb 20	Lecture 17 (Lecture + Hands-on): Finite State Machine • State Diagram, LED example, Serializer in simplified model	Serializer as FSM
7	Feb 25	Midterm project with FPGA	Design your own model
7	Feb 27	Midterm project with FPGA	Design your own model
8	Mar 4	Special Lecture (Part1)	Matt Andrew (TBD)
8	Mar 6	Special Lecture (Part2)	Chris Ketter (TBD)
9	Mar 11	Midterm Presentation	Midterm Presentation
9	Mar 13	Lecture 21: Neural Network - AND Gate, Simple Perceptron, Logistic Regression	
10	Mar 18	Spring Break	
10	Mar 20	Spring Break	
11	Mar 25	Lecture 22: Multi-Layer Neural Network - Multi-Class Logistic Regression, XOR, Multi-Layer Perceptrons	Basic Python ML Implementation
11	Mar 27	Lecture 23: Deep Neural Network - Activation functions, Vanishing gradient problem, Overfitting, Optimization methods, Batch normalization	Continued
12	Apr 1	Lecture 24: Introduction to hls4ml - HLS, Pruning, Quantization	hls4ml tutorial
12	Apr 3	Lecture 24: Introduction to hls4ml (cont'd) - HLS, Pruning, Quantization	hls4ml tutorial
13	Apr 8	Lecture 25: Introduction to hls4ml (2) - Vitis HLS Tutorial	hls4ml tutorial
13	Apr 10	Lecture 18: Ethernet Transmission Lecture 19: ZYNQ System	MicroBlaze and ZYNQ tutorials
14	Apr 15	Special Lecture (Part3) -- Versal FPGA, AI Engine	Yun-Tsung Lai (KEK)
14	Apr 17	Lecture 26: Introduction to hls4ml (3)	hls4ml tutorial
15	Apr 22	Final Project Work	Final Project Work
15	Apr 24	Final Project Work	Final Project Work
16	Apr 29	Final Project Work	Final Project Work
16	May 1	Final Project Work	Final Project Work
17	May 6	Final Project Work	Final Project Work
17	May 8	Final Presentation	Final Presentation
18	May 13	OFF	OFF
18	May 15	OFF	OFF

\* The latest timetable can be found here: ([link](#))