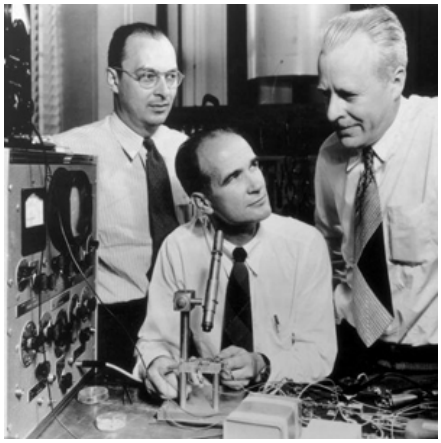
PHYS475 Electronics for Physicists



Professor Gary S. Varner

Last updated 5-NOV-2016

Fall Semester, 2016.

Latest:

- Introduction to Programmable Logic ("Firmware"): [3-NOV-2016]
- Link to "Firmware Bootcamp"
- FW Session #2 reading **(for Thursday, Nov. 10)**: [UCF] [constraints example] and [homework - self study]
- FW Session #3 reading **(for Tuesday, Nov. 15)**: [6800 example]
- Labs 12 & 13 [Supplemental Material]
- Lab 12 [pdf]
- **Design Review:** Thursday, Dec. 1 during class period
- **Final Presentation: Friday, Dec. 9 @ 9:30am**
- **Current** version (2-NOV-2016) of the course Syllabus may be found [here].

- Some helpful documentation for preparing your labs:
  - Sample template for scientific writing, including LaTex source file
  - Another example of a proper Scientific Report, with illustrations of how the captions for Figures and Tables should be treated, as well as the use of References

This is a Writing Intensive course, and the Student Learning Outcomes are posted [here].

All lab work is to be recorded in your notebook. A hand-out on expectations for lab detail recording is [here].

For sample tex file of the LAB # 1 handout, click here
Figures are drawn with the xfig utility, which is widely available for free in most unix/linux distributions.
For PC users, a very nice program which allows one to run such utilities under a Windoze environment is cygwin: http://cygwin.com/

Lecture references:

- PHYS475 Intro [pdf]
- 5spice simulation tool (free) [link]
- PHYS476 in Spring (as follow-on) [2011] and special ASIC version
- Thanks to Matt Andrew: Tutorials on how to solder: [through-hole] [surface-mount 1] [surface-mount 2]

Sample Design Review

Lab # 1 -- DC Circuits

Lab 1: click here

Encapsulated postscript, PDF figures as an example (do not Write Up Lab #1)

Lab 1, Figure 1 : [eps] [pdf]
Lab 1, Figure 2 : [eps] [pdf]
Lab 1, Figure 3 : [eps] [pdf]
Lab 1, Figure 4 : [eps] [pdf]
Lab 1, Figure 5 : [eps] [pdf]
Lab 1, Figure 6 : [eps] [pdf]

Lab # 2 -- Capacitors

Lab 2: click here

Encapsulated postscript, PDF figures in the lab write-up:

Lab 2: xfig files archive [zip]
Lab 2, Figure 1 : [eps] [pdf]
Lab 2, Figure 2 : [eps] [pdf]
Lab 2, Figure 3 : [eps] [pdf]
Lab 2, Figure 4 : [eps] [pdf]
Lab 2, Figure 5 : [eps] [pdf]
Lab 2, Figure 6 : [eps] [pdf]
Lab 2, Figure 7 : [eps] [pdf]

Lab # 3 -- Diode Circuits

Lab 3: click here

Encapsulated postscript, PDF figures in the lab write-up:

Lab 3: xfig files archive [zip]
Lab 3, Figure 1 : [eps] [pdf]
Lab 3, Figure 2 : [eps] [pdf]
Lab 3, Figure 3 : [eps] [pdf]
Lab 3, Figure 4 : [eps] [pdf]
Lab 3, Figure 5 : [eps] [pdf]
Lab 3, Figure 6 : [eps] [pdf]
Lab 3, Figure 7 : [eps] [pdf]

Lab # 4 -- Bipolar Transistors

Lab 4: click here

Encapsulated postscript, PDF figures in the lab write-up:

Lab 4: xfig files archive [zip]
Lab 4, Figure 1 : [eps] [pdf]
Lab 4, Figure 2 : [eps] [pdf]
Lab 4, Figure 3 : [eps] [pdf]
Lab 4, Figure 4 : [eps] [pdf]
Lab 4, Figure 5 : [eps] [pdf]
Lab 4, Figure 6 : [eps] [pdf]
Lab 4, Figure 7 : [eps] [pdf]
Lab 4, Figure 8 : [eps] [pdf]
Lab 4, Figure 9 : [eps] [pdf]

Lab # 5 -- Field Effect Transistors

Lab 5: click here

Archives of source files:

Lab 5: xfig files archive [zip]
Lab 5: eps files archive [zip]
Lab 5: PDF files archive [zip]

Lab # 6 -- Operational Amplifiers I

Lab 6: click here

Archives of source files:

xfig files archive [zip]
eps files archive [zip]
PDF files archive [zip]

Lab # 7 -- Operational Amplifiers II

Lab 7: click here

Archives of source files:

xfig files archive [zip]
eps files archive [zip]
PDF files archive [zip]

Lab # 8 -- Comparators

Lab 8: click here

Archives of source files:

xfig files archive [zip]
eps files archive [zip]
PDF files archive [zip]

Lab # 9 -- Logical Gates

Lab 9: click here

DO NOT WRITE UP

Lab # 10 -- Flip Flops

Lab 10: click here

DO NOT WRITE UP

Lab # 11 -- Counters, Shift Registers and Timing

Lab 11: click here

DO NOT WRITE UP
