Overview of Trigger/DAQ design for Super-KEKB

based on discussions at Belle Trigger/DAQ workshop in Nara (Nov.03)

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1. Introduction
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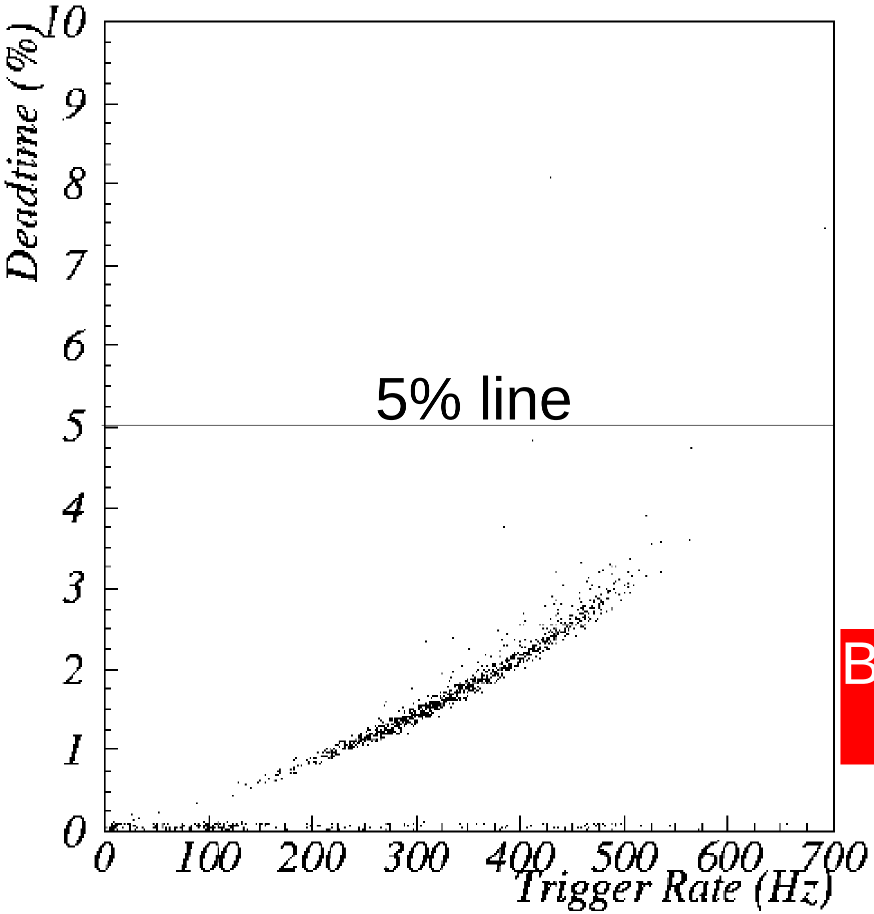
Super B Factory Workshop in Hawaii, 1/20/04

1. Introduction

- Expected trigger rate @ Super-KEKB is more than 10KHz with an event size of a few hundred kilobytes.

- Belle DAQ : running at ~ 400Hz with the size of ~40KB/event.
  - currently using Q-to-T conversion + multihit TDC
    => no pipeline is used.
    => has readout dead time.



~2% @ 400Hz

becomes >50% @ 10KHz
(linear extrapolation)

Belle's DAQ is not usable for SuperKEKB
-> need to develop pipelined DAQ

* Data flow rate

- Assume 10KHz trigger with 200KB/event size
  -> results in 2GB/sec data flow at Level 1

- Online data reduction @ Belle
  So-called L2.5 trigger
  - ultra-fast tracking to discard off-IP events
  - take "physics-trig'd events" (like Etot > 3GeV)
  -> Reduction factor : ~50%
  => flow rate -> reduced to 1GB/sec
  .... still too much

  c.f. Expected data flow at storage in LHC experiments
  ~ 200-300MB/sec

We need a factor 5 more reduction!
- Trigger tightening? <- already tight enough
- Sophisticated event selection
  ->A large scale Level 3 farm is required.

Design strategy

- Make use of know-hows in current Belle's Trigger/DAQ systems as much as possible
- Pipeline based readout is essential
- Use of common electronics as possible

  $\rightarrow$ CoPPER (Common readout platform)

  * unified handling of pipeline readout using on-board PC module

  * detail will be covered in Higuchi's talk
- Scalability

  $\rightarrow$ to keep up with gradual increase in luminosity

2. Design of Trigger

- Belle's trigger scheme is working fine and scalable to SuperKEKB environment.
  * Belle's design was made in order to minimize the trigger rate to reduce the DAQ deadtime. -> suitable for SuperKEKB

- Main Triggers
  - CDC : charged track trigger
  - ECL : Total energy and cluster counting

<u>Things not yet fixed</u>

- Event Timing (required for CDC tracking/SVD L0 trigger)
  * Belle's timing : TOF/TSC -> jitter < 10ns
    SuperKEKB : CsI ~ 20ns
- Z-trigger
  * No fast Trigger output from SVD readout chip
  * Need to think about inteligent z-trigger using CDC stereo.

Iwasaki @ Nara WS

Available Sub-Triggers

Trigger Type		Belle	Super-Belle
Charged Track	r/phi	CDC	CDC
	z	CDC or SVD	n/a (CDC ???)
Energy		ECL	ECL
Cluster		ECL	ECL
Timing		TOF	ECL
		ECL	
Muon		KLM	KLM
Bhabha		ECL	ECL
		EFC	
Cosmic		ECL	ECL

- Charged Track Z-Trigger
  - It is very powerful to reduce BG
  - We should think about it : special device or use CDC stereo hits
- Timing source
  - Redundant timing sources are preferable

Iwasaki @ Nara WS

L1 Rate @ SKEKB : Rough Estimation

Exp.	Rate	Luminosity		Current		Magic Number
		Rate / Lum	Rate @ 10^35	Rate / Current	Rate @ 13A	20
7	200	13	13 k	210	2.6 k	n/a
17	250	4.5	4.5 k	130	1.7 k	n/a
27	350	4.4	4.4 k	150	2.0 k	7.0 k

- Vacuum is the biggest factor to estimate the rate
- CDC Z-trigger is included in above numbers
  - We have to live @ SKEKB without Z triggers
    - ~30% increase without Z trigger (Exp.31)
      4.4 kHz x 1.3 = 5.7 kHz
    - On the other hand, if we have SVD Z-trigger, we can reduce L1 rate by factor 2~5.
- Very important
  - We can not know real BG situation in SKEKB

Physics Rate
1.0 k

3. Design of DAQ

Requirements to DAQ

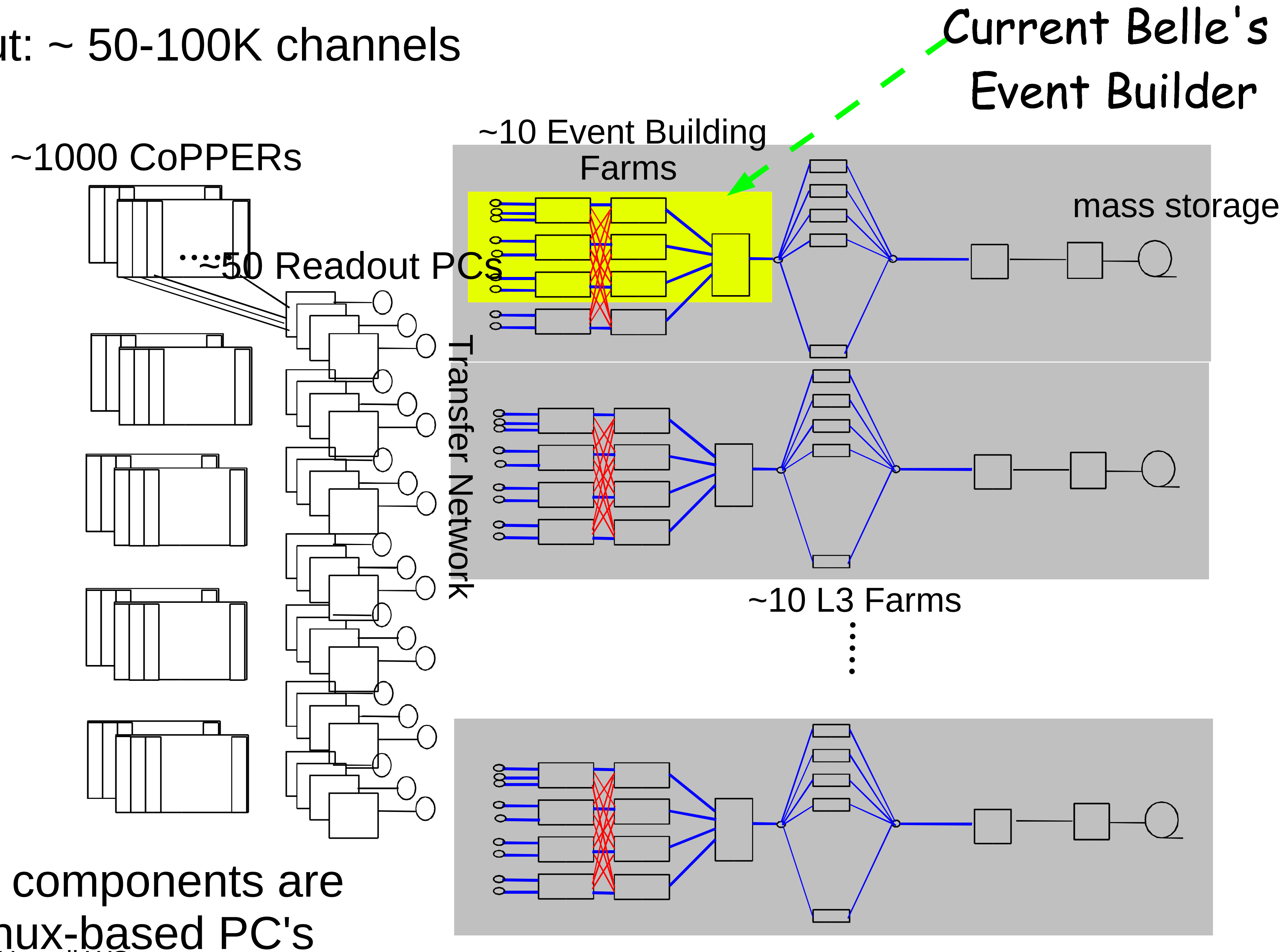
	Belle	SuperKEKB(>10^{35})
Physics trigger rate	100Hz	>1KHz
Maximum trigger rate	500Hz	10-30 KHz
Event size at L1	40KB/ev	200-300KB/ev
Data flow rate at L1	20MB/s	> 2 GB/sec (>5 GB/sec w/o z trigger)
Data flow at storage	10MB/s	250MB/sec
Reduction factor in DAQ	2	5~10

How to achieve higher event reduction factor

→ Key of DAQ design

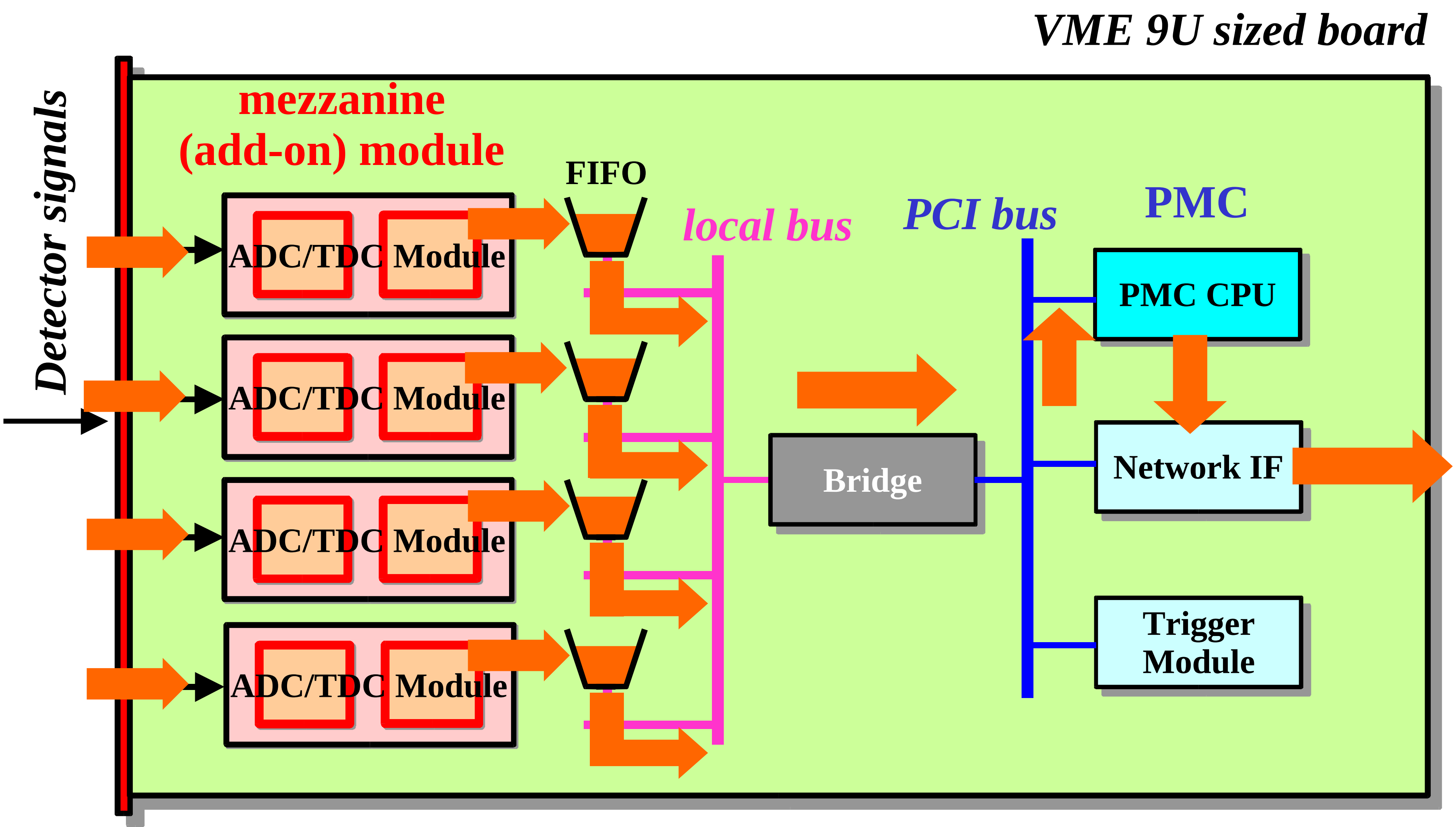
Reference Design

Input: ~ 50-100K channels



all components are Linux-based PC's

Schematic of the DAQ Platform(CoPPER)



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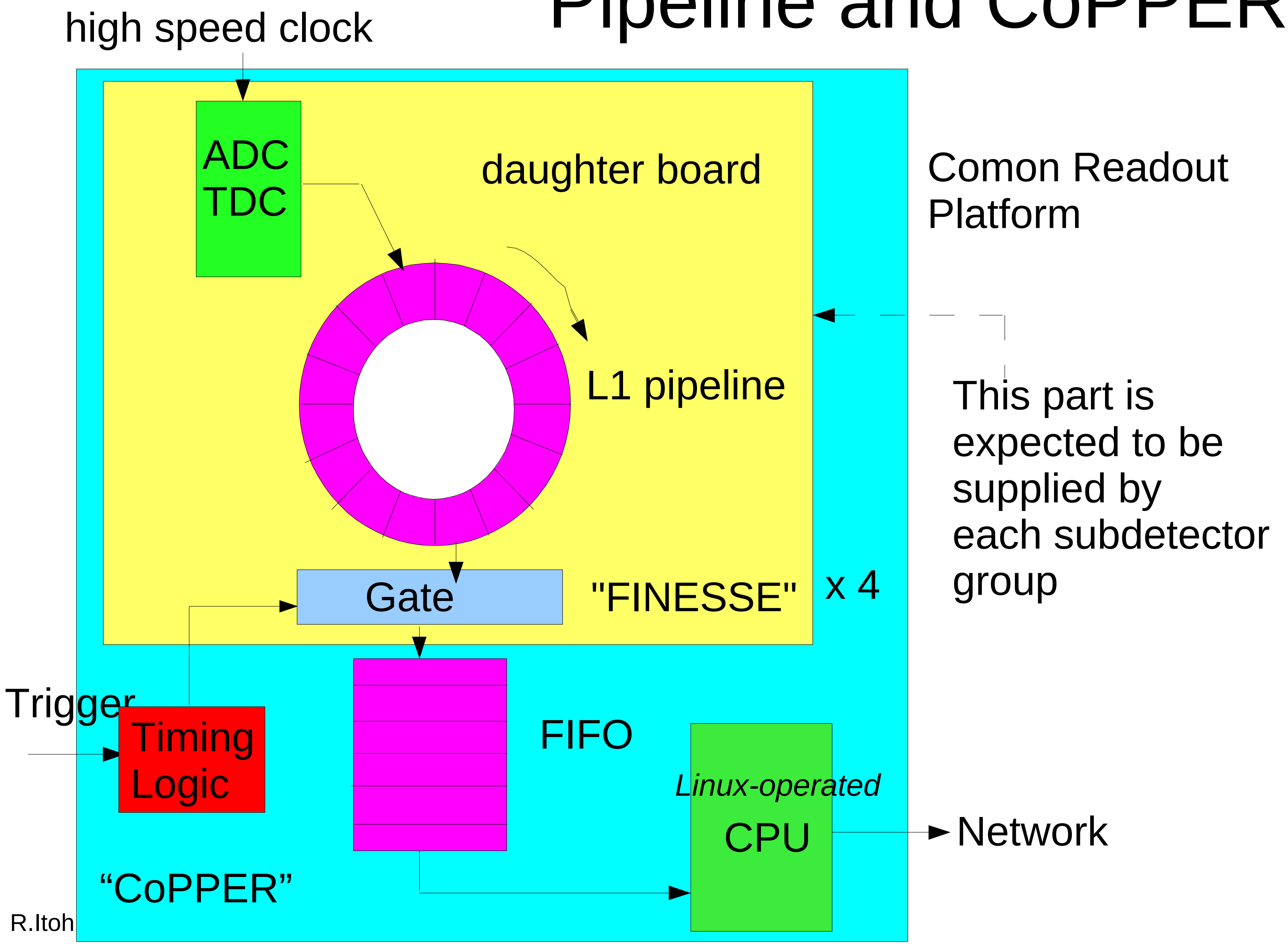
Pipeline and CoPPER



Detector Electronics Quick Summary

- SVD : CMS APV25 chip -> promising!
- Pixel : candidate = CAP(continuous acq.) <===> "striplet" option
  large data size : 620-1280KB/evt (4bytes/pixel,1% occ.) too much!
- CDC : 3 approaches
  1) ADC with waveform sampling (10bit@200MHz)
  2) pipelined TDC with current Q-to-T conversion
  3) TDC + FADC (TMC+12bitFADC@20MHz)
- ECL : wave form sampling needed to avoid pileup effect
  (12bit FADC@2MHz for barrel, 20MHz(?) for pure CsI)
- TOP/RICH : need to manage pixel photo-detector
  * Time stretcher(Varner)/AMT(Arai), analog pipeline(Ikeda)
- KLM : readout scheme is not so much different from Belle's
  regardless of choice of detection device (RPC/Sci. Tile)
  * "hit" info multiplexing + on-board data compression

all electronics will be equipped as "FINESSE"
implemented as daughter board on CoPPER.

Expected event size at L1

	Belle	SuperKEKB
Pixel(Striplet)	-	~1000KB(!?)(30KB)
SVD	15KB	~30KB
CDC	6KB	~10KB
PID	3KB(TOF/ACC)	~20KB
ECL	8KB	~100KB
KLM	3KB	~3KB
TRG/others	3KB	~3KB
	~40KB	~200KB

* Pixel: event size compression is absolutely necessary
* ECL : wave form sampling to obtain required resolution
(~10 buckets/hit*12bit)
-> can be reduced to 1/5 by feature extraction
* Other: event size compression using word-packing/"zip"

→ **Event Processing on CoPPER** → ~100KB/ev

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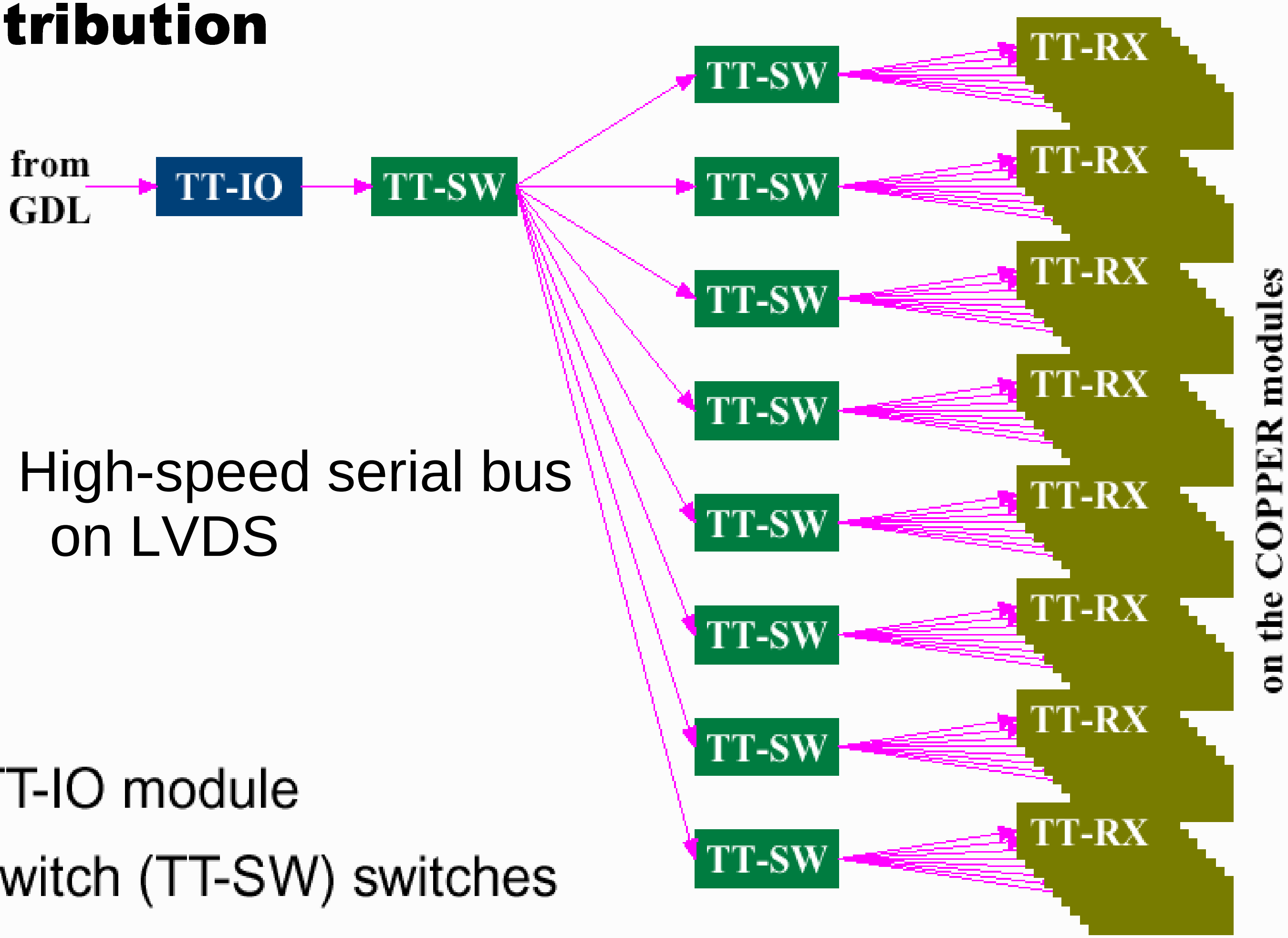
Timing Distribution

2 -step
cascade



High-speed serial bus
on LVDS

- Master TT-IO module
- 1-8 TT-Switch (TT-SW) switches
- 64 distribution by 2-step cascade (4096 by 4-step)
- TT-Receiver (TT-RX) on each COPPER

Multi-stage event building

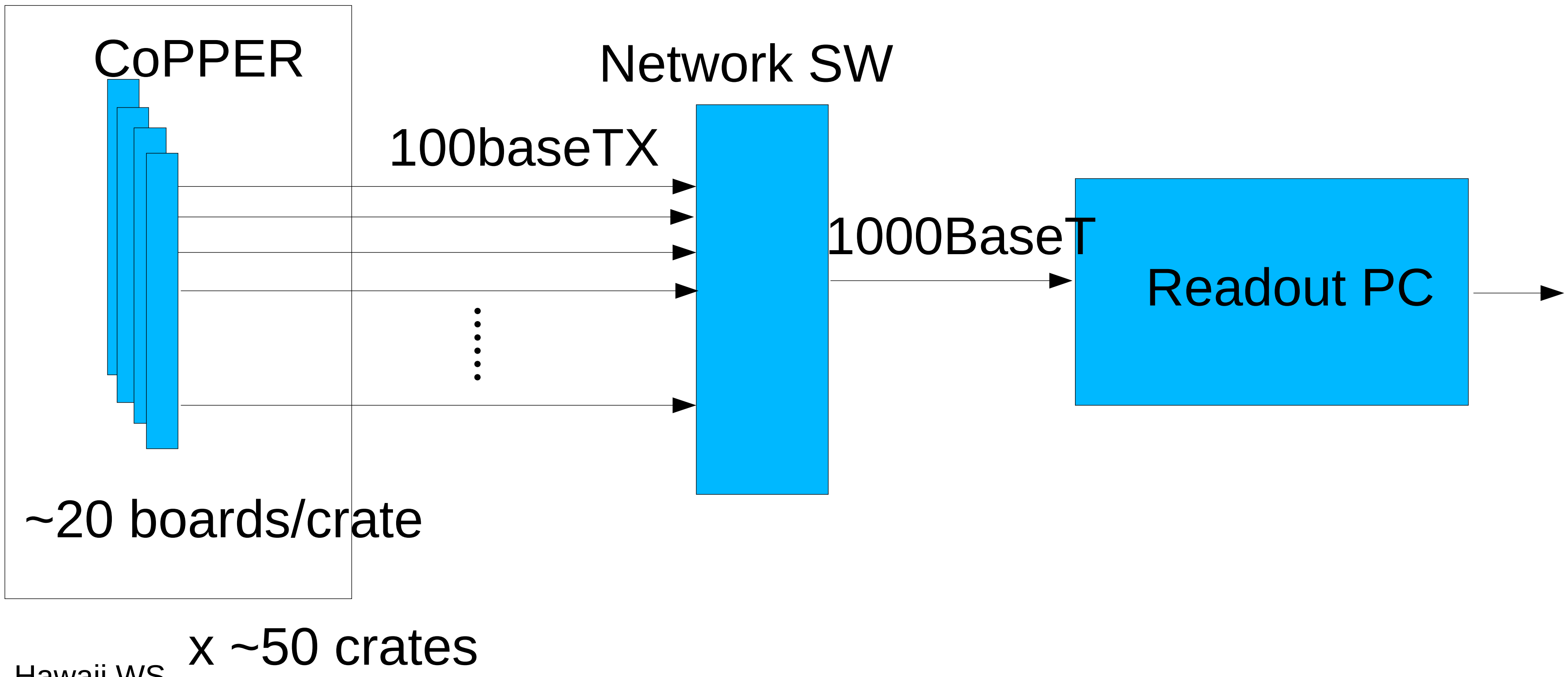
* Event Building is done in 3 steps.
  Stage 1 : Gather event fragments from CoPPERs in a crate
  Stage 2 : Gather event fragments from one subdetector
  Stage 3 : Build complete one event

* Event reduction at each stage
  Stage 1 : Feature extraction, further sparcification -> size reduction
  Stage 2 : Level 2.5 trigger using partial subdetector info.
  ex. Trigger Info + fast CDC tracking -> z trigger
  fast SVD-only tracking -> vertex trigger
  Stage 3 : -> L3 Farm

Common event building software framwork at all stages
("switchless event builder" + BASF)

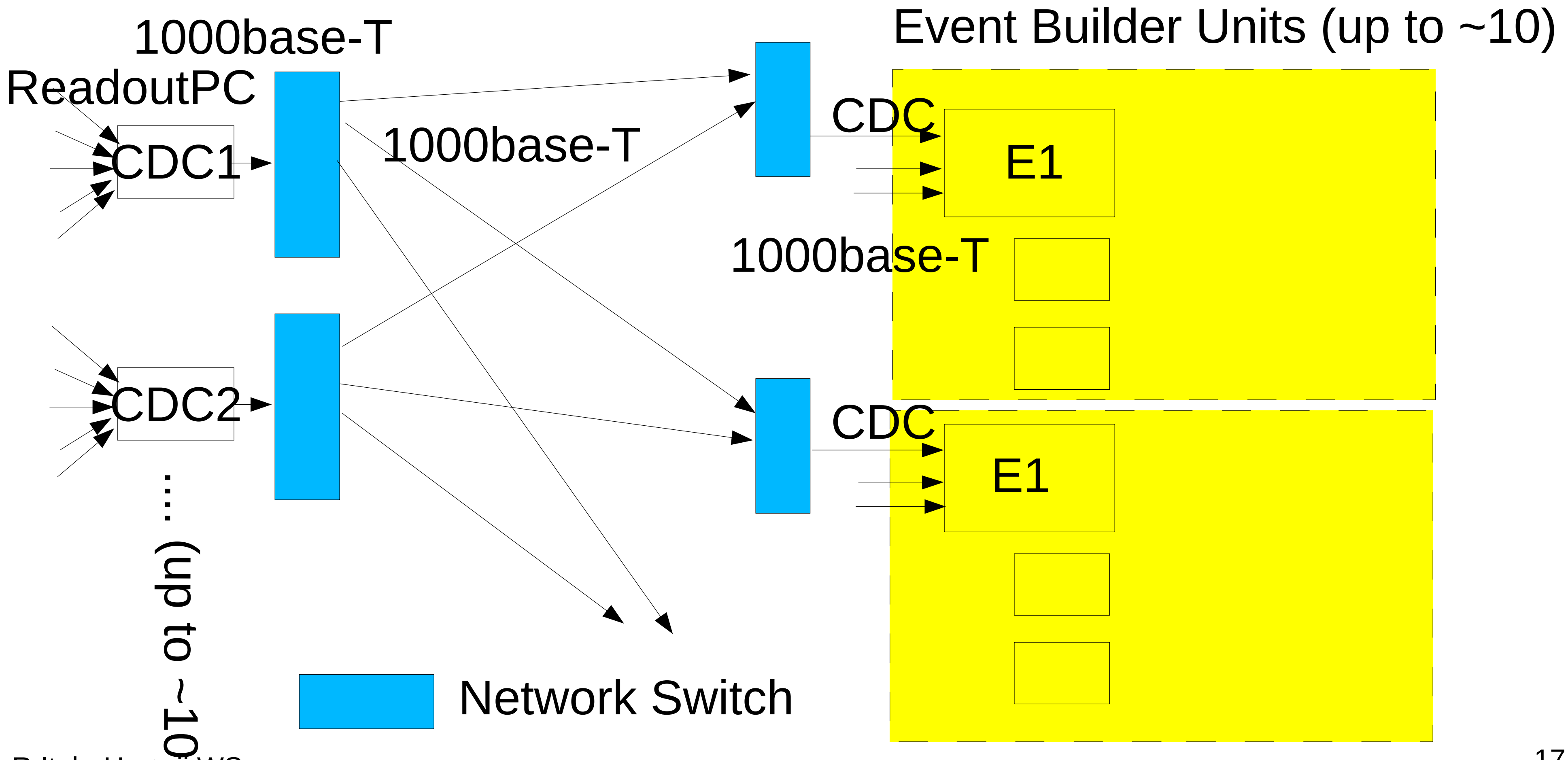
Stage 1 Event Building

* "switchless event builder" software on Readout PC
* Network switch is used to share (a) 1000base-T port(s) on readout PC. Connection between each CoPPER to Readout PC is fixed port-to-port basis and the switch is "transparent".
* Further event size reduction on Readout PC



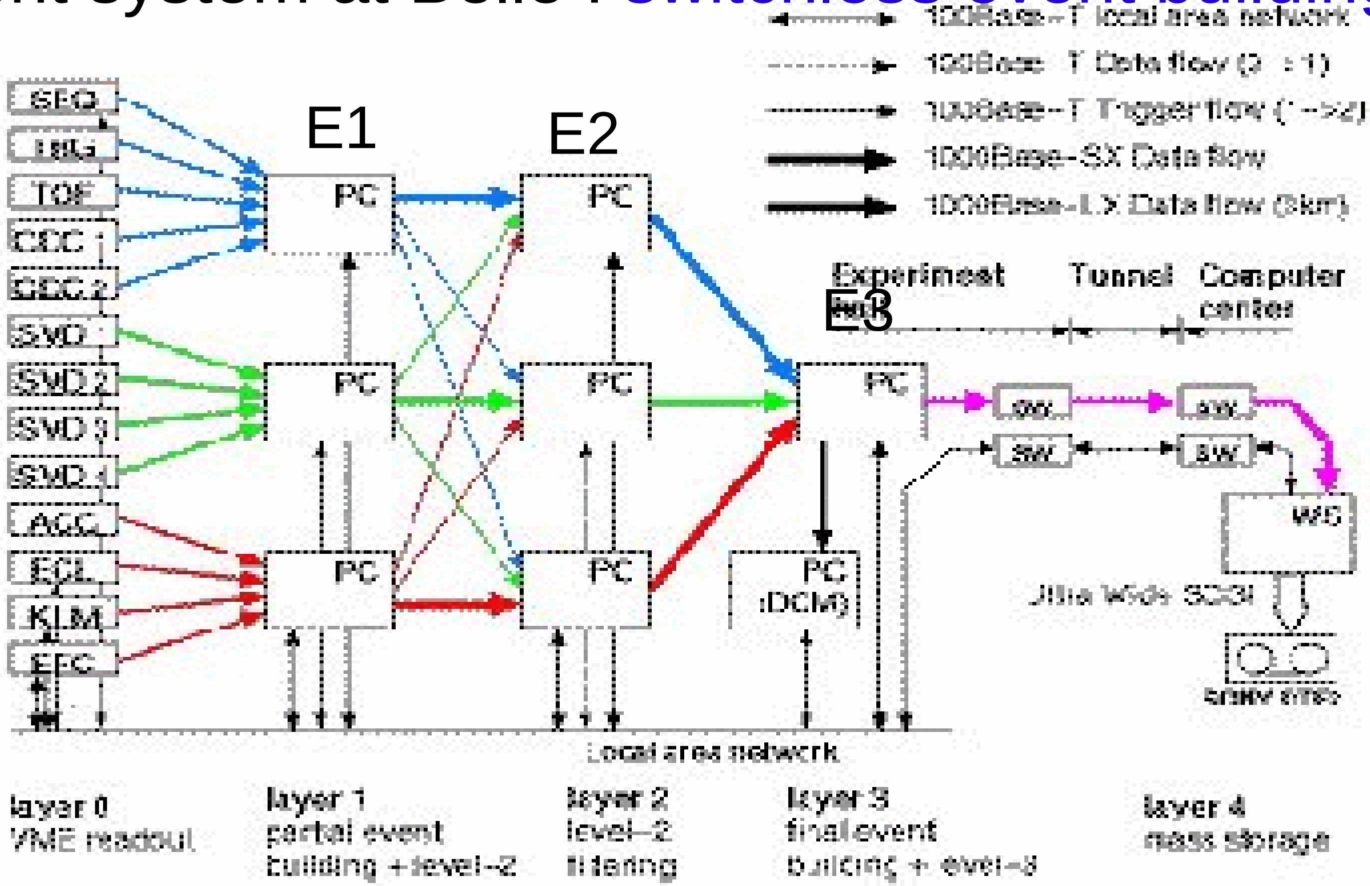
Stage 2 event building

* Readout from 1 subdetector can be from multiple CoPPER crates
* Gather them to form an event from the subdetector using network swich complex.
* The same "swithless event building software" on E1 node
* Transparent port-to-port connection from ReadoutPC to E1



Stage 3 event building

Current system at Belle : switchless event building farm

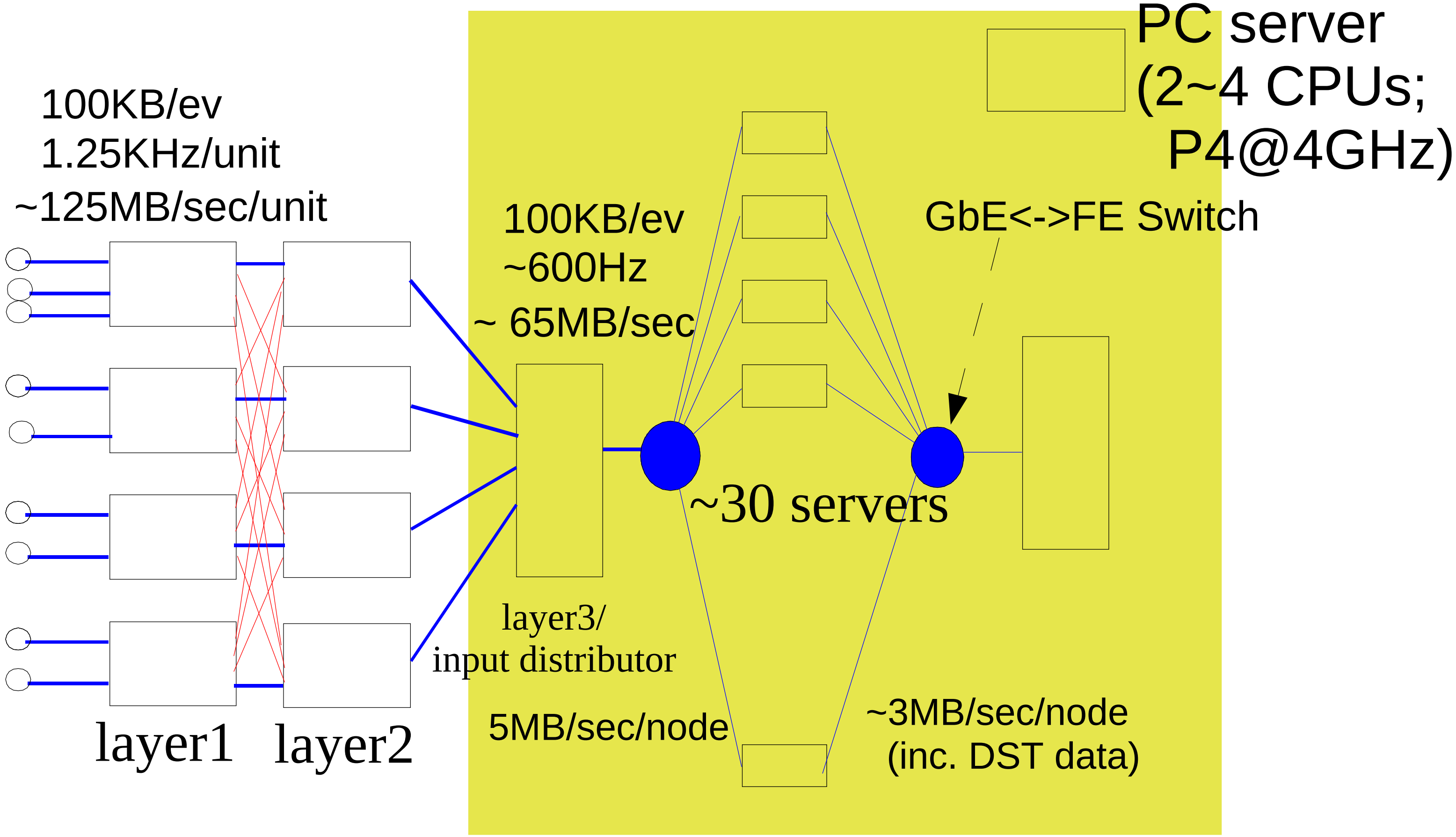


x 10

* BASF framework running on all nodes
* Level 2.5 trigger software on E1 node
* Event rejection at E2 node

Level 3 Trigger Farm

* Full event reconstruction capability is necessary to achieve ultimate data reduction.
* A PC cluster is connected to event builder output.



1 Unit → processing power for L=$10^{34}/cm^2/sec$

Storage

Belle: Currently using high speed tape device w/ robot(DTF/PetaSite)
* SONY gave up to release faster DTF drives
* market is small → expensive

- Recent disks are much faster than tape drive
    * ex. Dell/EMC CX600 / Fujitsu ETERNUS
        - 200MB/sec (2Gbps FiberChannel I/F)
            * preliminary test (Dell CX600) shows
              >100MB/sec read/write speed
              cf. DTF : 24MB/sec

↓

Record data on disk directly. Multiple data streams.

→ R&D has been started with Computing people.

4. Data reduction

- Data Reduction is very important in high-intensity experiments to keep mass-storage manageable.
- We need a versatile and powerful software trigger /event size reduction scheme to obtain reduction factor of <1/10 after L1 trigger.

1) Level 2 trigger (on CoPPER modules)

- event trigger after pipeline readout
- trigger signal is genarated by dedicated hardware(ex. Z-trigger by SVD fast readout)
  -> latency < ~50μsec (cf. L1 latency : ~10μsec)
- trigger signal is distributed to CoPPER via timing logic with event tag
- software running on CoPPER CPU rejects the event by looking at the trigger event tag

Trigger rate reduction : ~1/3-1/5 (30~50KHz -> 10KHz)
Event size reduction : 1 (~200-300 KB)

2) Event processing on CoPPER/Readout PC

CoPPER : linux-operated PC on board
$\rightarrow$ possibility of versatile event data processing

- Software data sparcification
  * Feature extraction for wave-form sampling
  * Event size compression by various method
    (bit-squeezing, zip, etc.)

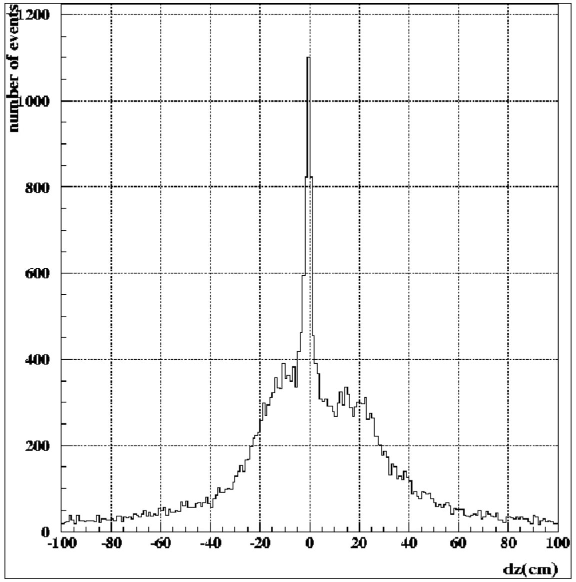
- Raw Data Formatting (to Panther / ROOT I/O (?))

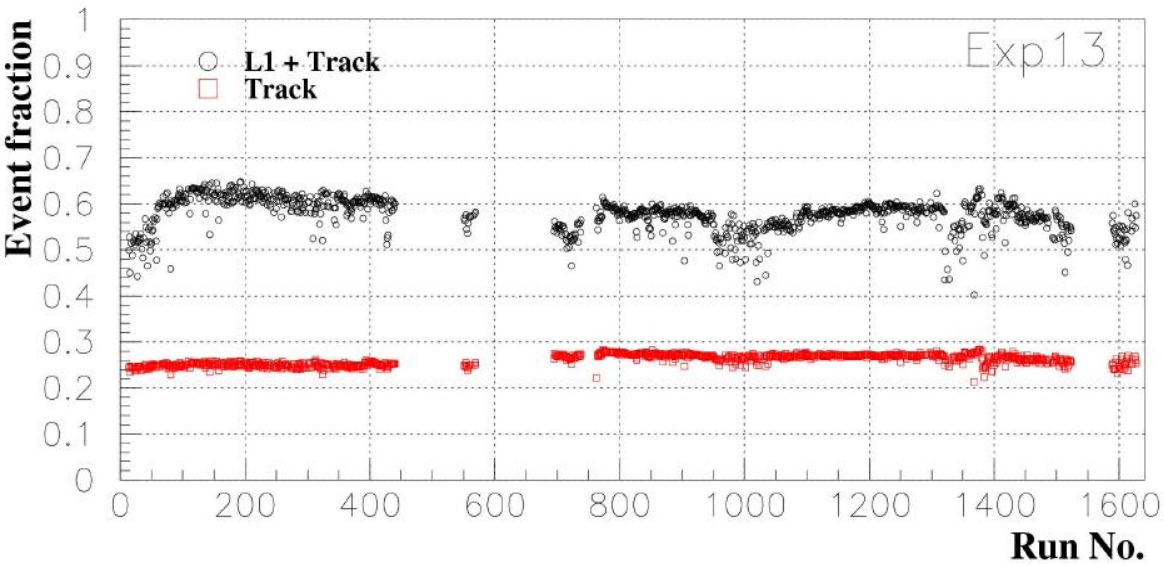
Trigger rate reduction : 1 (10KHz)
Event size reduction : 1/3 (~200 KB->100KB)

3) Level 2.5 trigger

- Software trigger using partially-built event data
  (data from one subdetector/several related subdetectors)
- Current Belle's "L3" scheme can be used

* Fast Tracking + Hardware trigger information (Belle)





Trigger rate reduction : 1/2 (10KHz->5KHz)
Event size reduction : 1

4) Level 3 trigger

- Software trigger using fully-built and fully-reconstructed data
- Trigger at a level of "Physics Skim"
  - * hadronic event selection
  - * selection of specially-interested events

Power of event reduction by "physics skim" at Belle

	Fraction in events after L2.5
Hadronic	14.2%
$\tau^+\tau^-$/2photon	9.6%
Monitor(=e^+e^-,$\mu^+\mu^-$,etc)	~1% (can be scaled)

Trigger rate reduction : 1/4 (~2KHz)
Event size reduction : 1 (+ reconstruction info(~100KB/ev))

* Data flow rate will increase by a factor of 2
  if we leave reconst. info together on storage
  $\rightarrow$ requires more multiplicity in storage

5. Summary

Trigger/DAQ for SuperKEKB are being designed based on

* "Tight" L1 trigger strategy based on Belle's

* Timing Distribution based on multi-level tree structure utilizing
a high-speed serial bus on LVDS

* Pipeline Readout implemented on a Common Readout Platform
FINESSE + CoPPER

* Multi-step event building based on the "switchless event building"

Data Reduction is performed by multi-step software trigger

- Level 2 on CoPPER	~30KHz->10KHz
- Event processing on CoPPER/PC	300KB/ev -> 100KB/ev
- Level 2.5 on event building farm	10KHz -> 5KHz
- Level 3 on Reconstruction (L3) farm	5KHz -> ~2KHz

Backup Slides

Physics Processes

Process	C.S. (nb)	R @ 10^{34} (Hz)	R @ 10^{35} (Hz)
Upsilon(4S)	1.2	12	120
Continuum	2.8	28	280
$\mu\mu$	0.8	8	80
$\tau\tau$	0.8	8	80
Bhabha	44	4.4	44
$\gamma-\gamma$	2.4	0.24	2.4
Two photon	15	35	350
Total	67	96	960

- Cross-sections are calculated in acceptance
- Bhabha and $\gamma-\gamma$ are pre-scaled by factor 100
- Two photon is with pt>0.3 GeV cut

ECL Trigger (B.G.Cheon)

Trigger bit	Rate @ 10^{35}
E_{TOT}>0.5GeV	6.5K
E_{TOT}>1.0GeV	3.4K
E_{TOT}>3.0GeV	2.5K
ICN bit-0	18.0K
ICN bit-1	5.0K
ICN bit-2	0.5K
ICN bit-3	0.2K
Bhabha	5.0K
Pre-Bhabha	1.5K
Cosmic	38.0K
CsI timing	110.0K

- Extrapolated by Lum.
- TC pulse width : 1us
  - TC occupancy < 10KHz @ 1035
- Current L1 trigger system may be kept.
  → Too optimistic ???
  → Beam BG level ???
- More simple/fast/flexible system against $>10^{35}$

Design Concept of Backend DAQ

- Multi-stage event building and selection
  "Build and select" scheme at each level of event building

- Versatile and powerful level 3 trigger farm
  -> "Full event reconstruction" is performed
  to obtain ultimate data reduction factor

- Maximum use of existing technology
  * Switchless event building technology
  * NSM based control

- Common software framework at all levels
  * BASF + Panther is used from CoPPER to L3 farm
  * Full use of Belle Software Library
  <- the same software environment as that in offline
  => easy development of data reduction software