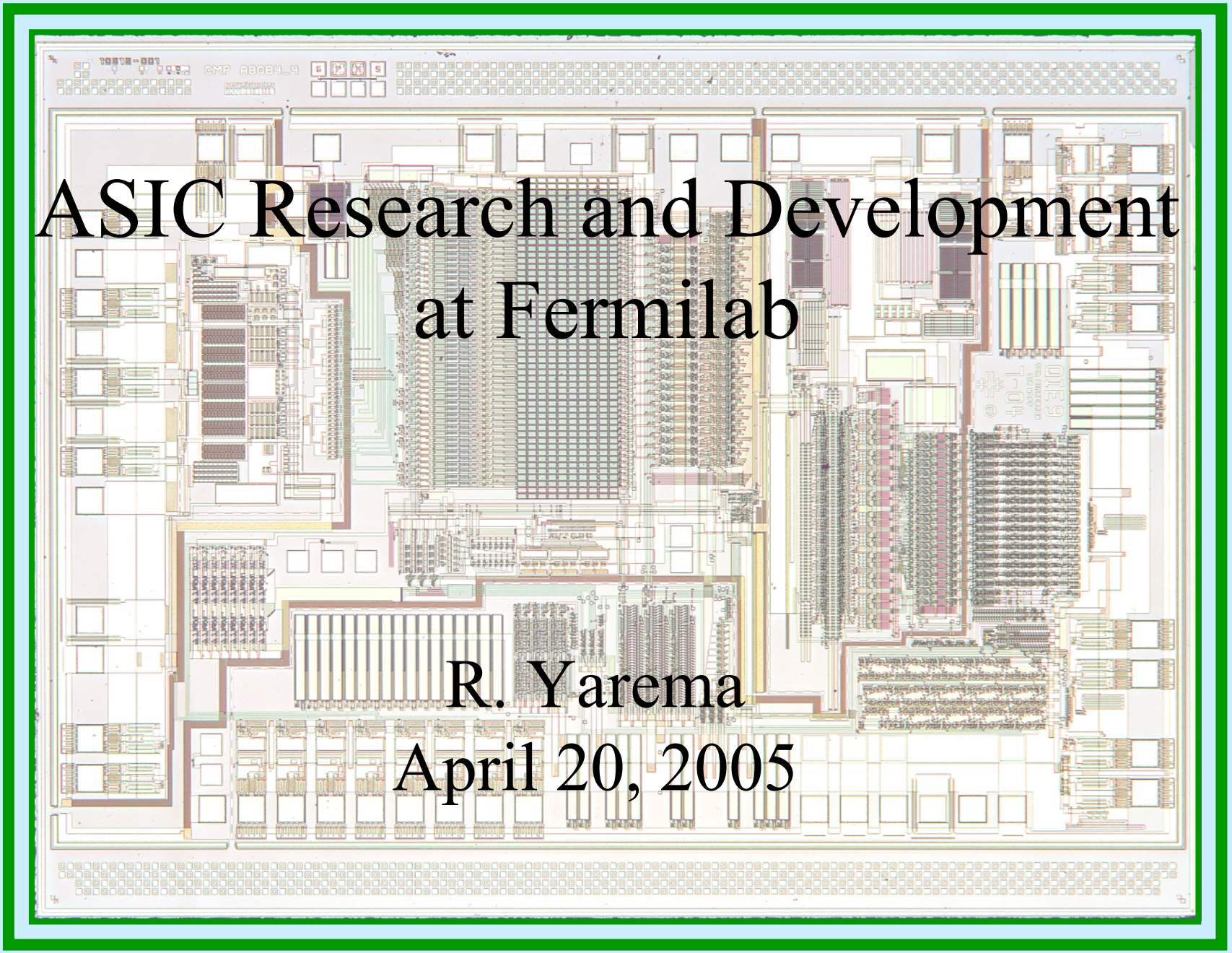


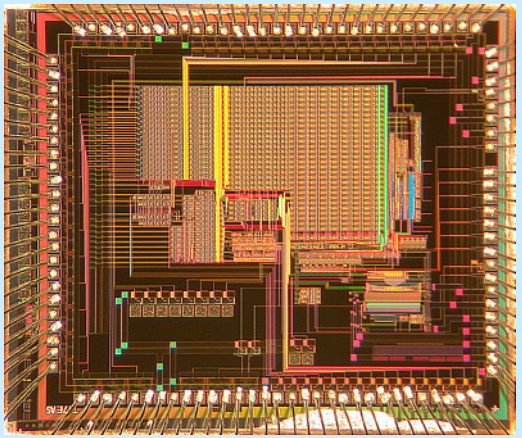
ASIC Research and Development at Fermilab

R. Yarema

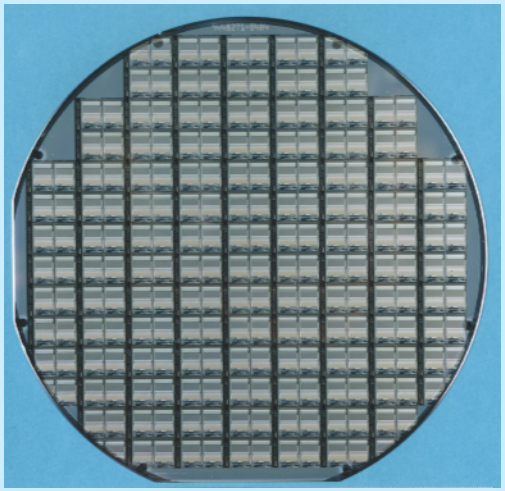
April 20, 2005

Main areas

- ASIC R&D happening in EED of PPD where we have capabilities and experience in several diverse areas.
- ASIC design at many silicon foundries
  - TSMC
  - IBM
  - AMS
  - Agilent
  - Atmel



- ASIC in-house testing
  - Wafer level testing
  - Packaged parts testing
- Board level design



Current Activities

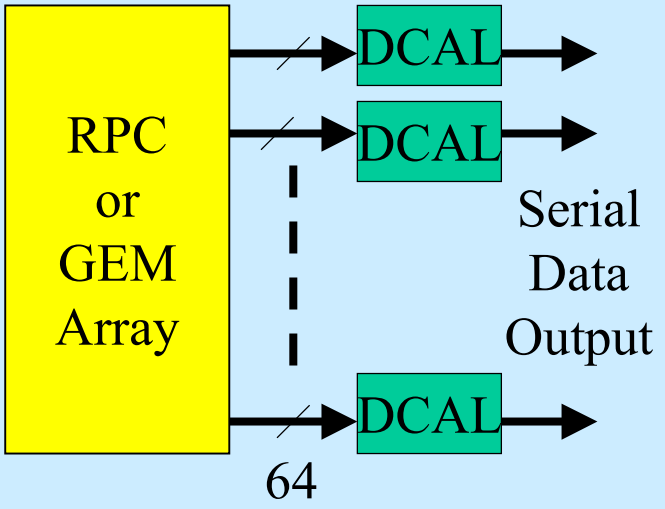
- 9 ASICs currently in design, fabrication, or under test.
  - Readout chip for Resistive Plate Chambers (RPCs) and Gaseous Electron Multipliers (GEMS)
  - Readout chip for Avalanche Photo Diodes (APDs)
  - Readout chip for Visible light Photon Counters (VLPCs)
  - Readout chip for Photomultiplier Tubes (PMTs)
  - Controller chip for Cockcroft Walton power sources
  - TDC for straw detectors
  - Readout chip for pixel detectors
  - Readout chip for silicon strip detectors
  - Evaluation chip for 0.13 micron CMOS process
- Discuss each device briefly to give over view of design capabilities - perhaps find new device for your experiment.

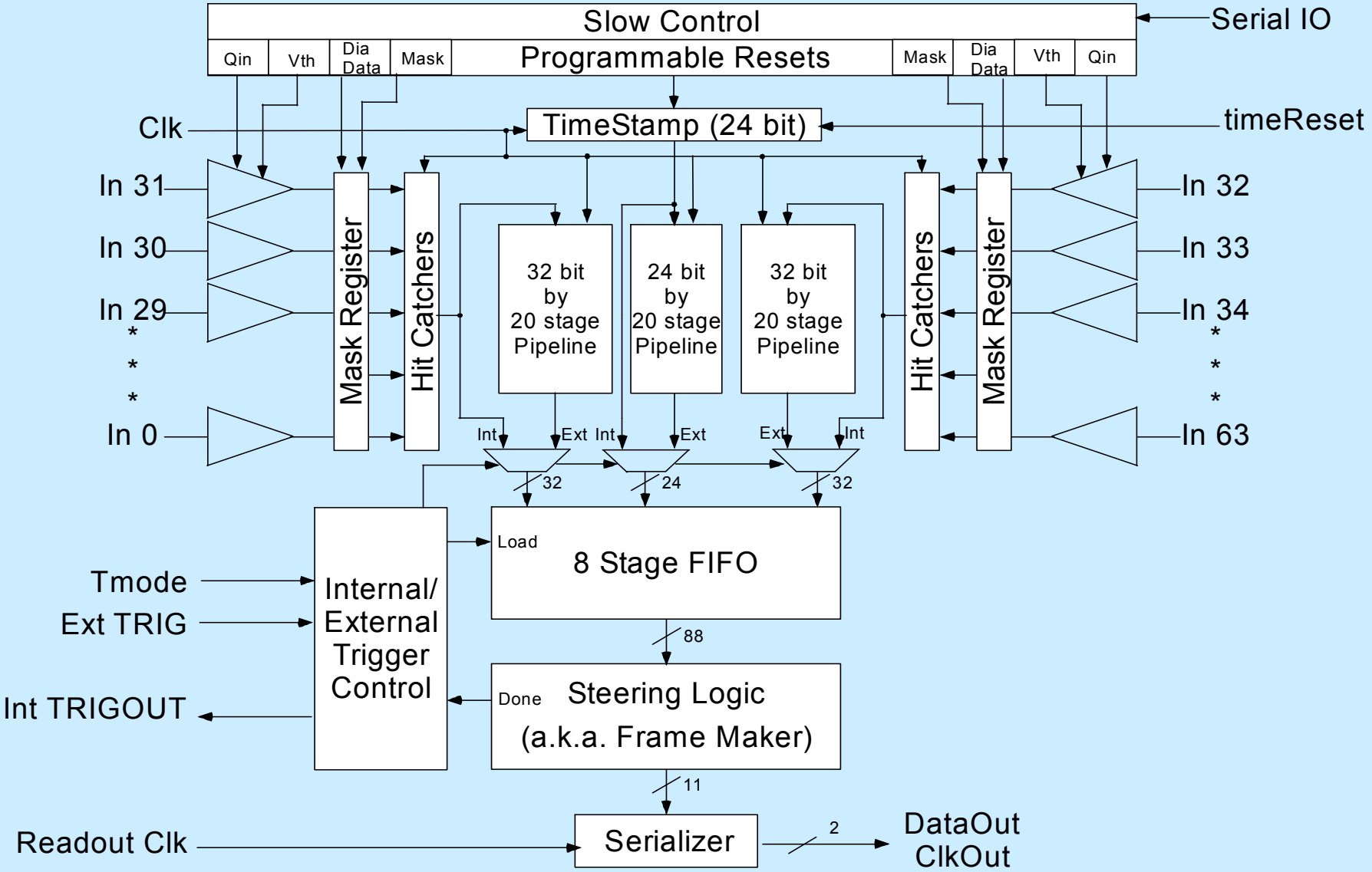
DCAL chip

- Digital hadron calorimeter readout chip for CALICE collaboration
- Designed for Fermilab test beam to prove digital calorimeter concept.
- 1 m^3, 400,000 channel detector
- Chip designed to operate with RPCs and GEMs
- RPCs used many places (Belle, etc.) GEMs are relatively new.
- Design to be refined for ILC beam structure at a later time.
- Chip is in fabrication (TSMC 0.25 micron CMOS)

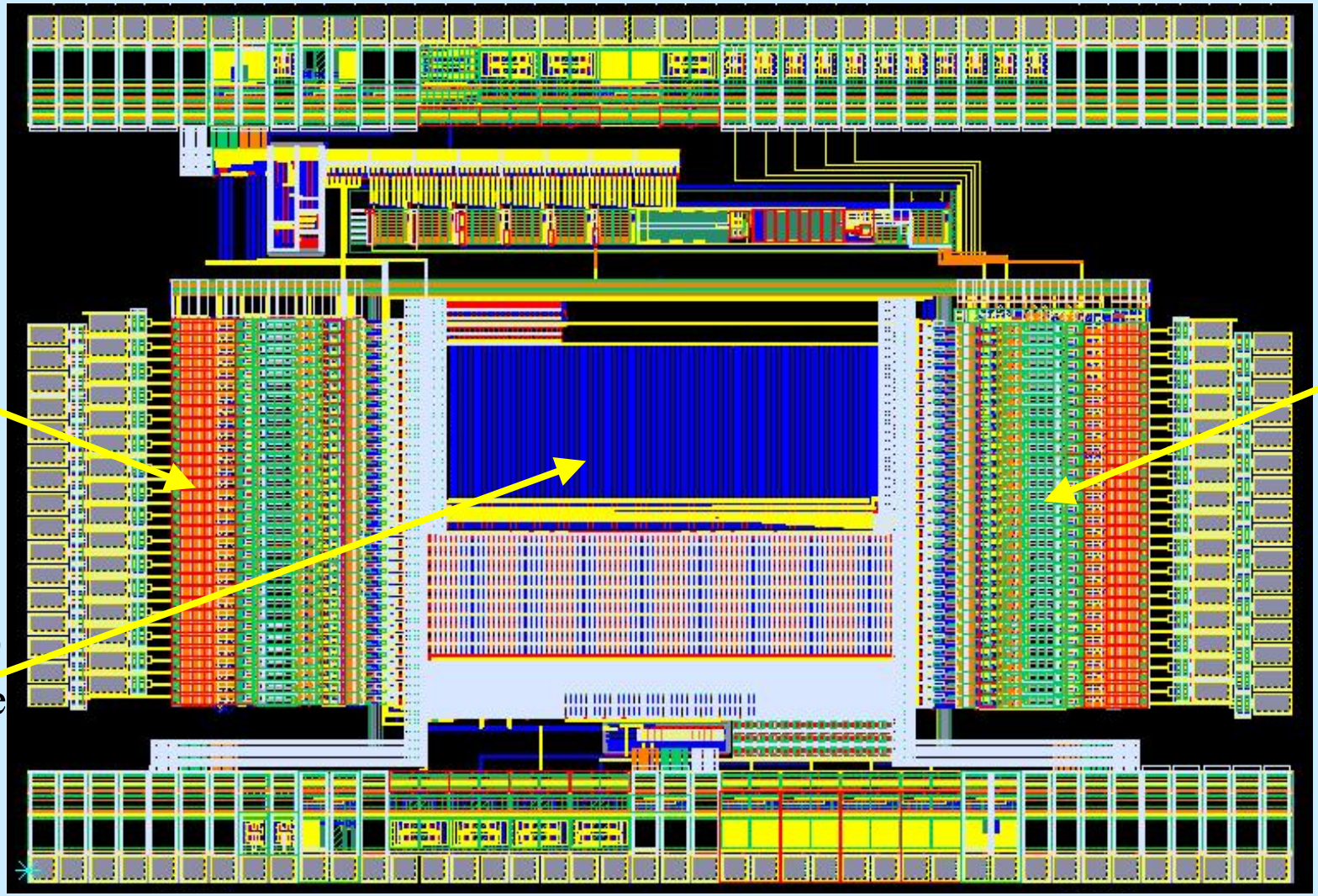
DCAL Specifications

- 64 channels/chip
- 1 cm x 1 cm pads
- Detector capacitance, 10 to 100 pf
- Smallest input signal, 100 fC (RPCs), 5 fC (GEMs)
- Largest input signal, 10 pC (RPCs), 100 fC (GEMs)
- Chip has adjustable gain for RPCs and GEMs.
- Signal pulse width, 3-5 nsec
- Trigger less or triggered operation
- 100 nsec clock cycle
- Serial output data – hit pattern and time stamp




Slow Control
Serial IO
Qin
Vth
Dia Data
Mask
Programmable Resets
Mask
Dia Data
Vth
Qin
Clk
TimeStamp (24 bit)
timeReset
In 31
In 30
In 29
In 0
In 32
In 33
In 34
In 63
Mask Register
Hit Catchers
32 bit by 20 stage Pipeline
24 bit by 20 stage Pipeline
32 bit by 20 stage Pipeline
Hit Catchers
Mask Register
Int
Ext
Int
Ext
Ext
Int
32
24
32
Load
8 Stage FIFO
Tmode
Ext TRIG
Internal/ External Trigger Control
88
Int TRIGOUT
Done
Steering Logic
(a.k.a. Frame Maker)
11
Readout Clk
Serializer
2
DataOut
ClkOut

DCAL Layout

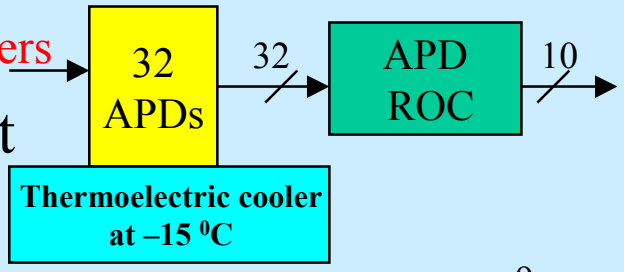


Avalanche Photo Diode Readout Chip

- Chip designed to readout APDs in the proposed NOvA (Neutrino off axis) experiment at Fermilab.
- Design based on previous FNAL chips: SVX4, MASDAX.
- Chip is designed for in–spill data taking from Fermilab neutrino beam and for trigger less operation to search for supernova events and to collect cosmic ray data.
- Low noise operation is one of the major problem.
- Chip design is complete in TSMC 0.25 micron mixed signal CMOS
- Layout is in progress.

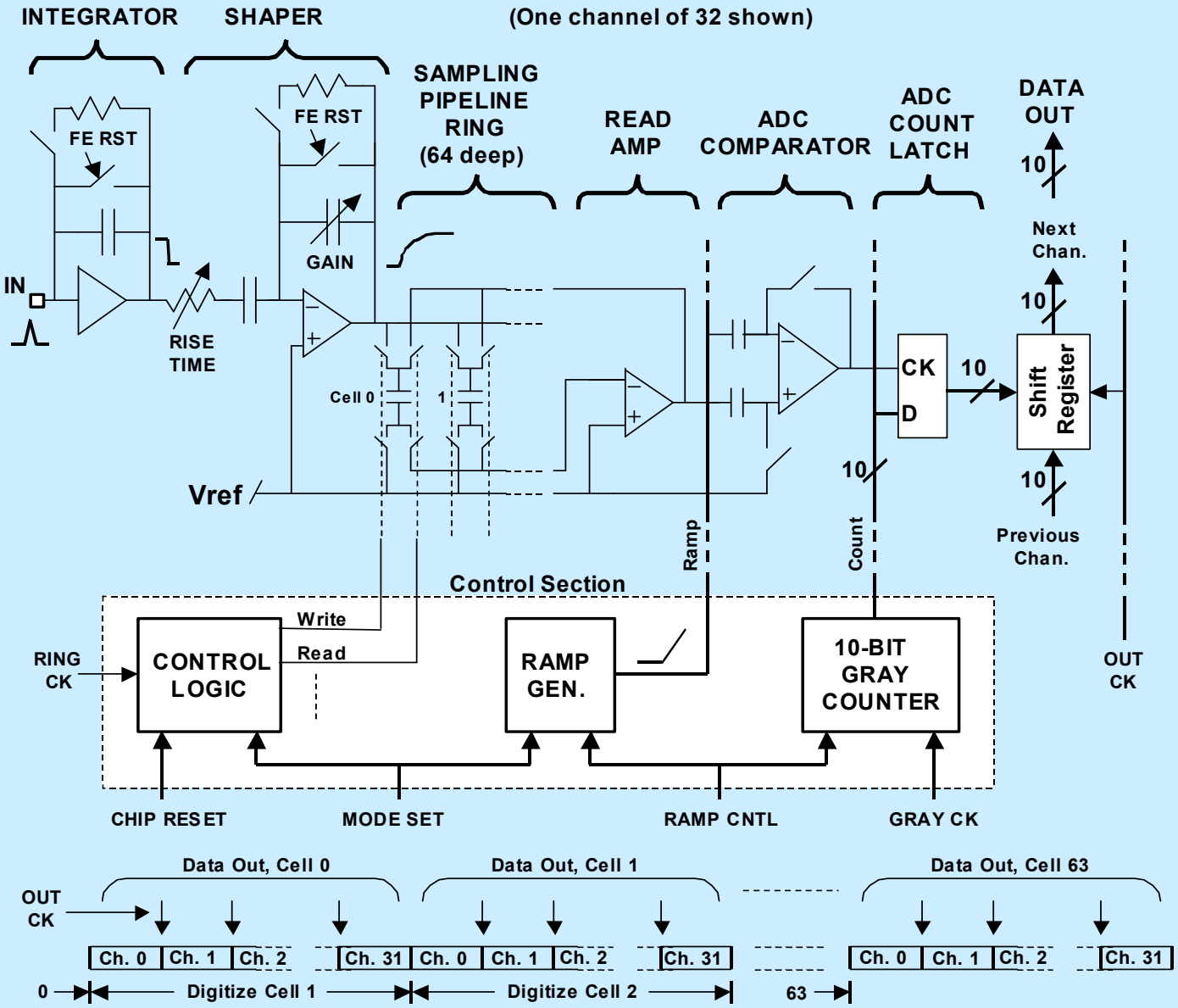
APD ROC Specifications

- 32 channels/chip
- APD is run at 400 V to give a gain of 100 and provide signals of 2500 e (min) to the APD readout chip.
- Detector capacitance = 10-15 pF
- Noise of readout chip = 200 erms max at 10 pF.
- First stage: high gain preamplifier with a shaping time of about 350 nsec.
- 64 stage switched capacitor array clocked at 500 nsec.
- Double correlated samples to reduce noise (various options)
- 10 bit Wilkinson ADC with linear or pseudo-log ramp
- Triggered or trigger less mode
- 10 bit serial-parallel output data format



APD READOUT CHIP

(One channel of 32 shown)



Front end reset modes:

1. Switched
2. Continuous

Pipeline modes:

1. Triggered
   (Write - Stop - Read)
2. Continuous
   (no deadtime)

Ramp modes:

1. Linear
2. Pseudo-log

Digitize modes:

1. Cell only (0, 1, ...)
2. DCS (1-0, 2-1, ...)
3. DCS every other
   (2-0, 3-1, ...)

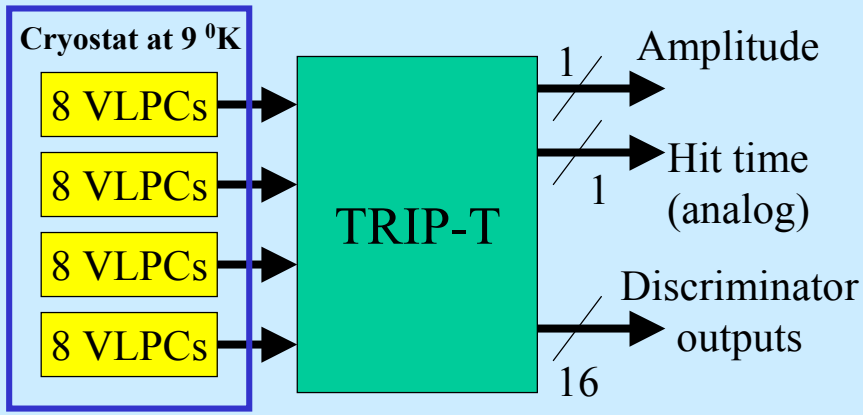
DATA OUT format example:
Cell only digitize mode
(10-bit DATA words)

TRIP-T

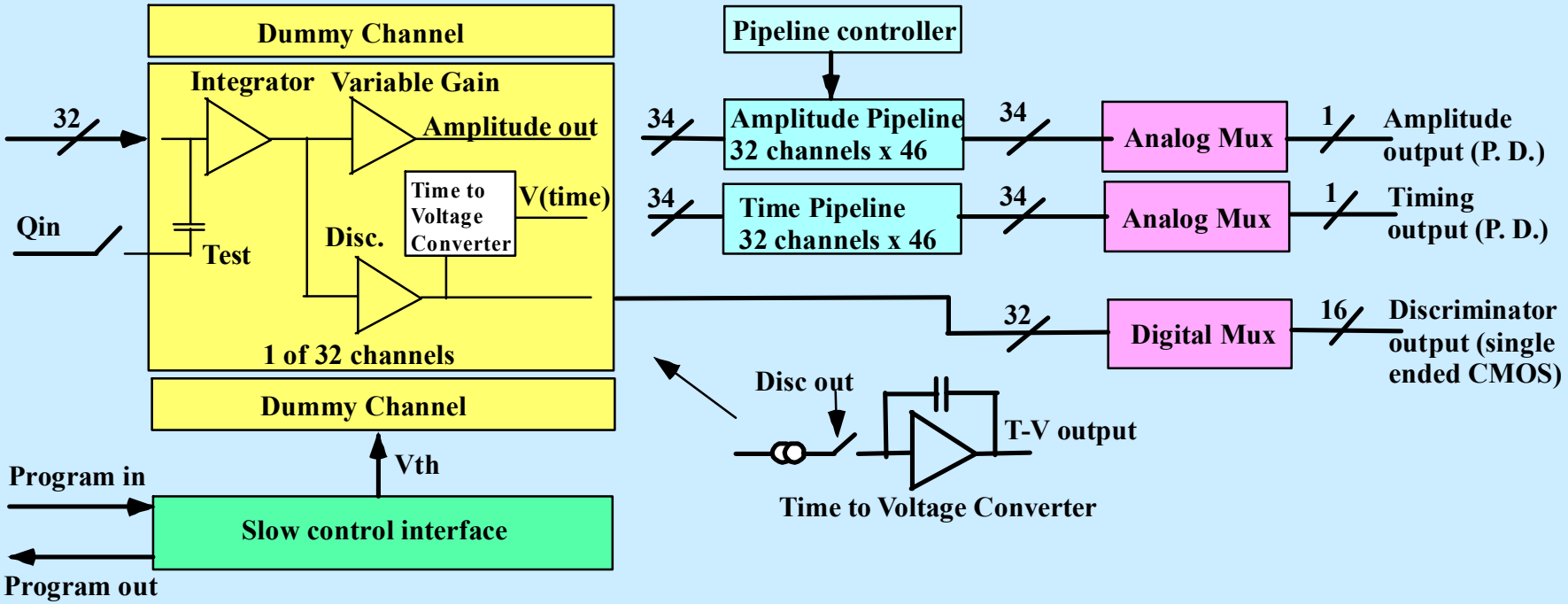
- The TRIP-T chip is a multi-channel front-end chip that has a preamplifier, a fast trigger output, and an analog pipeline for the VLPC based central scintillating fiber tracker and pre-shower detectors at Dzero.
- Performs 3 functions
  - Detect and send hit information to trigger system every beam crossing.
  - Store analog signal level in pipeline for readout and digitization later.
  - Store arrival time of hit within within 100 nsec integration window for readout and digitization later.
- The chip is expected to also be used by the proposed Minerva neutrino experiment.
- Chip is designed and layout is finished.
- To be submitted about May 15 to TSMC 0.25 micron CMOS process.

TRIP-T Specifications

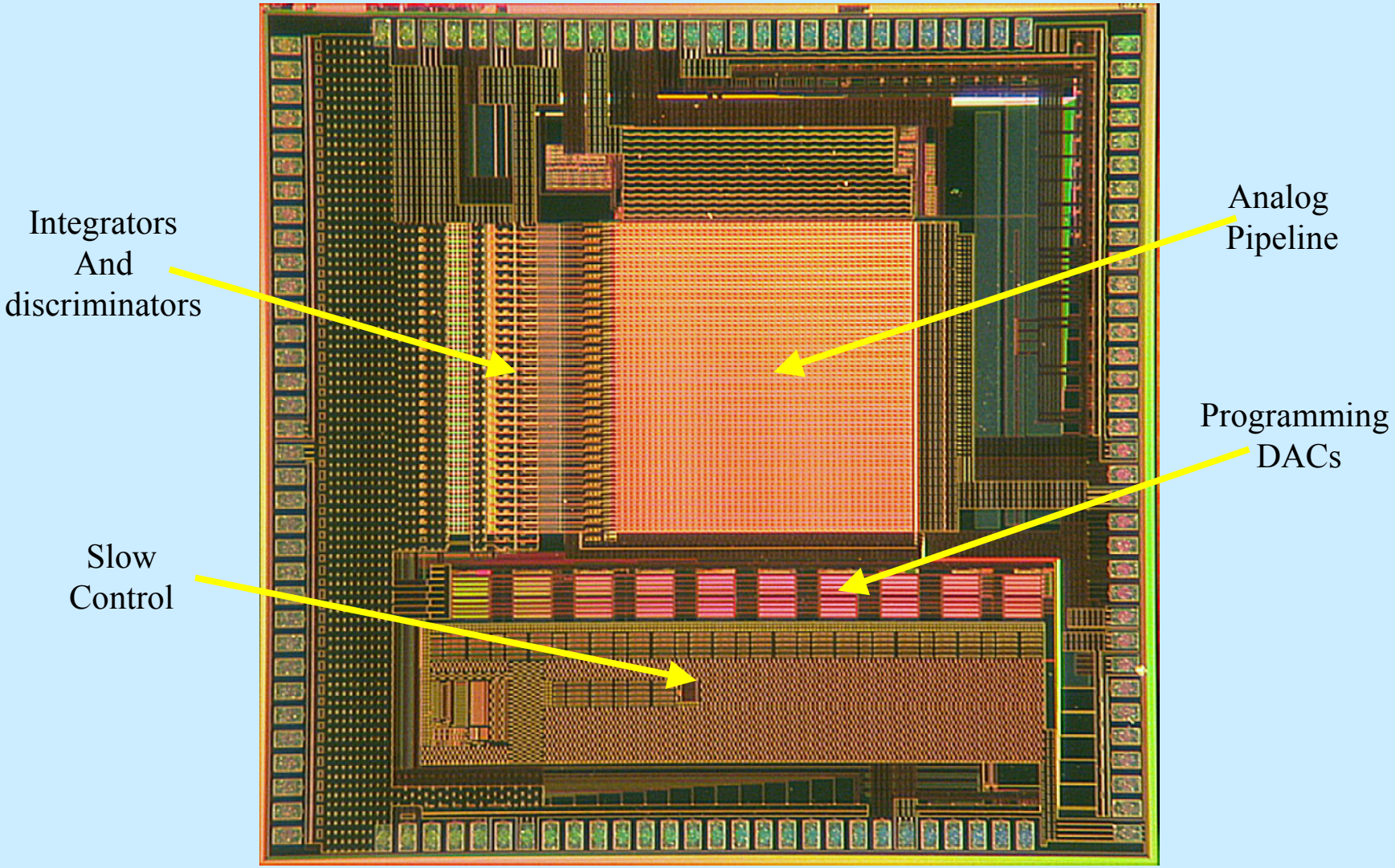
- 32 channels per chip
  - 32 discriminator outputs
    - Multiplex 32 signals to 16 output lines each clock cycle
  - 46 cell deep, analog pipeline; read out after trigger
    - Pipelined amplitude output to ADC
    - Pipelined time to voltage converter output to ADC
      - To provide 2 nsec resolution
- 396 nsec clock with 100 nsec signal integration
- Chip-wide programmable gain, and discriminator threshold control
- Input signal range:
  - 4 fC – 150 fC (high gain)
  - 1890 fC max (low gain)
- Analog ENC: < 1 fC rms.
- Detector capacitance: 35 pF



TRIP-T Block diagram

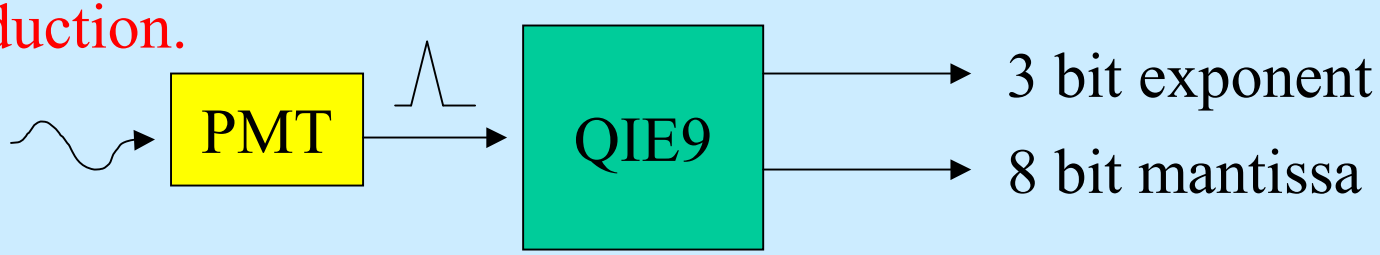


TRIP-T Chip


Integrators
And
discriminators
Analog
Pipeline
Programming
DACs
Slow
Control

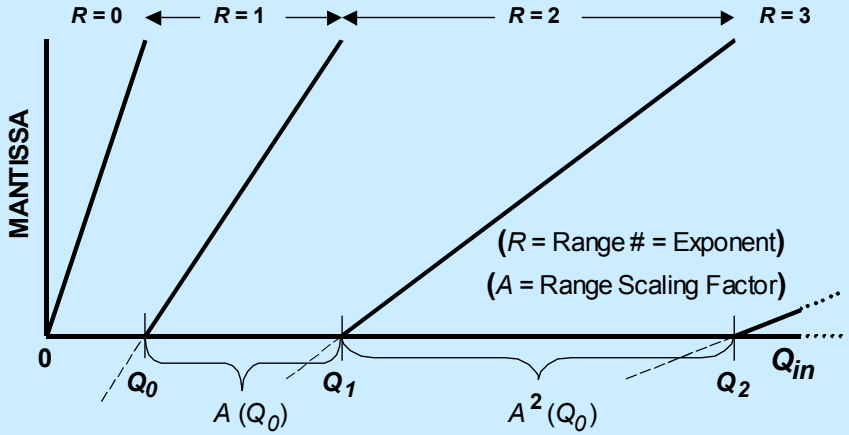
QIE9 (Charge Integrator and Encoder)

- QIE9 is the latest chip in a series of chips designed for several experiments: KTEV, CDF, CMS, MINOS, and BTEV. Devices designed for different signal ranges and speed.
- Device is used for digitizing signals that cover a wide dynamic range (16 bits) but need only limited resolution (8 bits).
- The QIE9 accepts charge from a PMT, splits the charge with a current splitter, integrates the charge on 8 binary weighted, parallel ranges, then digitizes the signal from the range of interest and outputs the input charge value as a modified floating point number. Data is processed internally in 3 stage pipeline.
- Prototyped in AMS 0.8 micron BiCMOS. Ready for production.

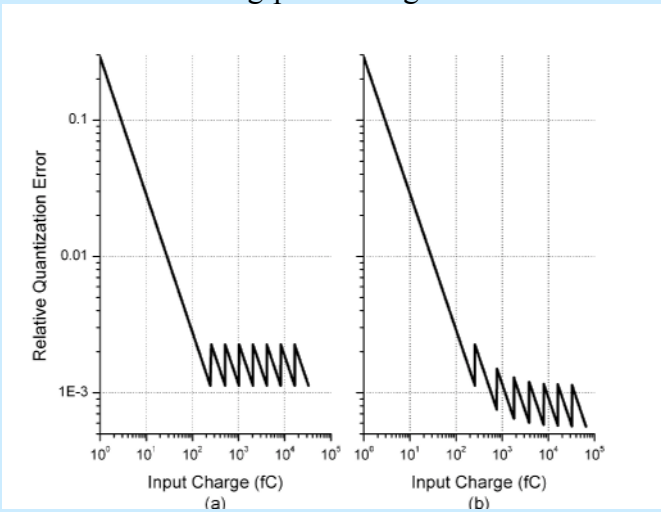


QIE 9 Specifications

Least count charge	**5 fC**
Max input charge	**300 pC**
Gated integration period	**132 ns**
Analog signal BW	**> 20 MHz**
Input impedance	**50 ohms**
Input noise charge (5 m cable)	**< 5 fC**
ADC DNL	**<< 1 LSB**
ADC INL	**< 1 LSB**
Resolution (relative error)	**<0.2% (for .2 pC inputs)**

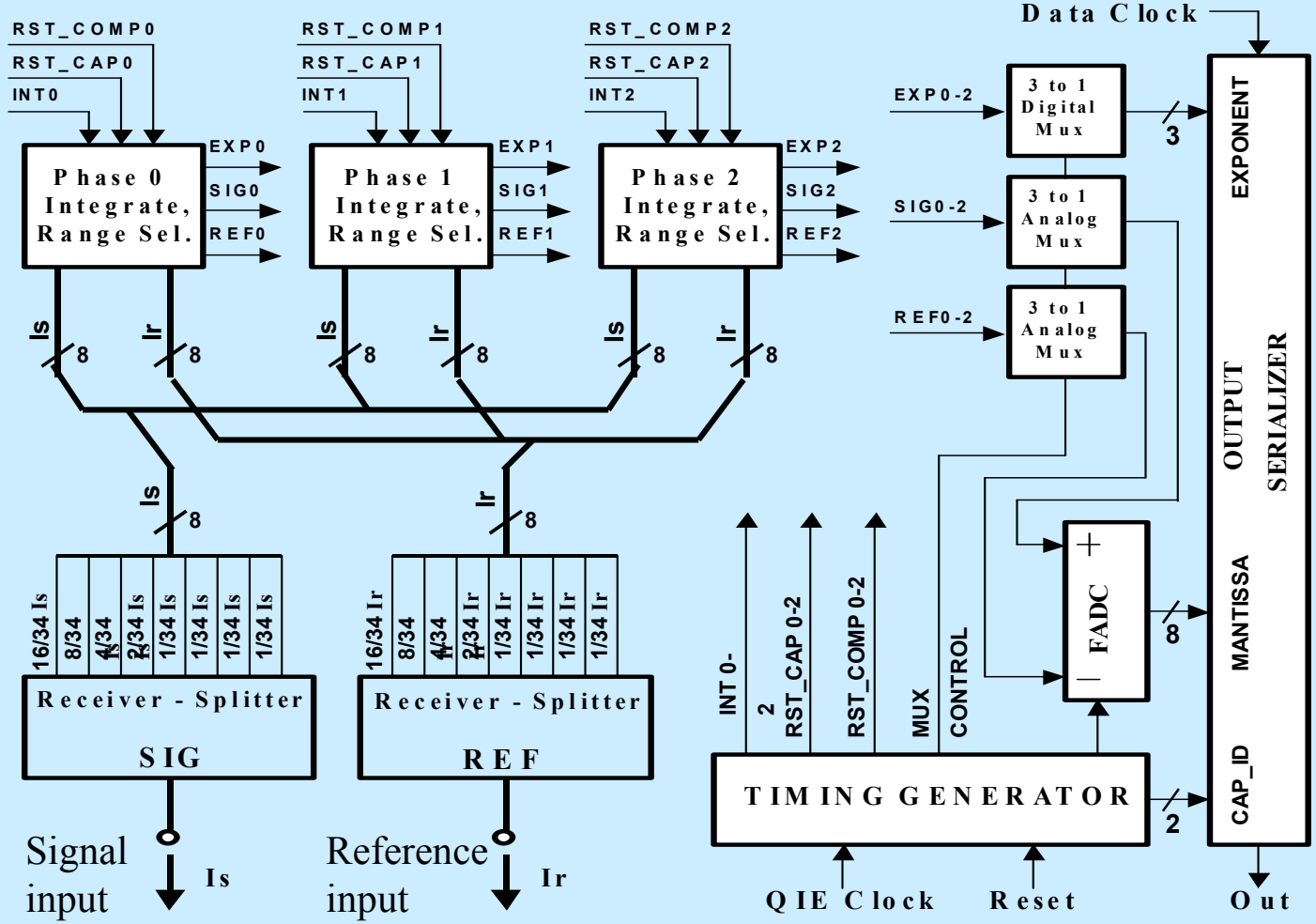


Typical modified floating-point charge transfer characteristic.

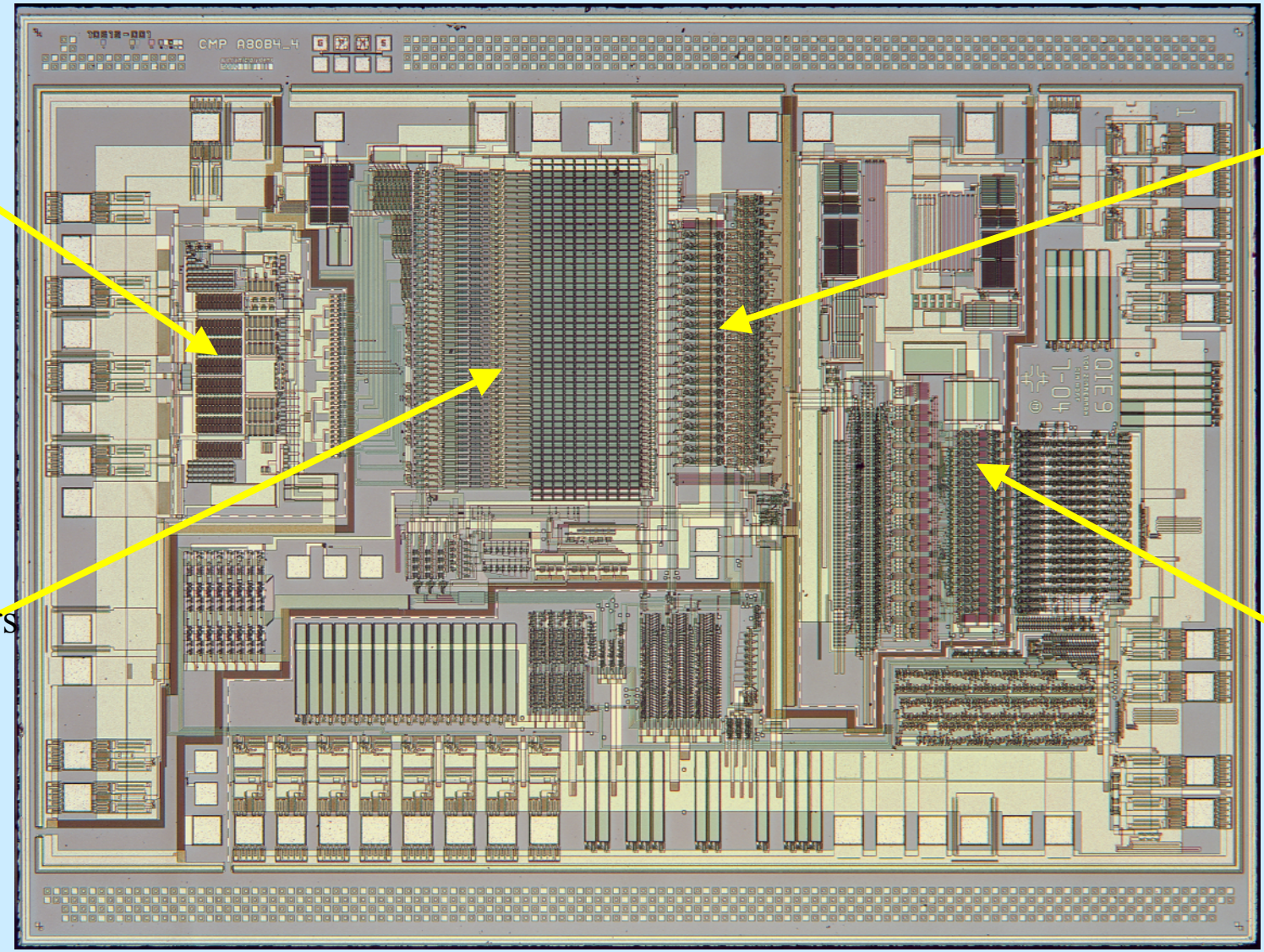


Relative error plots for (a) standard and (b) modified floating point.

QIE9 Block Diagram

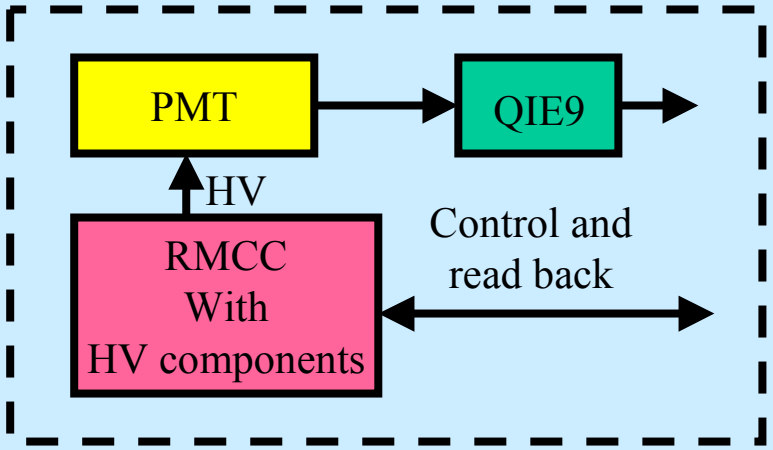


QIE9 Chip

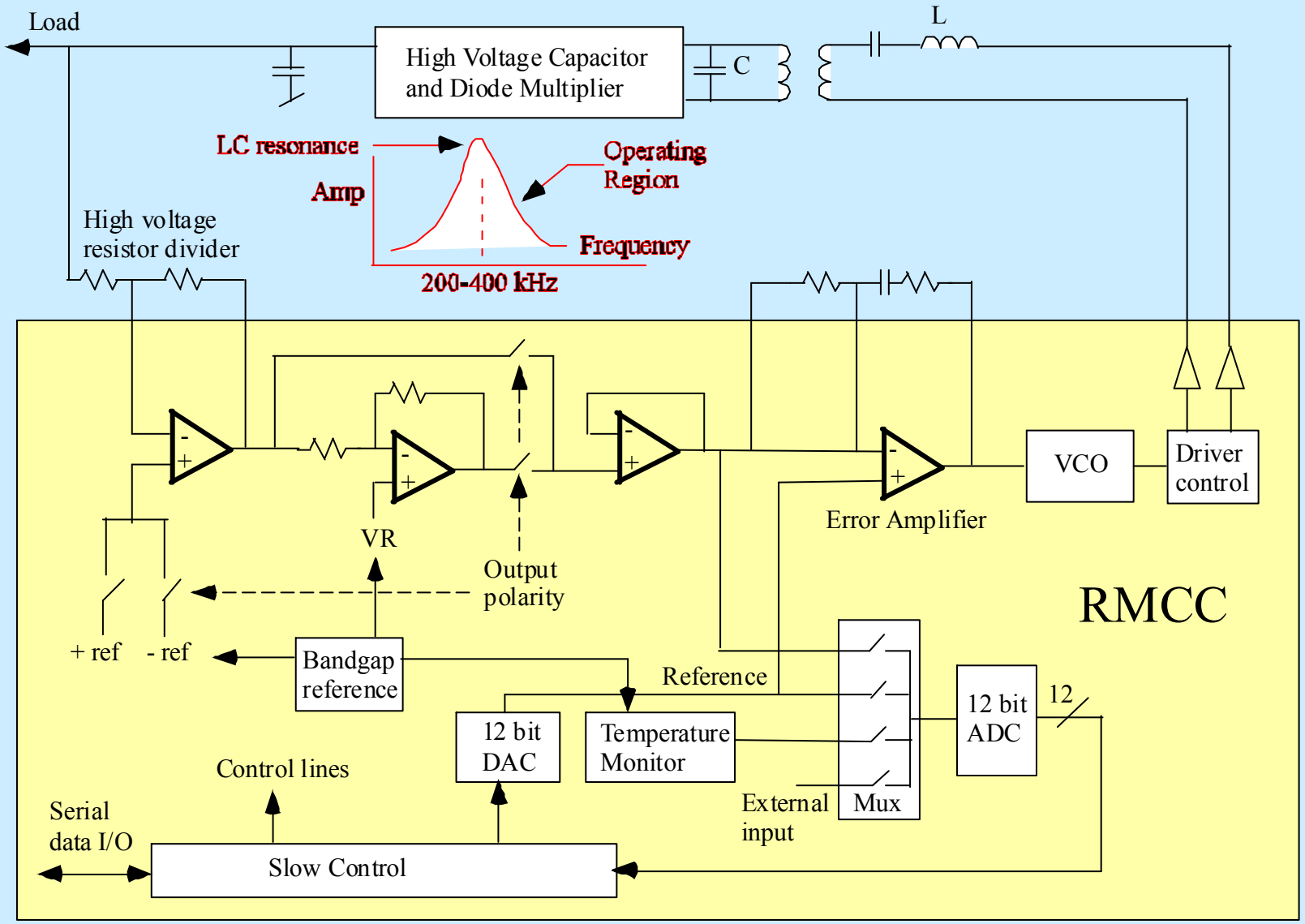

Input
Receiver/
splitter
Integrators
Range
select
8 bit
ADC

Resonant Mode Converter Controller (RMCC)

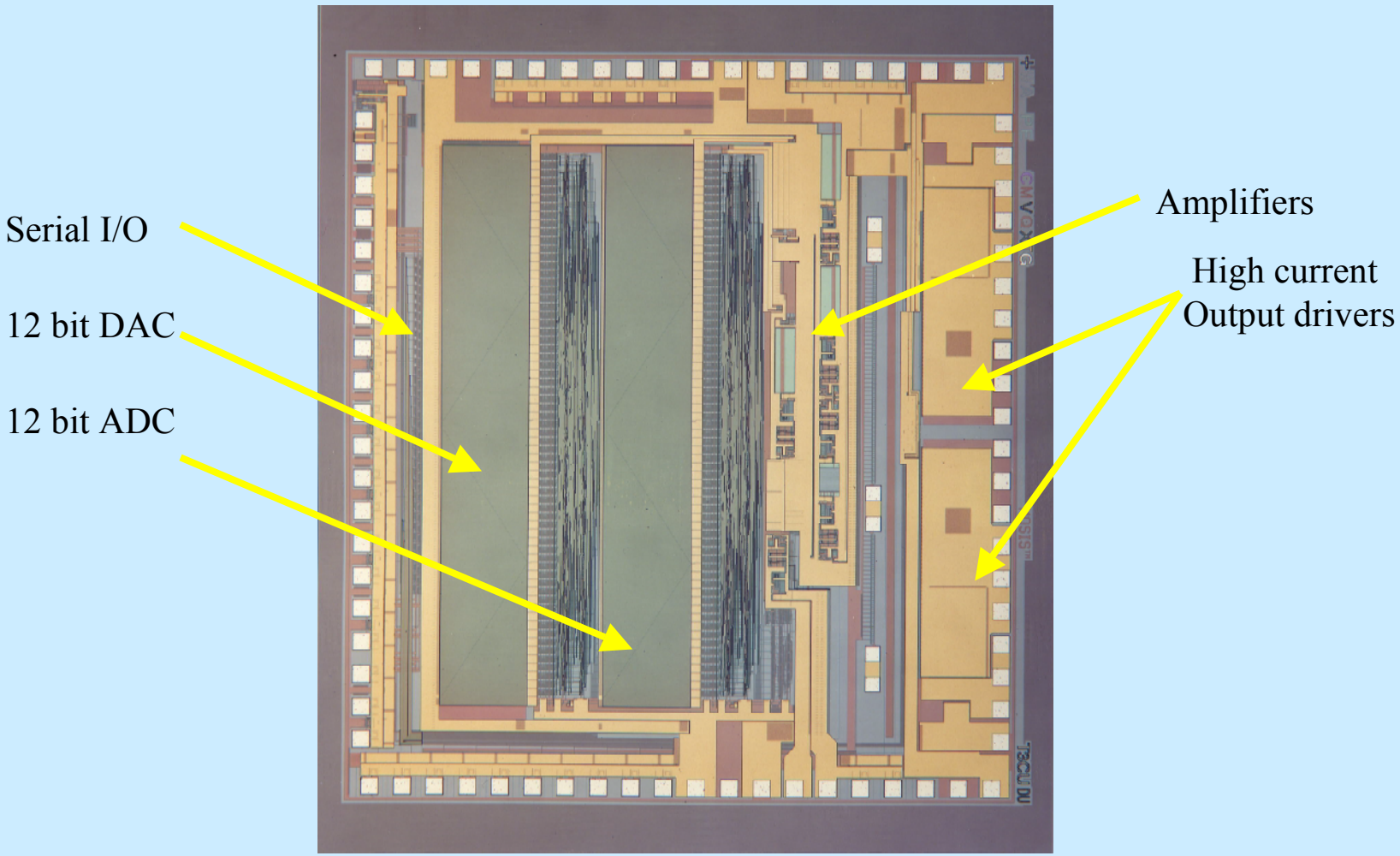
- Controller chip for Cockcroft-Walton type of high voltage supply.
- Power source for high voltage, low current detectors such as PMTs, pixel and strip detectors, APDs, etc.
- Advantages
  - Highly programmable
  - 12 bit ADC read back
  - Integrate power near detector
  - No H. V. connectors
  - Relatively low cost
- Prototype received
  - AMI 0.5 micron CMOS
- Testing 4 channel board



Cockcroft Walton Converter using RMCC

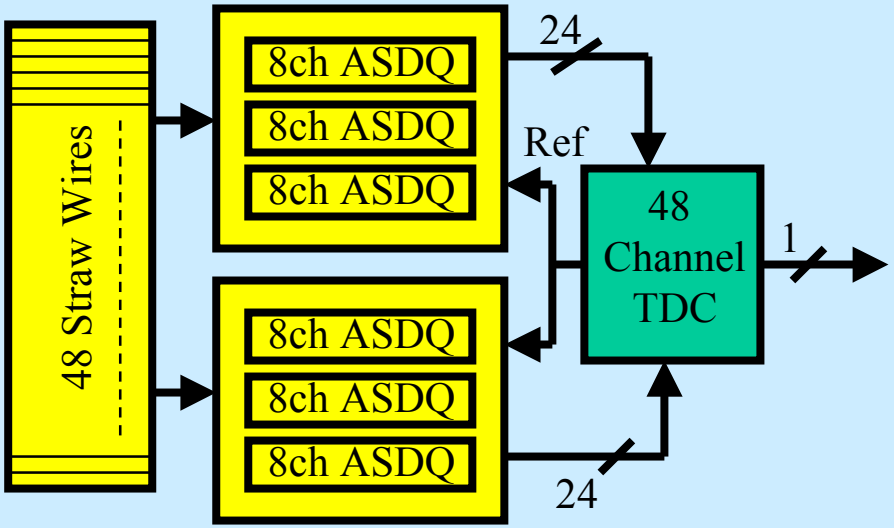


RMCC

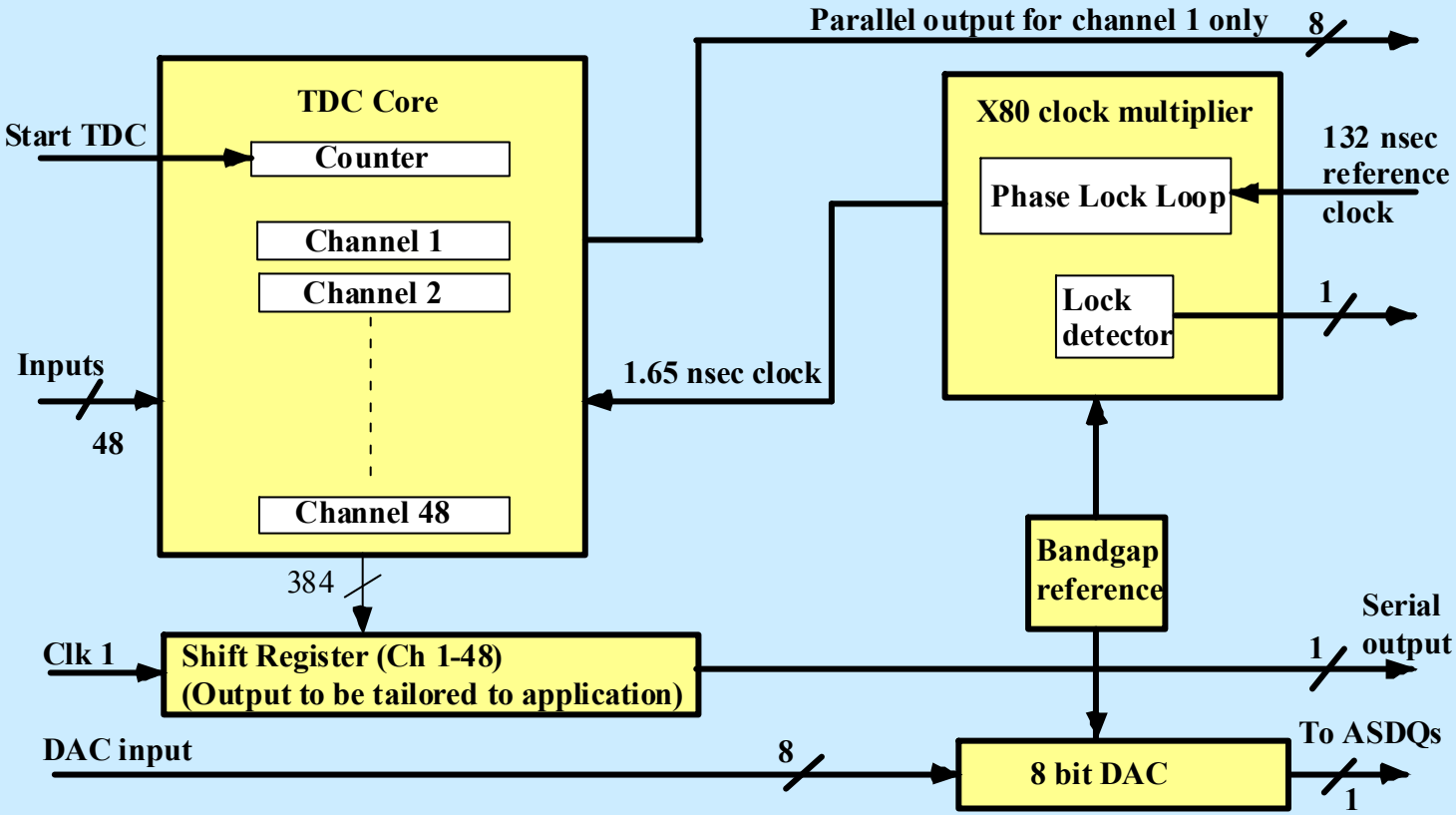

Serial I/O
12 bit DAC
12 bit ADC
Amplifiers
High current
Output drivers

Multi-channel TDC

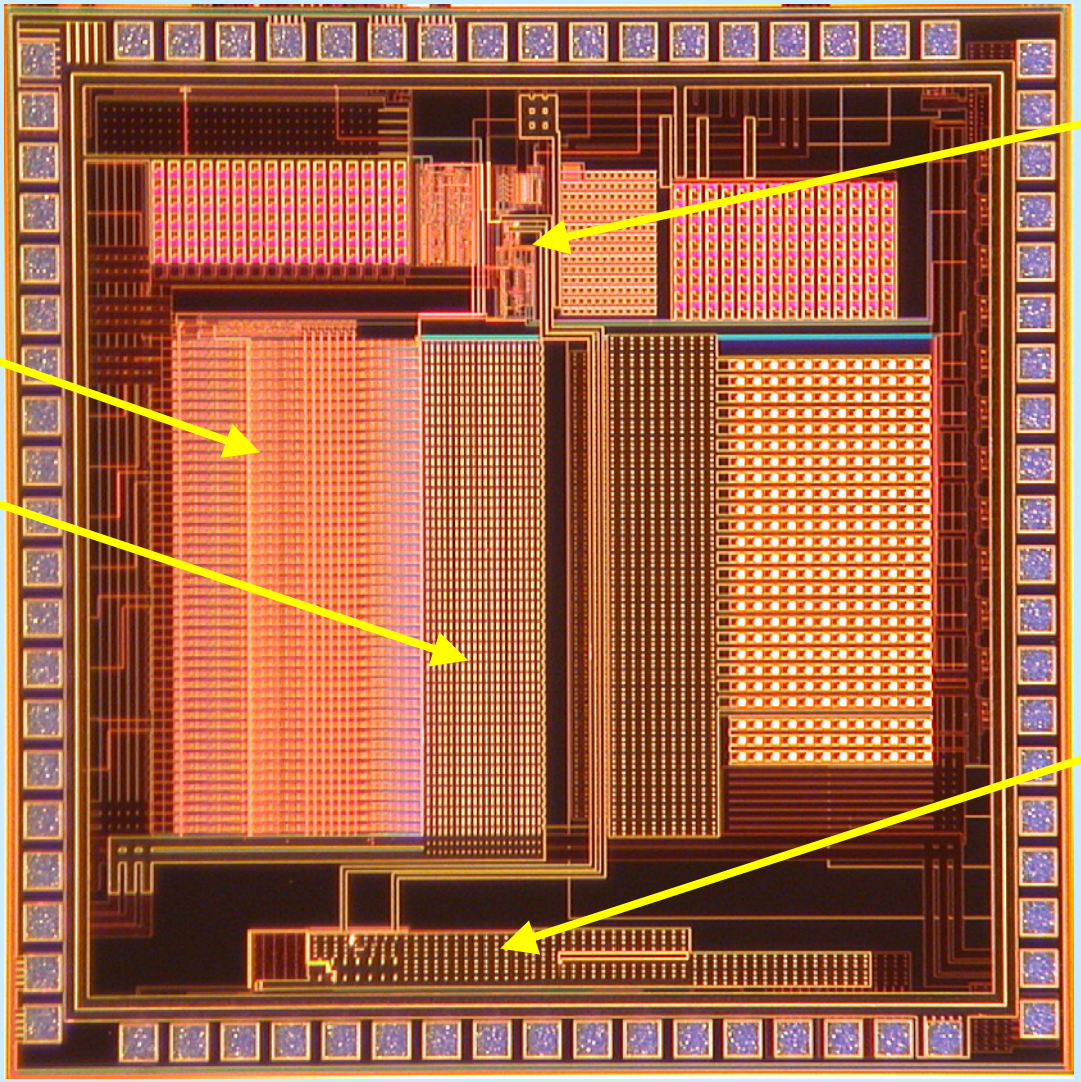
- Intended for use with straw detectors
- TDC features:
  - Radiation tolerant (TSMC 0.25 micron CMOS)
  - 48 channels
  - Serial CMOS output
    - To be tailored for application
  - 1.65 nsec resolution
  - Min. input PW = 10 nsec
  - On chip DAC reference for ASDQ chip
- Chip under test
  - Appears functional



Multi-channel TDC Block Diagram

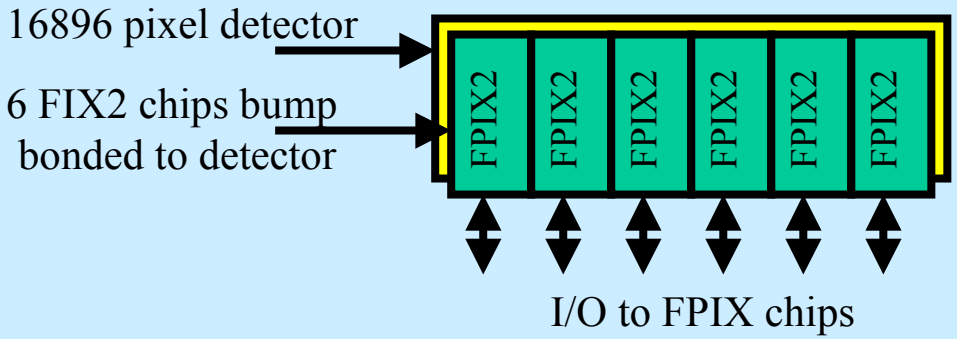


TDC Chip


Phase lock loop
48 TDC channels
Output Shift Register
8 bit DAC

FPIX2

- Pixel readout chip designed for the proposed BTEV experiment.
- May be used in Phenix upgrade at BNL
- Other applications being considered
- Design work complete
  - Final production version to be submitted about May 15



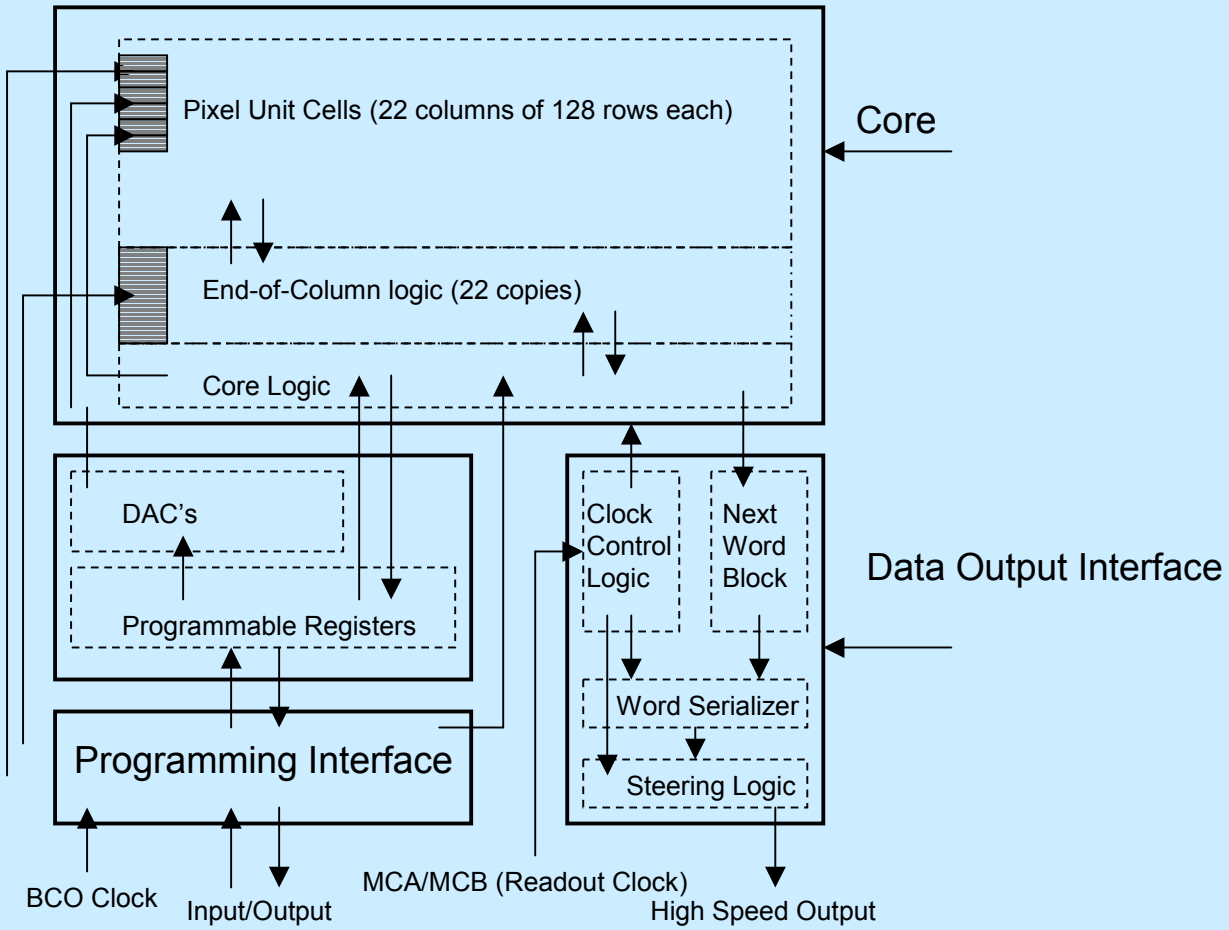
FPIX2 Specifications

- Pixel chip intended for use in Level 1 trigger (a first in HEP)
  - All hit information must be read out in 132 nsec
  - Zero suppressed data readout
  - 840 Mbit/sec readout capability (1-6 programmable serial outputs)
- 3 bit ADC in every pixel cell
- Low noise with detector (110 e rms)
- Low threshold dispersion with detector (250 e rms)
  - No individual pixel trim DACs
- Intended for 132 nsec beam interaction rate (can be run faster)
- 50 x 400 micron cells arranged in 22 columns by 128 rows
- Tolerates large leakage current (100 nA)
- Functionality is highly programmable
  - All adjustable parameters set to default values upon startup
- Radiation hard to > 30 Mrads.

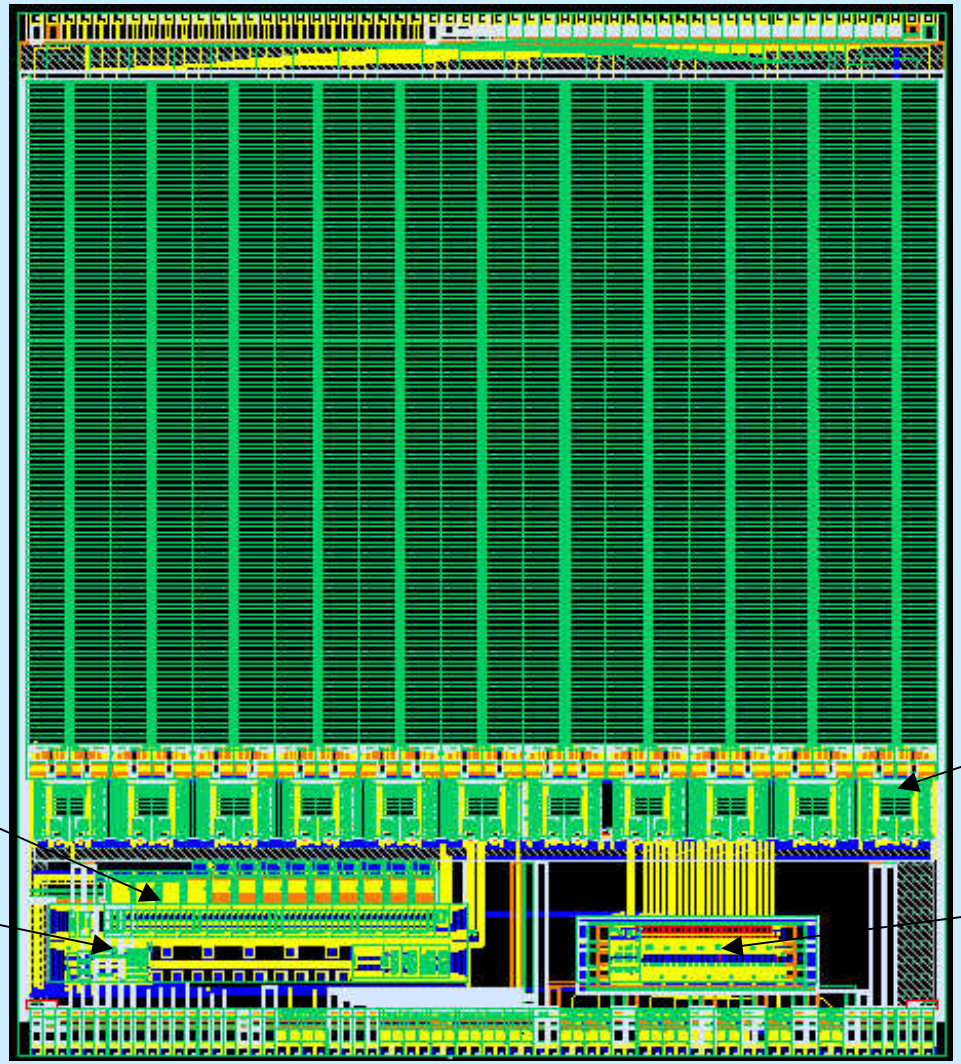
FPIX2 Block Diagram

Only bias voltages required are 2.5V & ground.

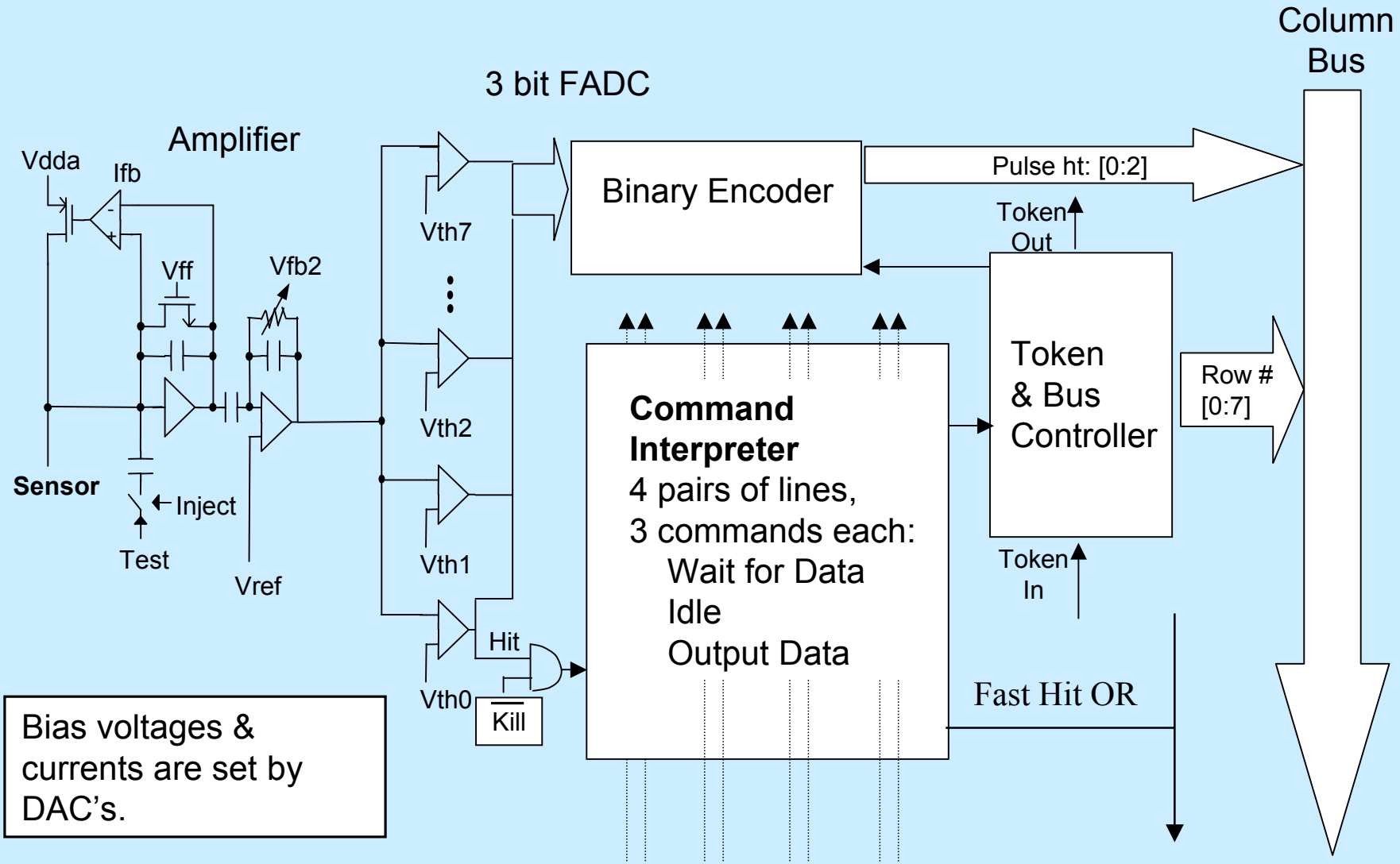
All I/O is LVDS.



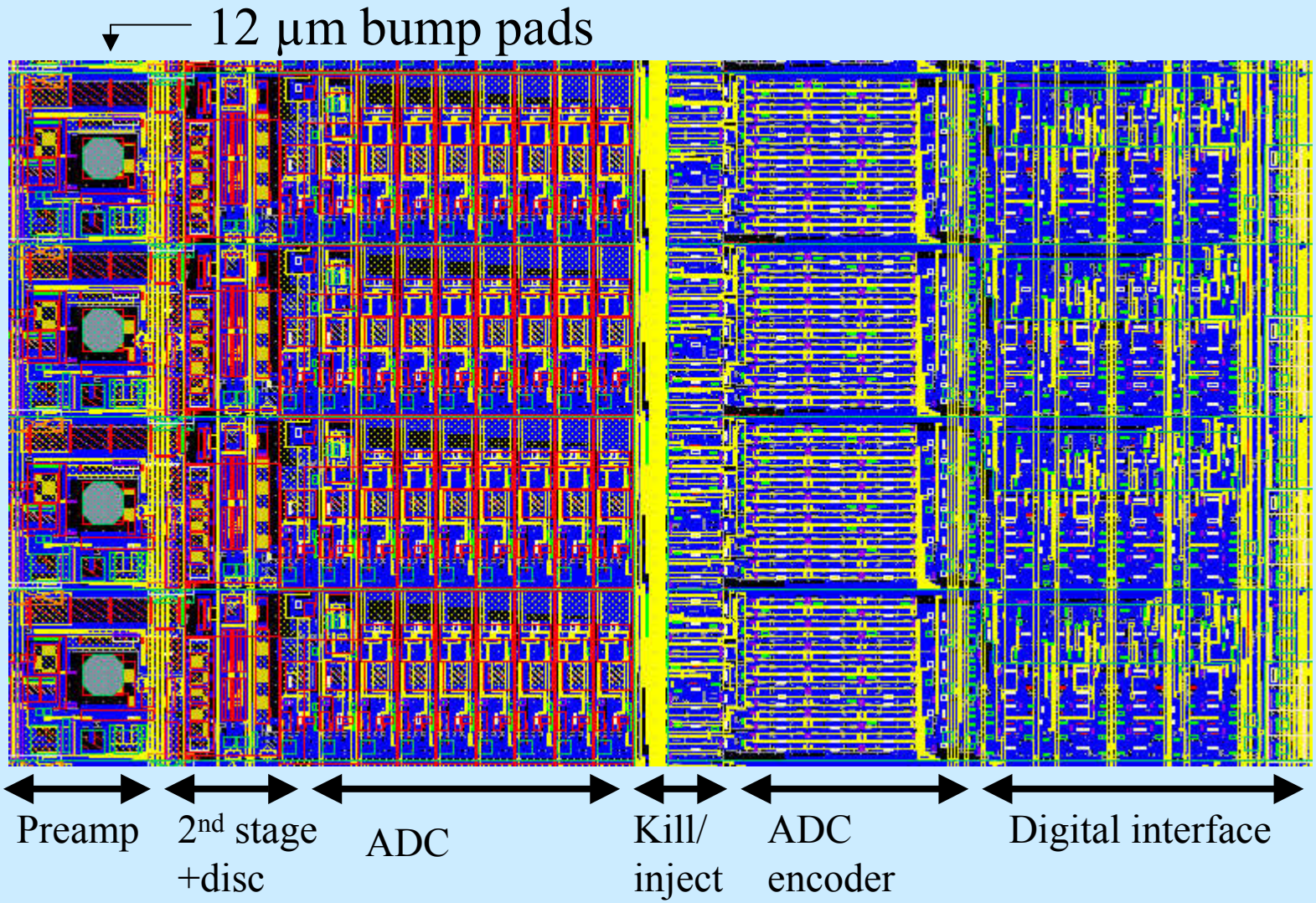
FPIX2 Layout



Pixel Unit Cell

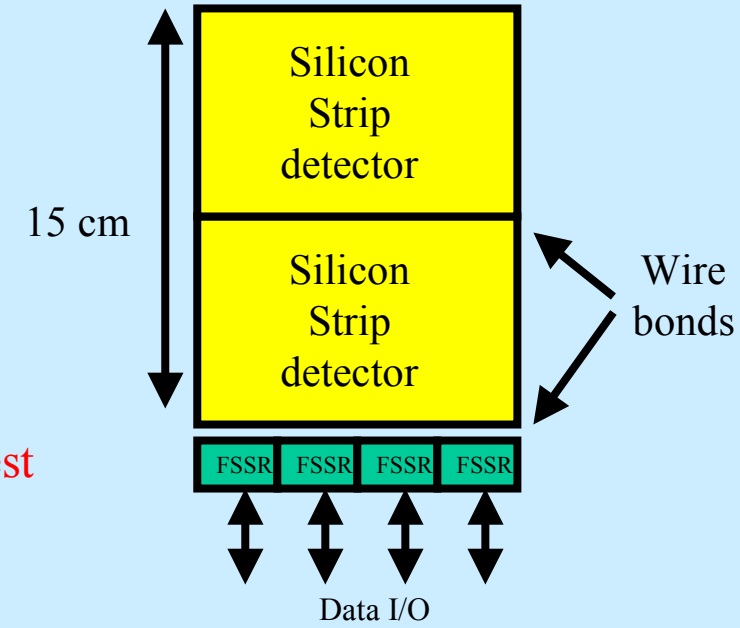


Layout of 4 pixels cells (50 μ x 400μ)



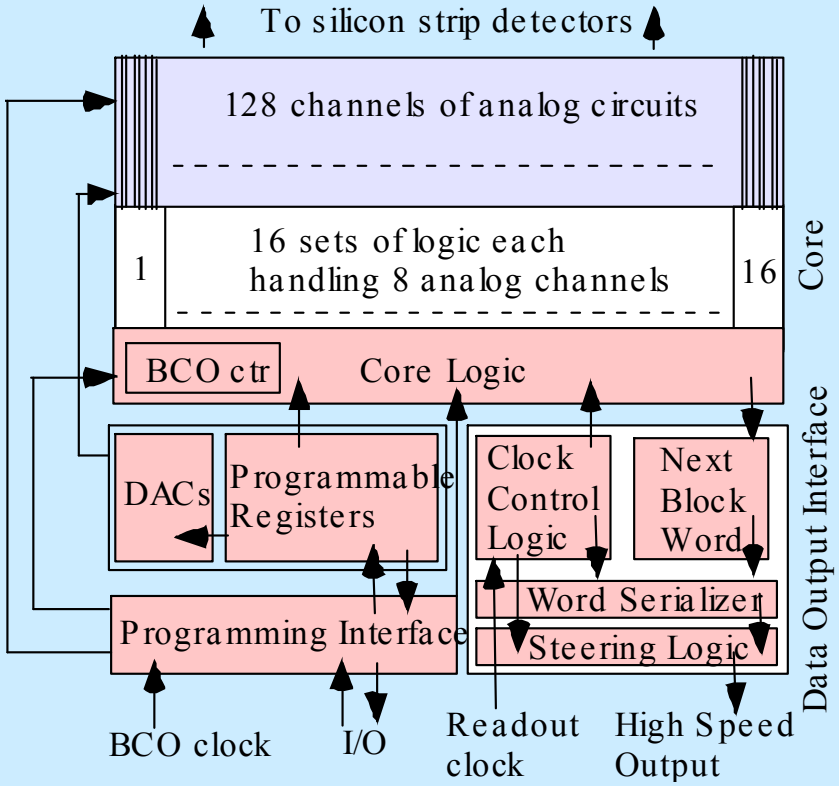
FSSR (Fermilab Silicon Strip Readout)

- Designed in collaboration with INFN personnel
- Originally planned for BTEV experiment
- Major requirements
  - Same programming interface and data output interface same as FPIX2
  - Data driven architecture – no trigger
  - Programmable shaping times (65-125 nsec) for 132, 264, or 396 nsec BCO
  - 128 channels/chip
  - ENC < 1000 erms @ Cdet=20 pF
    - Measured 220 e + 26 e/pF
  - Threshold dispersion < 500 erms
    - Measured 440 e rms
  - Programmable gain of 10 or 6.7mV/fC
  - 3 bit ADC/channel
  - Power < 4mw/channel
  - Detector inputs on 50 u pitch
  - Radiation hard (TSMC 0.25 µ CMOS)
- Pre-production parts received and under test

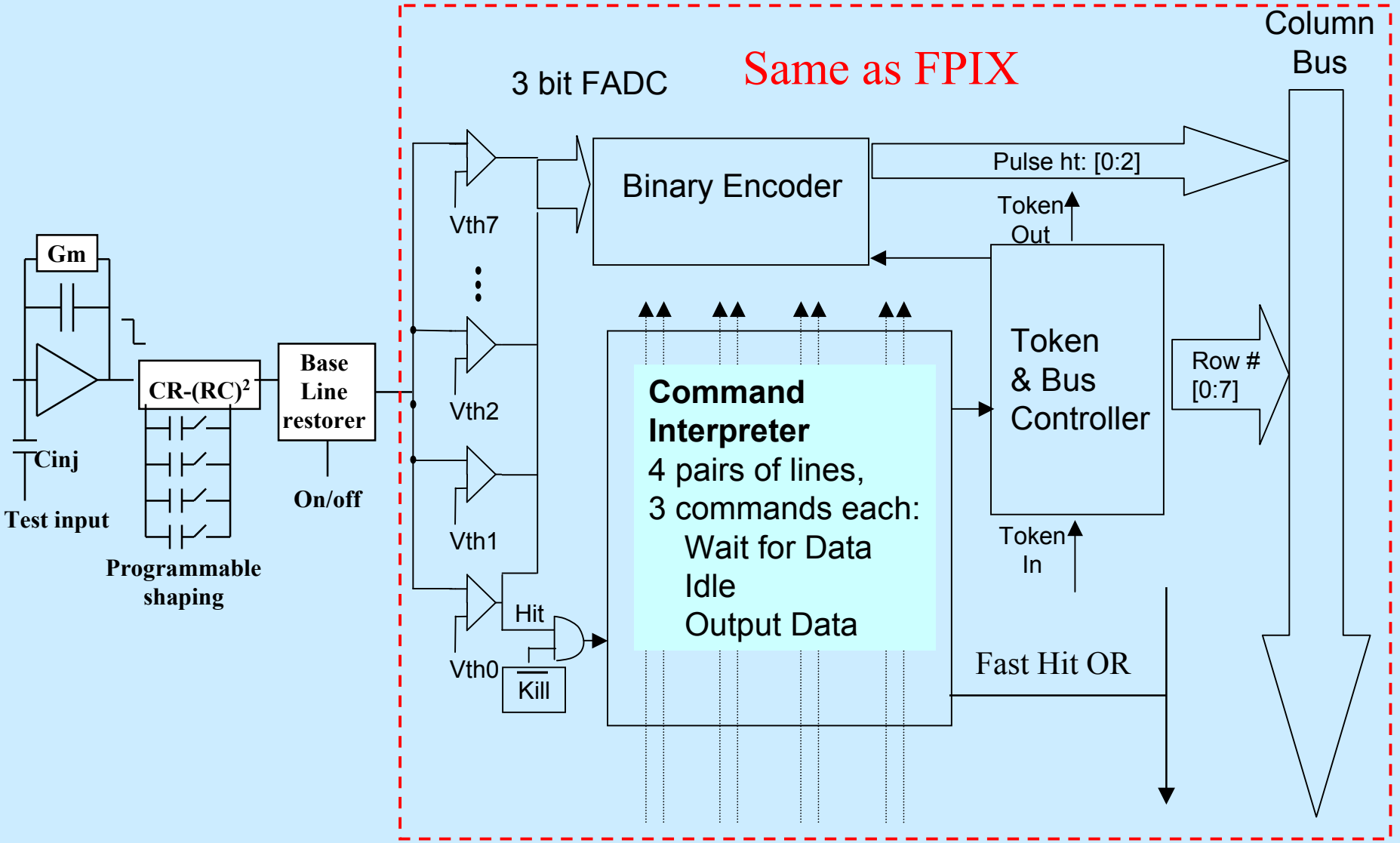


FSSR Block diagram

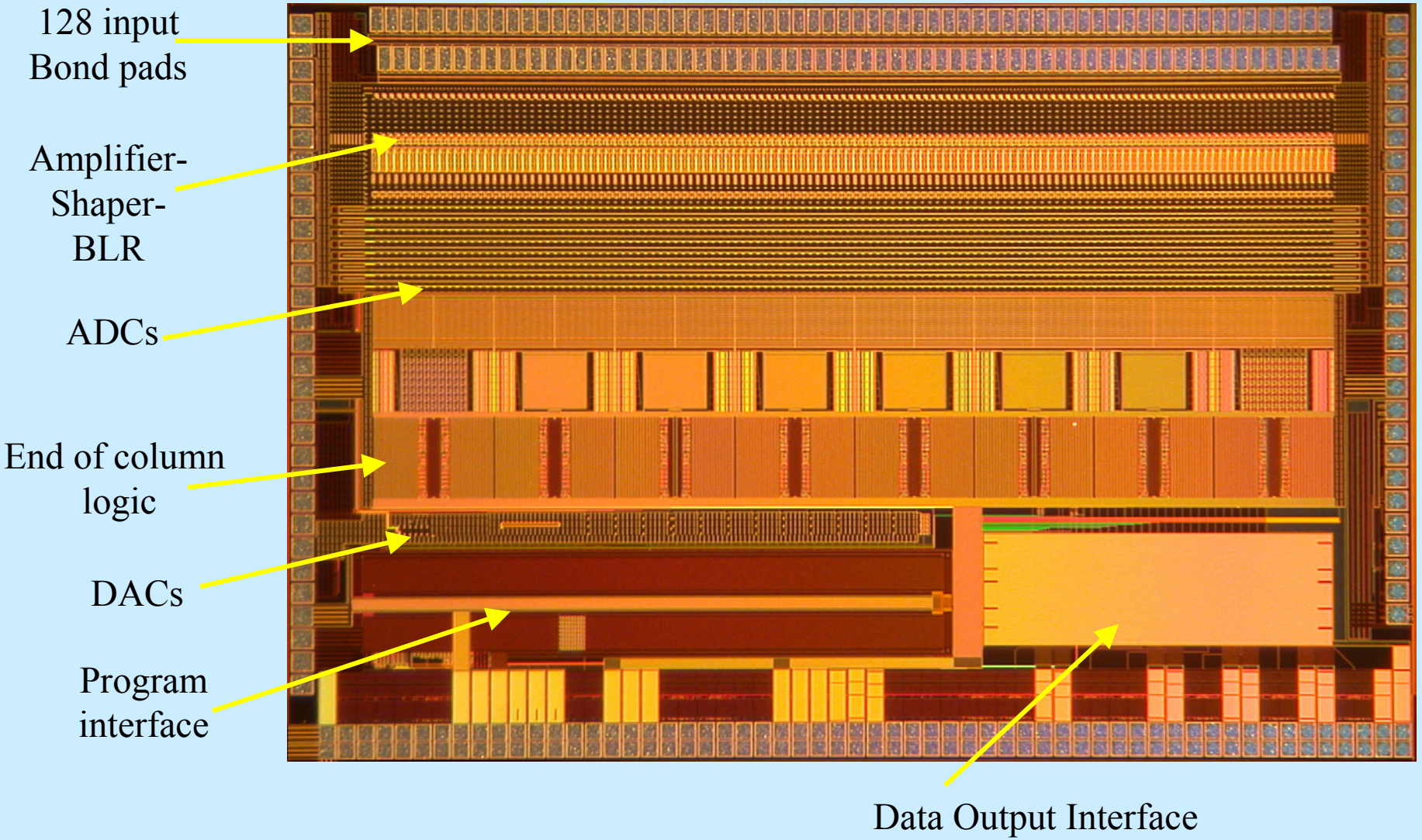
- FSSR Core
  - 128 analog channels
  - 16 sets of logic, each handling 8 channels
  - Core logic with BCO counter
- Programming Interface (slow control – same as FPIX2
  - Programmable registers
  - DACs
- Data Output Interface
  - Communicates with core logic
  - Formats data output
  - Same as BTEV FPIX chip
    - Allows common DAQ



FSSR Channel Electronics



FSSR Chip


128 input
Bond pads
Amplifier-
Shaper-
BLR
ADCs
End of column
logic
DACs
Program
interface
Data Output Interface

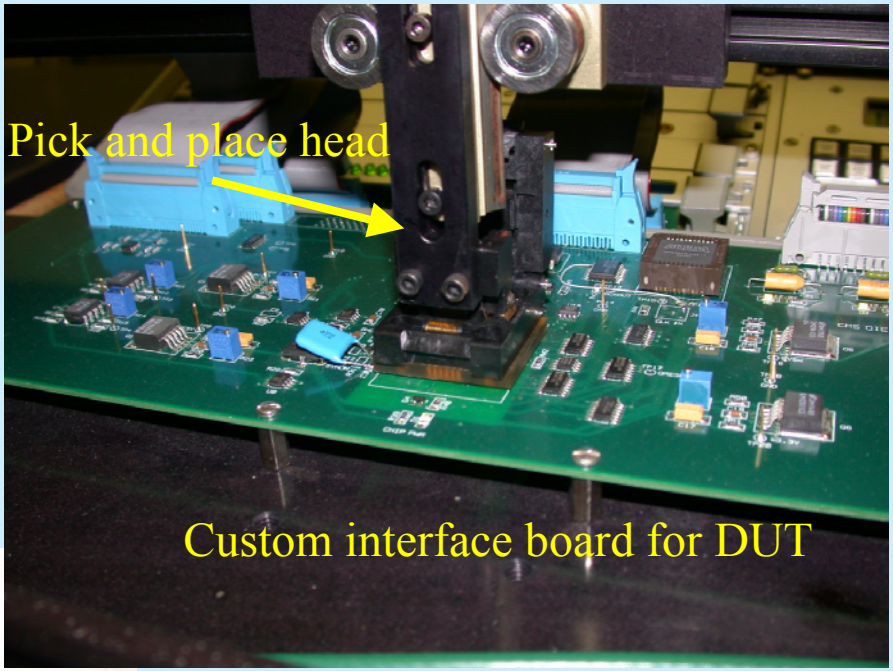
IBM 0.13 micron Evaluation Chip

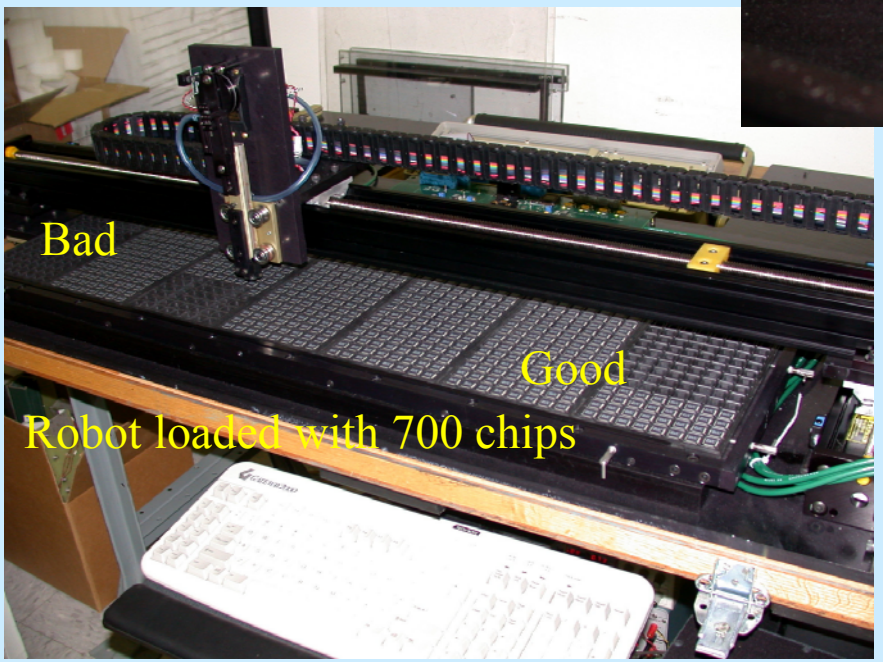
- First venture into 0.13 micron design
- Chip includes
  - Pixel design based on FPIX2
  - Various registers to study SEU
  - Frequency multiplier (PPL)
  - Test devices
- Initial tests suggest good correlation between simulations and actual devices.
- Interest for possible MAPS applications

Chip Testing at FNAL

- Production testing group for all chips developed at FNAL.
  - Wafer level testing
    - Semiautomatic 8 inch wafer probe station
  - Packaged parts testing
    - Two robotic packaged parts testers
- Testing also done for other customers
  - CMS (pixel readout chips, token bit manager chip)
  - University of Michigan MASDAX chips

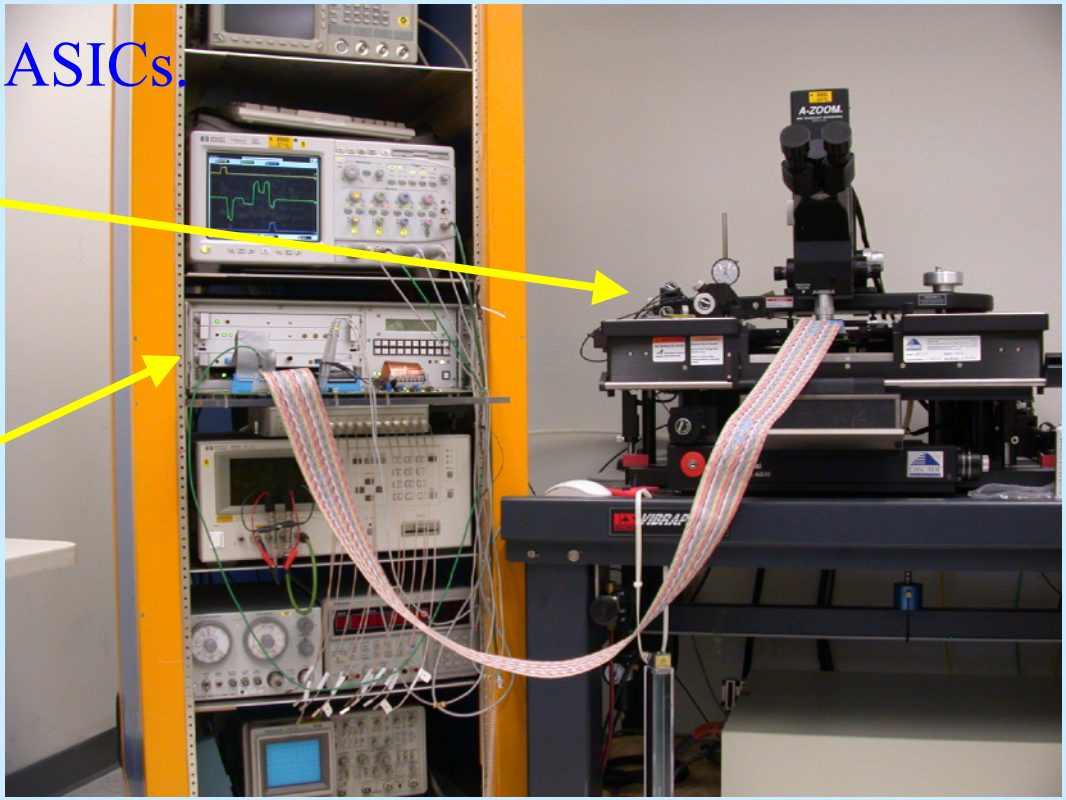
Robotic ASIC Tester



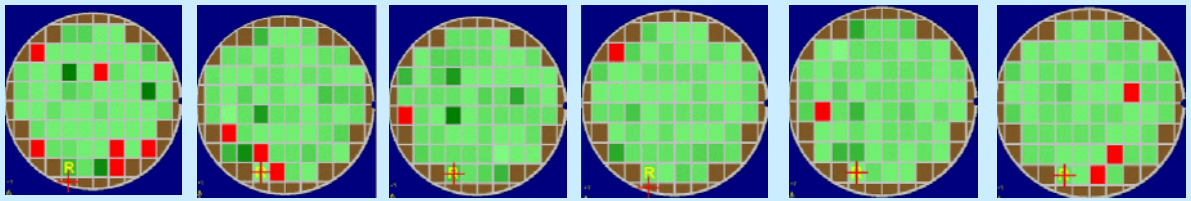


Wafer Testing on Probe Station

- Hardware has tested many ASICs.
- Probe station
  - –Semi-automatic
  - –Micro chamber
  - –8” chuck
- Data acquisition
  - –Tester box
  - –Interface PCBs
  - –Computer
  - –Test & measurement equipment



Wafer maps showing Good and bad chips (green shading shows grading)



Summary

- Fermilab ASIC designers have designed chips for numerous different experiments.
  - CDF, Dzero, CMS, KTEV, MINOS, NOvA, CALICE, BTEV, etc.
- Designs are generally mixed signal with an emphasis on the analog design.
- New areas of current interest include ILC (vertex, tracking, calorimetry), SNAP (CCD control), PHENIX (mini strips), SCMS (pixels, mini strips).
- Always interested in new projects.
- For more information, checkout our web page

  http://www-ppd.fnal.gov/EEDOfficew/ASIC_Development/asicmain.html.