Trigger Timing Distribution (TTD) Upgrade

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changes in the Belle timing system

current timing system

- FASTBUS based ⇒ Interface with COPPER
  i.e. timing distribution to ~1000, something compact & scalable
- Faster system clock (16 MHz ⇒ 42 MHz)
  to reuse technologies developed for LHC. 42 = rf-clock/12
- Step-by-step replacement
  i.e. old and new system co-exist, something compatible
- Need a better signal monitoring
  No monitoring at various points (LEMO cables, FASTBUS backplanes)
- Need to update chips/tools
  Built in ‘95–’97, no longer existing Xilinx FPGA nor software support
Something compact

- **Idea** — all signals in one CAT5e cable using serial-bus LVDS
- **Pros** — fits on PMC, 10 ports on VME 6U, cheap cables
- **Cons** — delay (=deadtime) due to SER/DES, cable can’t be very long

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encoded and decoded at every 42.33 MHz clock (508 Mbps on CAT5e)

pair 1: upstream → downstream 10 bit (trigger tag, type, sync, abort, error detection)
pair 2: downstream → upstream 10 bit (busy, other errors, error sources, error detection)
pair 3: upstream → downstream 1 bit dedicated LVDS for the trigger timing
pair 4: upstream → downstream 1 bit dedicated LVDS for the system clock
**Something compatible**

- **Idea** — no change in the trigger-busy handshake
  Interface module that handles signals of various levels: NIM, ECL, TTL with compatible connectors, and in VME6U
- **Pros** — only LVDS inside TTD, no external level converters
- **Cons** — complicates firmware and module usage

**TTD system**

- LEMO 4 in/4 out, 8 pair differential in, 5 pair ECL out, 17 pair TTL bidirectional

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Something scalable

- **Idea** — cascading same type modules with same format (1 to 8)\(^4\) stages \(\Rightarrow\) up to 4096

- **Pros** — only 3 module types (master, switch and receiver)

- **Cons** — further delay (deadtime)

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1 \(\rightarrow\) 4096 fanout by cascading 4 TT-SW modules

Stage 1 & 2 \(\rightarrow\) 64 in 1 master VME

Stage 3 \(\rightarrow\) 8 (or \(n \rightarrow 8n\)) in every detector VME

Stage 4 \(\rightarrow\) 16 (or \(3 \rightarrow 24\)) in every COPPER crate
TTD modules

**TT-IO** master-TTD, or multipurpose I/O module (VME 6U)
- ECL, NIM, TTL, LVDS inputs and outputs
- Construct downward TTD signals from various inputs, and receives upward TTD signals for the event sequence
- Also works as a receiver module or a level converter

**TT-SW** 1-to-8 switch module (VME 6U)
- Distributes the downward TTD signals, and merges 8 sets of upward TTD signals into one
- Extra LVDS inputs to attach to the TTD signals

**TT-RX** receiver module on COPPER (PMC card)
- Receives the TTD downward signals, and collects busy etc and sends back as upward TTD signals
Development of history

- 2001 Super-B DAQ discussion started
- 2002 April TTD design started
- 2002 Dec first prototype of TT-RX receiver module
- 2003 Nov second version of TT-RX
- 2004 Sep first prototype of TT-SW switch module (4 modules)
  (JPS meeting, IEEE NSS’04)
- 2004 Nov final version of TT-RX (35 modules)
  (HL6 workshop, mini DAQ WS)
- 2004 Feb first prototype of TT-IO interface module (2 modules)
  (2nd SuperB WS)

All three types of modules are ready
**TT-IO**

- Xilinx 9500XL CPLD
- Xilinx Virtex II Pro FPGA
- General LVDS Input/output
- TTL I/O

**TT-SW**

- Xilinx 9500XL CPLD
- Xilinx Spartan3 FPGA
- RJ-45
- DES

**TT-RX**

- PCI interface (PCI9054)
- Xilinx CPLD for bus handling (Spartan-3)
- Xilinx FPGA for everything (Spartan-3)

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*TTD modules*

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Performance tests

- Cable length
- Serial bus stability
- Synchronization (in a cascade configuration)
- Trigger-busy handshake
- Latency measurement (due to the serial-bus en/decoding)
- Jitter measurement (of the system clock timing)

In addition to basic functionality checks and debug (so far all the tests were made with TT-RX and TT-SW modules only)
Cable length and stability

- Cable length limit — serial-bus does not allow long cable
- Shielded CAT5e works up to 15 m (but 20 m did not)
- Constrains the cable layout in the electronics-hut

- Stability — bit-error is not allowed at any clock
- Tested for 20 days with no bit-error
- Still not immune to a large EM noise (e.g., power cycling in a nearby crate)
- Upward TTD signal has to be in phase at every stage
- Tuning knobs — clock edge selection at FPGA or serializer (or digital clock manager (DCM) in the FPGA, not successful so far)
- 4-stage cascade works (no bit-error) after properly setting the clock edges (modified TT-RX is used as the Tx in the test)
Trigger-busy handshake and serial-bus delay

- Trigger-busy handshake
  - Tested with the serial-bus based busy signal
  - Works at 30 kHz design L1 rate or more

- Serial-bus delay = busy delay = **deadtime**
  - Round-trip delay of 41 clocks (~1 μs) is measured
    - ~4 clock delay due to encode/decode
    - busy delay of ~0.5 μs
  - 1.5% intrinsic TTD deadtime at 30 kHz
    (Belle people are more generous about deadtime)
Clock jitter is the most relevant, other downward signals to be within the same clock, and not essential for the upward signals.

Measured jitter of 240 ps (rms) is small enough. Originally planned to use the reconstructed clock. Jitter can be improved by fixing the TT-RX design. However, PID will need very small jitter and handled separately anyway.
No change in the core part of the current timing system and software, interface with the TT-IO module

Need a temporary system clock line for EFC

Clock part of the master TTD system should (partially) exist

Cables have to be laid out in the hut

Installation during 2005 summer shutdown

Repeated for CDC upgrade in 2006 if it works (RF bucket ambiguity will increase from 8 to 12)
It may be easier to move to the global TTD system when more than one subsystems exist (EFC + CDC)

- FASTBUS readout systems still remain
- All software has to be replaced
Short-term plan and summary

2005 spring — Works on firmware/software, 2nd version of TT-SW
2005 summer — Pilot COPPER installation for EFC
2005 autumn — 2nd version of TT-IO, module mass production
2006 winter or summer — Global TTD installation

- (Almost) ready to start replacing the timing system
- Step-by-step installation benefits with the current Belle and is compatible with SuperBelle