Abstract

Utilizing a time expansion technique, a dead-time-less, multihit TDC has been developed for readout of the BELLE TOF detector at the KEK B factory. Time digitization consists of three steps: tagging the input signal timing with respect to a reference clock synchronized with a beam collision time, expansion of the time interval and readout by a conventional multihit TDC. Assuming a time expansion factor of 20 and a multihit TDC with a 500 ps LSB, this system provides a precision TOF measurement of 25 ps LSB with a dead time of less than 1 μs. The design concept and prototype test results are described.
1. Introduction

The TOF system of the BELLE detector at the KEK B factory is designed to provide $3\pi/K$ separation up to a momentum of 1.2 GeV/c for B-flavor tagging, which requires a TOF time resolution of 100 ps. An intrinsic time resolution of 90 ps has been demonstrated in several beam tests of real size prototype counters [1]. A leading edge discrimination scheme with time walk correction is used to derive a precise TOF timing. To ensure a time resolution of 100 ps, additional errors in determining the TDC start time (beam collision time) and in TDC module, should be minimized.

At the KEK B factory, the beam bunch interval will be approximately 2 ns for a high luminosity operation of $10^{38} \text{cm}^{-2} \text{s}^{-1}$ [2], and the signal rate is expected to be a few ten kHz per TOF counter [3]. The beam collision time should be precisely determined event by event, and dead time in data readout should be minimized. To meet such a high frequency beam collision and high signal rate, we have developed a new TDC system of a clocked time stretcher using an external clock (approximately 16 ns) synchronized to the RF signal (approximately 2 ns), which will be used to control the KEKB accelerator.

Figure 1 (a) shows a block diagram of BELLE TOF readout electronics. Charge (Q) and timing (T) signals are converted to timing signals through a charge to time converter (QTC) and a clocked time stretcher (TS) [4], respectively, then the converted timing signals are recorded by a multihit TDC. This readout scheme allows a substantial flexibility in event decision latency time up to the full range of the TDC (32 μsec). It also provides a precision time measurement.

Figure 1 (b) shows a block diagram of the TOF front end electronics (TOFFEE), which provides timing signals (differential ECL) for each PMT analog signal: a charge Q from QTC and a timing T from a discriminator. It uses a double discriminator scheme to gate the relevant signals. A low level (LL) threshold is used for precision timing measurement, while a high level (HL) one provides a self gate for QTC and T to reduce an effective dead time. The timing output T is expanded by the clocked TS before recording by the multihit TDC. Maximum dead times in QTC and TS are designed to be 3 μs and 1 μs, respectively.

We describe time stretcher schemes in section 2, a design of TDC system for BELLE TOF counter in section 3. Then, we describe test results of prototypes in section 4 and make a summary of this new TDC system in section 5.

2. Simple time stretcher and clocked time stretcher

The time stretcher principle is shown in Figure 2, where (a) and (b) are for a simple...
time stretcher and a clocked time stretcher, respectively.

Measuring time with higher resolution requires converting the time to a voltage (or charge), namely with a time-to-amplitude converter (TAC), and then measuring the voltage (or charge) with an analog-to-digital converter (ADC) [5, 6, 7]. A charge proportional to the time interval ($\Delta T$) is accumulated on a capacitor through a constant current source, then it is discharged in a longer time interval ($f \times \Delta T$) with a lower speed, and digitized by counting a clock by a scaler until the discharge is completed. This is a conventional TDC technique used for TOF readout.

The factor ($f$), given by the ratio of the source currents in ramping up (TAC) and ramping down (ADC) processes, is called as the time expansion factor or time stretch factor. The maximum time range is a function of the resolution of the ADC and the desired time resolution. 12 bits of ADC can cover a maximum time range of 100 ns with 25 ps LSB. Assuming a digitization clock of 40 MHz and a time stretch factor of 1000, a conversion time of 100 $\mu$s is required to cover the full time range. The digitization can be made much faster using a multihit TDC with 500 ps LSB which is equivalent to 2 GHz clock, and choosing a smaller time stretch factor. If a time stretch factor of 20 and a clock of 2 GHz are used, only 2 $\mu$s is required to digitize the full time range with 25 ps LSB.

Longer time intervals can be measured with a technique similar to that of a random interleaved sampling oscilloscope, i.e. by measuring with respect to a continuous clock signal. Figure 2(b) shows the clocked time stretcher concept. The time interval $\Delta T$ between the start signal and the next clock signal is expanded to $f \times \Delta T$, then $T_1$ and $T_2$ are measured with a precision of 500 ps LSB by a multihit TDC, with respect to
the stop signal. The timing of the input signal is calculated as $T_1 - \Delta T$ from those two measurements with a precision of 500/\(f\) ps, namely 25 ps for a stretch factor of 20. This is the clocked time stretcher. In this scheme, the time interval to be expanded is always between one to two clock periods, thus the conversion time is determined by a choice of the time stretcher clock (TS clock). This clocked time stretcher allows a long time interval measurement with a high precision within the full range of the readout TDC.

3. TDC SYSTEM FOR BELLE TOF DETECTOR

In order to measure a particle Time of Flight, the beam collision time ($t_0$) should be determined precisely event by event. In the TRISTAN experiments, a timing signal of 5 \(\mu\)s period was used for TDC start timing, which was picked up from a beam button located at a few meter away from the interaction point. However, the same scheme can not be adopted at KEKB because the bunch separation (2 ns) is small. There is no beam pickup available yet which can distinguish individual beam bunch timing with a time jitter of 20 ps.

For the BELLE experiment, we decided to adopt a clocked time stretcher. A reduced RF clock of approximately 16 ns period will be used as a TS clock. The clock is precisely synchronized to the RF signal provided from the KEKB accelerator. A time stretch factor of 20 is chosen to get a 25 ps LSB with TDC1877S readout (500 ps LSB and \(\sigma=300\) ps). The time interval to be measured is constrained between 16 ns
and 32 ns. The dead time is about 800 ns, including a recovery time before accepting another signal input.

The design goal is 20 ps for the time jitter of the RF clock to the RF signal (508.9 MHz) [8]. An integer number \((N_{\text{bunch}})\) is associated with each beam collision time, as the collision time is quantized exactly by the bunch period of approximately 2 ns. The \(N_{\text{bunch}}\) is obtained from the recorded data in offline analysis, and the beam collision time \((t_0)\) can be determined with the same time jitter as the RF clock provides.

With central drift chamber (CDC) tracking, the timing of each track at the interaction point can be calculated from the raw data with a precision of 500 ps, without fine corrections. These timings can be used to determine the collision bunch. If the TS clock is not synchronized to the beam collision time, the offset time varies randomly even by event, so that a self determination of the \(t_0\) is required for each event. In this case, precision of \(t_0\) will be largely degraded depending on the number of relevant TOF tracks in the event. This is the major reason to use the RF clock for the TS clock.

The beam phase relative to the RF signal is monitored by a beam bunch feedback system with 8 ps LSB [9]. This phase information as a function of bunch number can be used for a further correction of \(t_0\). For this purpose, the beam bunch number is recorded together with the TOF data. Taking into account the jitter of the RF clock and a beam bunch length of 4 mm, a time jitter of 30 ps is a goal for \(t_0\) determination.

Figure 3 shows a timing diagram for the clocked time stretcher TDC. Each input signal timing is measured with respect to the next clock. The TS output contains two pulses with four edges, which are named as \(T_1\), \(T_2\), \(T_3\) and \(T_4\) in order. \(T_1\) and \(T_2\) are the input signal timing and the next clock edge, respectively. The time interval \(\Delta t = (T_2 - T_1)\) is expanded to \(f \times \Delta t = (T_3 - T_2)\). \(T_4\) is created at the next clock edge following \(T_3\), when the TS completes the conversion and is ready to accept the next input signal. All four edges are recorded by a multihit TDC with a precision of 500 ps LSB, with respect to a common stop signal initiated by a global trigger signal.

The exact signal timing can be reconstructed from \(T_2\) and \(T_3\) with a precision of 25 ps LSB, if accurate values for the time stretch factor for each channel and the clock period of the readout TDC are given. Measurements of \(T_1\) and \(T_4\) are important to calibrate those parameters. The measurements of \((T_2-T_1)\) can be used to calibrate the time stretch factor in comparison with \((T_3-T_2)\), and \((T_4-T_2)\) can be used to monitor the time scale of the multihit TDC in comparison with the exact RF clock period. Even though those parameters may be a function of temperature and supply voltages, they can be monitored continuously and self-calibrated from the recorded data. This feature of self-calibration eliminates the need for a dedicated calibration system.
4. Test results of prototype modules

4.1 Test results of simple vs clocked time stretchers

A prototype time stretcher was built and tested for a proof of principle. It was fabricated with two channels for each simple and clocked TS. A time stretch factor of 20 was chosen. Two channels of the simple TS required a common start signal. An internal clock of 100 MHz was used for the clocked TS. The timing signals from the four channels were recorded by a CAMAC multihit TDC 3377 with a 500 ps LSB. The delay time between the two signals was varied from 10 to 90 ns.

The residuals of time difference measurements are plotted as a function of the delay time in Fig. 4. Resolutions of 22 and 32 ps were found for the two channels of the simple TS. The clocked TS was evaluated by looking at the difference time of the two channels and was found to be 35~40 ps per channel. The worse resolution was considered to be caused in the synchronization circuit of the clocked TS. Results of the simple TS indicated that a goal of 20 ps jitter should be achievable with a clocked TS. The clocked TS was also tested by using double pulses in each channel as a function of delay time between them, which was varied by steps of 77 ps in a time range from 2.0 μs to 2.3 μs. The results were the same as described above.

4.2 Test results of clocked time stretchers II

According to the test results of the first TS module, a careful design was made for a second prototype of the clocked TS, considering isolation of analog and digital parts to avoid ground noise and interference through power lines. Two families of ECL chip,
Figure 4: Test results of time stretcher prototype I.

ECLips for channel 1 and 10KH ECL for channel 2, were fabricated on a board for comparison. The ECLips channel was expected to have better performance. A time stretch factor of 20 was chosen. A CAMAC TDC3377 of 500 ps LSB was used for recording. Two TS clocks: an internal 100 MHz and an external 64 MHz, and three kinds of pulses were used to test the TS channels.

(1) Test 1: an internal TS clock of 100 MHz and a double test pulse with a time interval of 77 ps × N + 1.8 μs, where N is varied from 0 to 4000. The phase of the test pulse is random to the TS clock.

(2) Test 2: an external TS clock of 64 MHz and a single test pulse synchronized to the TS clock. The delay time of the pulse is about 20 ns.

(3) Test 3: an internal TS clock of 100 MHz and a double test pulse synchronized to a 64 MHz clock with a fixed time interval of about 10 ns. The test pulse phase is random to the TS clock. After removing interference between the TS clock and the input signal in the ECLips channel.

The test results are shown in Table 1. The 10KH ECL channel showed a resolution of 30 ps better than the ECLips one. On the other hand, the test results with a synchronized single pulse mode (Test 2) showed a comparable resolution of 22~25 ps for the both types. After careful investigation of the results, the cause is considered to be due to an interference of the input signal lines and the TS clock line in the ECLips design. The TS clock disturbed the TAC process through the interference. For a synchronized single test pulse (Test 2), the interference did not worsen the time jitter
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Table 1: Time jitter of time stretcher study modules. See text for detail of the tests.

![Image](image1.png)

Figure 5: Test results of time stretcher prototype II.

due to its fixed phase the TS clock, while it did for a random test pulse (Test 1). The results after modifying the board are summarized in the last column of the table. Fig. 5 shows a result of the ECLips channel as a function of the delay interval between the double test pulses. The residual is for a time difference measurement, then it should be divided by a factor $1/\sqrt{2}$ to give a 20 ps per measurement. With those improvements, a production design of clocked time stretcher with 20 ps resolution is completed. A production prototype daughter-board is now being fabricated.

4.3 Test results of TS daughter board prototype
This contents will be almost the same as in the section 4.3. We would like to discuss here the tester module in detail, because it is very important for clear description of performance test of the production prototype TS modules. We are looking forward the test results.

5. **Summary**

A new TDC system has been developed for the BELLE TOF detector at the KEK B factory, which accommodates high beam collision rate. This system consists of a clocked time stretcher and multi-hit TDC. By choosing a time stretch factor of 20 and a multi-hit TDC with a 500 ps LSB, this provides time measurement with a precision of 20 ps and with a dead time of less than 1 μs. In addition, by using an external clock of approximately 16 ns, which is precisely synchronized with the accelerator RF signal, this system provides a beam collision timing with the same precision as the RF clock provides.

We would like to acknowledge Dr. R. Suentake and Dr. E. Kikutani for their valuable discussions and their work to provide a RF clock and a beam phase monitor system for the BELLE detector.

Finally, we gratefully appreciate the support of Department of Energy, and would like to express our thanks to Prof. S. Iwata and Prof. F. Takasaki at KEK for their support to this work.

**References**


T.Yamaguchi,"Simulation of Photon Background on TOF in BELLE detector", BELLE Note #133.


[8] Private communication with Dr. M.Suetake, who is responsible for the RF signal for the KEKB accelerator system. For the TRISTAN accelerator, they succeeded in providing an RF signal with a time jitter as good as 20 ps.