Belle Upgrade:
MTS1 Preliminary Test Results

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Today’s Objectives

• Brief TS Reminder
  – Multi-channel
• Preliminary MTS1 Test Results
• What next
Time-to-Time – Clocked and MTDC

Sample edges with 500ps resolution

Reference Time
First pulse
Clock
Synchronized pulse
Ramp
Output

2ns
TS + MTDC Performance

• ~20ps jitter

\[ \sigma = 22.5\text{ps} \]
Works Well, Why Change?

- **LRS Demise**
  - Unobtainium
  - Use new generation of precision, low deadtime multi-hit TDCs
  - Form-factor
    - Lower card costs, many channels
    - FINESSE/COPPER (PMC)
  - For TOP want multi-hit truly deadtimeless
    - Min. $\delta T \geq 10$ns (HPTDC) [5ns typ.]
  - Reference to RF bunch and self-calibration
Time Stretcher Module

- Designed with LRS
  - R&D 100 Award

- 16 Channels/1 per DC
- Stretch factor 20x
- RF clock Reference

VIPA Standard Module
MTS1 Layout

- Sent for Fab. Sept 16, due back mid-Dec.
- Received just before Christmas
MTS1 Silicon (1)
MTS1 Silicon (2)

Completely differential signal routing
Evaluation Board

- Quick and simple test board – avoid complexity unless MTS1 shown to work – found bias changes!
Test Station

• Software readout works – but very slow (1/4 Hz)
Input:
4:1 Stretch Ratio
25ps → 100ps lsb

Output to TDC
Ramp
Ref

TS SPICE Output

Output Signal

- Measured with a 5GSa/s scope (500MHz ABW) ......{200ps/sample}
TS SPICE Simulation

- Simple fit:

\[ y = 3.7503x + 4.9388 \]

\[ R^2 = 1 \]

Input Time difference [ns]

Stretched Time [ns]
MTS1 Timing Residuals

- After trying many things, still getting clock feedthrough – however can be simply calibrated
MTS1 Timing Residuals

- However, this value includes the (large) system jitter
MTS1 Jitter

\[ \sigma_{MTS1} = \sqrt{\sigma_{meas}^2 - \sigma_{Jitter}^2} \]

\[ = \sqrt{(51.3)^2 - (49.5)^2} \]

Use RMS value

\[ \sigma \sim 13.5\text{ps} \]

\[ \sigma \sim 49.5\text{ps} \]

- Not sure believe it, but promising and impetus to put together a better test system

Direct Residuals Comparison

- Comparable:

![Graphs showing residual comparisons between MTS1 Time Stretcher and LRS module test.](image-url)

**MTS1 Time Stretcher residuals**

- \(\sigma = 22.5\text{ps}\)
- RMS = 22.0ps

**LRS module test**

- \(\sigma = 26.3\text{ps}\)

**MTS1 Simulation**

- \(\sigma = 26.3\text{ps}\)
- RMS = 22.0ps
Summary

• Results
  – Some work on linearity needed
  – Multi-hit capability works

• Next steps
  – Proper Test board (Hulya)
    • with separate analog/digital VDD
    • Move 5V (noisy!) oscillator offboard
  – CAMAC based test set up (<<50ps intrinsic noise)

• Future
  – Unfortunately Agilent 0.5µm no longer supported by MOSIS
  – Enough for prototyping (~20 chips), but may want to migrate to
    TSMC 0.35µm process
  – TDCless TOF/TOP? (STRAW2) – chip back, awaiting test