Belle Upgrades and Possibilities: Part 3: SVD2, SVD3 & Pixel

Gary S. Varner
University of Hawai‘i
Local Belle meeting
February 2003
Schedule

• **TOP Counter** (Fall)
  – PID Comparison/Super-Belle
  – Monolithic Integrated Time Stretcher (MTS1)

• **Vertexing upgrades** (today)
  – SVD2.0 (*Kirika* L1.5 BB)
  – Pixel R&D: XTEST2 and MAPS (*Fang*)

• **FINESSE and COPPER** (next time)
  – Pipelined Readout: $10^{35}$ Luminosity issues (*Yangheng*)
  – Evaluation board for MTS w/HPTDC + TMC
  – TDCless TOF/TOP? (*STRAW2*)

Details subject to interest/feedback
Today’s Objectives

• **SVD2.0 Upgrade**
  – Improvements and impact

• **SVD3.0 Upgrade Options**
  – “deadtimeless” readout?

• **Pixel R&D**
  – XTEST2 architecture – new lease on life
  – MAPS proto testing
SVD 2.0 Upgrade

- Larger angular acceptance.
- Increase of number of layers 3 to 4.
- Smaller radius of inner-most layer (3cm→2cm).
  (smaller r of BP also)
- Radiation tolerant (20 Mrad) readout chip (VA1TA).
Double-Sided Strip Detectors

Benefits of “Atoll structure”

<table>
<thead>
<tr>
<th>DSSD</th>
<th>L1~L3</th>
<th>L4</th>
</tr>
</thead>
<tbody>
<tr>
<td>P(z)</td>
<td>N(ϕ)</td>
<td>P(z)</td>
</tr>
<tr>
<td>size</td>
<td>79.2x28.4</td>
<td>76.4x34.9</td>
</tr>
<tr>
<td>Strip pitch</td>
<td>75µm</td>
<td>50µm</td>
</tr>
<tr>
<td># of strip</td>
<td>1024</td>
<td>512</td>
</tr>
<tr>
<td>Strip width</td>
<td>50µm</td>
<td>12µm</td>
</tr>
</tbody>
</table>
Ladders

Forward

Backward

L#1
L#2
L#3
L#4
2002 “Progress”

- Ladder production started in Feb.
- Low yield of flex, especially for longer one
  - Improvement of etching, laser surgery....
- Very low yield of functional hybrid
  - Ran out of AlN substrate even with 50% spare
- Give up to complete for 2002 summer installation
- Partial mount (3/4) for system commissioning
- Additional delivery of hybrids Nov.-Dec.
- SVD1.6 work for beam pipe replacement
AlN Hybrid Woes

VA 0.35R – >20MRad hardness

Solder joints of double row legs of SM connector are too weak

Heat conductivity too good in AlN+Cu+AlN boards to make good soldering
Flexible Circuit Boards

- Flexible layout of Si detector
  Different size of DSSDs are read out via same hybrid
- Lower capacitance than double metal routing
- Fine pitch (~$50 \mu$m), Large area (~$30 \times 3.3 \text{cm}^2$)
- Production yield is poor: strip yield >95%
Flex defects and surgery

Before Surgery

Cut

Several Ohm

Short

After Surgery

Cut

>10 M Ohm

Short

Several Ohm
Mounting completed Feb. 13

The last Ladder!
New Beampipe

- Smaller radius (1.5cm)
- Better cooling with liquid
- Heavier masks
Readout System – Similar, but...

Big change!!
Floating supplies
Cosmic Results

- Basic functionality shown – trigger main residual task
SVD2.0 Schedule

- Real full system (hardware) ready at early March
- Commissioning of trigger system in progress (Kirika)
- Installation in July-Sept. is assumed.
SVD3.0 Goals

- Smaller-radius beampipe → Rbp = 1cm
- Good intrinsic resolution → 50um or less
- Survival
- Smaller amount of material → need studies

½ of present resolution seems feasible. 1/3 of present should be tried!
Resolution with Rbp=1cm and Strip pitch = 50um

To meet the Super KEKB requirement
Further improvement possible by reducing material (especially beampipe and the innermost pixel, as well as having a larger lever arm)

5-layer SVD (a la Inner Tracker taskforce)
Occupancy issues

Pixel for $R < 3\text{cm}$
Pipeline for $R < 10\text{cm}$

Trigger simulation study desirable

Large ambiguity even with dedicated simulation. Need to be conservative.
Configuration of SuperB VXD

Rbp = 1cm
2-layer Pixel
3 or more DSSDs
Rcdc > 15cm

Extrapolating present hit rate and requiring the hit rate being less than the present, Rcdc > 12cm is “probably no problem”.

DSSD w/ Pipeline readout

Additional DSSD layers

Silicon Strip Readout Requirements

- Good S/N (> 20)
- Small Occupancy (< 5%)
- Small Deadtime ( < 10 usec/event )
- Radiation Hardness (up to 40 Mrad)
- Fast Trigger Capability
- External Noise Immunity (tolerance for CMN ~1000e-)
- Readiness in 2006 (“Evolution” rather than “Revolution”)

Choice of readout chip is essential.
## DSSD Readout chips

<table>
<thead>
<tr>
<th>Exp</th>
<th>chip</th>
<th>process</th>
<th>pipeline</th>
<th>fasttrig</th>
<th>principle</th>
</tr>
</thead>
<tbody>
<tr>
<td>Belle</td>
<td>VATA</td>
<td>AMS 0.8um</td>
<td>x</td>
<td>o</td>
<td>cnt. Shaping. Analogue</td>
</tr>
<tr>
<td>BaBar</td>
<td>AtoM</td>
<td>Honeywell</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLEO</td>
<td>FE/BE</td>
<td>Honeywell</td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>ZEUS</td>
<td>Helix</td>
<td>AMS 128cells</td>
<td>x</td>
<td></td>
<td>Analogue</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(non-radhard)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CDF II</td>
<td>SVX4</td>
<td>IBM ? um</td>
<td>47cells</td>
<td>x</td>
<td>FE/BE architecture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>double-corr. Sampling</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>periodic reset, Digital</td>
</tr>
<tr>
<td>CMS</td>
<td>APV25</td>
<td>IBM 0.25um</td>
<td>192cells</td>
<td>x</td>
<td>Analogue</td>
</tr>
<tr>
<td>ATLAS</td>
<td>ABCD?</td>
<td>132cells</td>
<td>x</td>
<td></td>
<td>Binary</td>
</tr>
<tr>
<td>LHCb</td>
<td>SICA-VELO DMILL</td>
<td></td>
<td>160cells</td>
<td>?</td>
<td>analogue</td>
</tr>
<tr>
<td></td>
<td>BEETLE</td>
<td>0.25um</td>
<td>160cells</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Belle</td>
<td>FELIX(+TA)</td>
<td>AMS0.35um</td>
<td>O(100)</td>
<td>o</td>
<td>Analogue</td>
</tr>
</tbody>
</table>
CMS APV25

- $T_p = 50 \text{nsec}$, $40 \text{MHz}$ sampling
- Pipeline depth = 192 cells $\rightarrow$ 4.8usec
- 128 channel/chip $\rightarrow$ readout latency below 10usec
- Reasonable S/N
  - $246e^- + 36e^-/\text{pF}$ (+ deconvolution effect)

Usage for “DC beam” (B factory)
$\rightarrow$ S/N degradation by $\sim$12%
Deadtime-less pipeline

- 192-cell ring buffer (4.8us)
- 32-depth FIFO (to store cell address)
- (3 consecutive cells / event)
- Trigger

- Readout time = 1/20MHz x 128ch = 6.4us
- No deadtime during readout (unless the address FIFO is full).
- Also periodic reset is not necessary (continuous shaping).
## SVD Trigger Needed?

### Beam Background Reduction Capability of SVD L-1

~ **SVD L-1 Trigger Simulation with CDC-Rphi Trigger and Beam Background (2)**

**K. Uchida**

### Result

**Triggered Track Rate**

<table>
<thead>
<tr>
<th></th>
<th>CDC-Rphi only (Hz)</th>
<th>SVD only (Hz)</th>
<th>CDC-Rphi &amp; SVD (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ffs</strong></td>
<td>17.9 ± 7.3</td>
<td>176K ± 19K</td>
<td>3 ± 3</td>
</tr>
<tr>
<td><strong>s</strong></td>
<td>6.3K ± 140K</td>
<td></td>
<td>473 ± 38</td>
</tr>
</tbody>
</table>

**LOGIC: 3 of 4 & 1st layer hits**

- **Reduction power**: 83 %
- **Reduction power**: 92 %

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<th>SVD only (Hz)</th>
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</thead>
<tbody>
<tr>
<td><strong>ffs</strong></td>
<td>17.9 ± 7.3</td>
<td>194K ± 20K</td>
<td>3 ± 3</td>
</tr>
<tr>
<td><strong>s</strong></td>
<td>6.3K ± 140K</td>
<td></td>
<td>670 ± 45</td>
</tr>
</tbody>
</table>

**LOGIC: 3 of 4 layer hits**

- **Reduction power**: 83 %
- **Reduction power**: 90 %
L1.5-like L1 with APV25

- SVD2 adopts L1.5 trigger
  - used as “abort” for other CDC/ACC/TOF/ECL/KLM ...
  - works as “L1” for SVD
- L1.5-like L1 for all detector components as SuperB
  - A plausible solution
  - CDC trigger used as “Lo” for SVD (latency should be less than 4us)

20MHz (or 40MHz)

APV25

128ch

6.4us (= T₀)

ADC

can be shorter

≈ 2T₀

L1.5-like L1 trigger

2T₀ + α

L1

FPGA

CDC trigger

Total latency depends on the choice of the chip
APV25 readout chain

- Test system – key elements of final system
- Quite similar to SVD 2.0

VME
- APV Sequencer: generates APV25 control signals (CLK, TRG, RES)
- VME-I^2C: slow control (APV25 bias settings)
- VME-ADC: 12 bit, 40 MHz conversion of analog APV25 output

Repeater
- Voltage regulators, signal buffers, I^2C extender
Common Electronics

- COPPER (CCommon Pipelined Platform for Electronics Readout)
- Card ~ crate – aid in data reduction
- On board data reduction

(Yangheng working on – more next time)
Tailoring

- **FINESSE (ADC/TDC):** Detector Interface
  - FINESSE (Front-end Instrumentation Entity for Subdetector Specific Electronics)
  - **FINESSE** is a mezzanine module.
  - An actual implementation of **FINESSE** is not defined by the platform, but can be defined by each sub-detector group so that best ADC/TDC can be designed.

- **Event Buffer**
  - FIFOs are implemented to minimize DAQ dead-time. FIFOs are to separate asynchronous data-read by CPU from event trigger.

**Diagram:**

- Analog signal from Belle → ADC/TDC
- Internal design depends on each sub-detector
- Buffer (FIFO) to minimize dead-time

**Symbols:**

- Sampling Clock
- Trigger Timing

Data Flow

- Multi-trig buffering
VTX FINESSE option 1

- FINESSE simply relay to COPPER event FIFO
VTX FINESSE option 2

Will build Prototype (student opportunity)

- FINESSE local bus control adequate?
- How many channels are realistic?
- Front-panel/cabling space issues
Recent Pixel developments

- **Want to evaluate MAPS type detector**
  - LBL/STAR pixel
  - Thin detector mechanics
- **XTEST2 validation**
  - Renewed evaluation
  - Stanford 10k frame/s camera
- **“deposited” detector**
  - Materials evaluation at HNEI
  - Possible “composite” detector
STAR MAPS Development

- F. Bieser
- S. Kleinfelder
- H. Matis
- P. Nevski
- N. Smirnoff
- G. Rai
- F. Retiere
- H. Wieman,

- Next generation vertexer – 4-5 year development timescale (LBL effort) – started as effort to repeat MIMOSA effort (in TSMC & faster readout)
Evaluation at UH

- Visited LBL @ end of Nov. – $50\mu$m mechanics
- Board here (Fang working on)
- Test SNR vs. frame rate, etc.
APS Concerns

• **Rad hard**
  – Addressed with measurements
  – Well-established techniques for deep sub-micron

• **Depends upon processing**
  – Could go away
  – Repeatability (wafer/batch) & yield
  – Kind of a crummy detector – but very thin

• **Readout speed/SNR**
  – Clear trade-off
  – CDS practicality
  – Pipelined readout
XTEST2 Revisited

A 10 000 Frames/s CMOS Digital Pixel Sensor

Stuart Kleinfelder, SukHwan Lim, Xinqiao Liu, and Abbas El Gamal, Fellow, IEEE

Abstract—A 352 × 288 pixel CMOS image sensor chip with per-pixel single-slope ADC and dynamic memory in a standard digital 0.18-μm CMOS process is described. The chip performs “snapshot” image acquisition, parallel 8-bit A/D conversion, and digital readout at continuous rate of 10 000 frames/s or 1 Gpixels/s with power consumption of 50 mW. Each pixel consists of a photogate circuit, a three-stage comparator, and an 8-bit 3T dynamic memory comprising a total of 37 transistors in 9.4 × 9.4 μm with a

- Essentially XTEST2 architecture
  - 8-bits, 37 transistors ~10μm²
  - 1G pixels/s P=50mW
DPS options

352*288 array

- Possible to use without bump bonding?
  - \( \approx 30\mu m^2 \) room for some digital processing

Fig. 19. 10,000 frames/s image sequence (frames 1, 10, 20, and 30 are shown).
Standard MAPS

- In terms of processing:
  - “easy” to put electrodes on top side

\[ n\text{-well/p-epi diode in epitaxial layer} \]
\[ \text{(standard CMOS process)} \]

charge collection to the diode \((3 \mu m \times 3 \mu m)\)
through thermal diffusion \((\sim 100ns)\)

charge readout: integrated NMOS transistors

\[ \sim 15 \mu m \]

\[ \sim \text{Substrate (P type)} \]
• Amorphous and micro/nano crystalline Si
  – Thin film samples in “January” (Bjorn)
  – Testing with probe station (Sanjay)
Trex Enterprises HDTV

Located in Maui

HNEI doing prototype Deposition work

Designing a 500M pixel array

- micro/nano crystalline Si deposit on HDTV
Interesting Possibility

Combine both!

Would allow redundancy at higher noise rates

Some compatibility issues in choice of circuits
Current thoughts

- Parallel efforts

Evaluation
- Gain experience
- Understand practical limits on performance
- Feedback to design process
- Give grad students/post-Docs some experience with pixels

Exploration/Design
- High Speed readout
- Pipelined readout
- Better SNR:
  - improve detector
  - lower noise
- TSMC submission possible (Nichi-bei request)
Preview of Coming Attractions

• **FINESSE and COPPER** (next time)
  – Pipelined Readout: $10^{35}$ Luminosity issues (Yangheng)
  – Evaluation board for MTS w/HPTDC + TMC
  – TDCless TOF/TOP? (STRAW2)

• **Technology Review** (Future)
  – Board & chip design
  – TOP front-end chip example

Details subject to interest/feedback
COPPER Hardware

- VME and PCI interfaces
FINESESE Hardware

- **Dimensions**
  - Depth × Width = 168.0(d) × 71.0(w) mm².

- **Layout example**

- "PMC" form factor -- compact
• Drift tubes, PIN diodes, RADFETs, RTDs amplifiers and associated bits fabbed at UH