Status of the CLEO-III Silicon Detector

Eckhard von Toerne
Kansas State University
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• Introduction
• Initial operating experience
• Longer term performance/radiation damage
• Outlook

evt@phys.ksu.edu
- CLEO-III silicon detector, installed Feb. 2000
- 4 layers of double-sided detectors (n-side= rφ)
- Readout electronics outside of tracking volume
- Readout on both ladder ends
- Up to 5 sensors are daisy-chained in the readout
Mechanical Design

Layer 4 is 53 cm long, Layer 1 = 16 cm

61 half ladders with 447 silicon Wafers

Layer 1: Silicon, 3z, 7φ
Layer 2: Silicon, 4z, 10φ
Layer 3: Silicon, 7z, 18φ
Layer 4: Silicon, 10z, 26φ
Mechanical Design constraints

- Tight mechanical constraints on SI3 detector:
  - 93% solid angle coverage
  - Front end electronics mounted on support cones outside tracking volume puts severe constraints on electrical design.
  - Total radiation length < 2%
  - CVD Diamond v-beams for mechanical support of silicon ladders
    - 200-300 µm thick, < 0.1 X0

Assembly of Layers 1+2 around the beryllium beampipe
Silicon Sensor

- Double-sided silicon sensors by Hamamatsu, n-type silicon
- 2 x 511 channels, wafer 53.2 x 27 x 0.3 mm
- Strip spacing 50 µm r-ϕ, 100 µm z.
- Ladder length requires low strip capacitance. 9 pF in p and n achieved,
- N-side with pstops, atoll design, pstops punch-through biased.
- P-side is double metal side. Hourglass design of metal layer overlap.
- AC coupling capacitor and bias resistor on separate chip
- Radiation damage constant(surface damage)
  5 nA / kRad / (exposed) cm²
Readout Chain

Silicon Wafer

- Double Sided
  pside = z-side
  nside = r/phi side
- 511 channels / detector

Flex Circuit

- Cu/Au traces on Kapton Substrate
- 511 channels + Bias lines
- Double Sided
- Two Flexes/detector

Hybrid Board

- R/C Chip
  Quartz Wafer
  128 channels
- Frontend
  Preamp + Shaper
  Custom Chip
- Backend
  SVX_CLEO
  8 Bit ADC
- Double Sided

Modular Design of Wafers and Hybrids
Front-End Electronics

- **RC chip (CSEM)**
  - RC chip hosts bias resistor and ac coupling capacitor
  - Operation voltage of RC chip 0-60 Volts
  - 1/2 Depletion Voltage over RC Chip

- **Front-End Electronics (Honeywell Rad Hard)**
  - PreAmp gain 40mV/MIP, output 200mV/MIP
  - Shaping time variable between 0.7 - 3.0 μsec
  - FE noise performance optimized
    - ENC = $145 \text{ e} + 5.5 \text{ e}/\text{pF}$ measured

- **BE Chip (Honeywell Rad Hard)**
  - 8 bit ADC, comparator and FIFO, on-chip sparsification
Hybrid Board
Hybrid Board

- 122 Hybrids, 125,000 readout channels
- Double-sided board carries 8 sets of RC, FE and BE chips
- Five electronics layer on BeO core
- ~60 surface mount parts, 24 chips and 2400 encapsulated wire bonds
- Noise performance on fully populated BeO-boards < 300 ENC
- < 4 Watt power consumption / hybrid
- Cooling through thermal contact with support cones
Power Supply System

- Linear power supplies chosen for low noise performance
- Power distribution boards in VME crates, power feed-in through J3 back plane connector
  - 4 hybrids powered per board
  - Analog and digital section isolated through opto-couplers
  - Additional monitoring software runs in CPU on board
Control System

• Hybrid voltages controlled by port cards
• Port cards connected to DAQ, slow control and power system
• Slow Control system monitors voltage, current, and temperature levels and sets hybrid voltages
  ♦ Slow control process resides in a single crate CPU
  ♦ Communication with Power crates through VME repeater boards
  ♦ SI detectors turn off if slow control process dies (time-out function of power distribution boards)
Initial Silicon Detector System Performance

**Signal-to-noise**, Situation right after installation (July 2000)

<table>
<thead>
<tr>
<th>Layer</th>
<th>Signal/Noise</th>
<th>Noise (100 e)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>r-phi</td>
<td>z</td>
</tr>
<tr>
<td>1</td>
<td>27.9</td>
<td>34.4</td>
</tr>
<tr>
<td>2</td>
<td>29.9</td>
<td>37.4</td>
</tr>
<tr>
<td>3</td>
<td>19.4</td>
<td>27.3</td>
</tr>
<tr>
<td>4</td>
<td>20.1</td>
<td>22.6</td>
</tr>
</tbody>
</table>

S/N >19,
Noise 400-600 e- ENC

**Frontend electronics works fine, low noise, common mode noise <400 e-**

**Stable power system**
(Description in Nucl.Instrum.Meth.A481, 538 (2002))
Performance
Hit Resolution

- Residuals from SI-hit extrapolation
  Residual $r-\phi = 13 \ \mu m$, $Z = 31 \ \mu m$
- Resolution $= \frac{\text{Residual}}{\sqrt{(3/2)}}$
  Resolution $r-\phi = 11 \ \mu m$, $Z = 25 \ \mu m$

Residual $= 13 \ \mu m$

Residual $= 31 \ \mu m$
Radiation Sickness

- Initially, efficiency in layer-1, r-\(\phi\), was \(~60\%\).
  
  **Lower than expected**

- But other layers (r-\(\phi\), z) were ok

- First hint at true nature of problem from high-statistics mapping of silicon hits.

- r-\(\phi\) efficiency shows structure on the wafer.

- Varying the detector/FE electronics settings within the possible range could not restore efficiency.
Hit Map Study

- 2D-Hit-map for first layer
- 3 sensors per ladder with 2mm spacing
- Half rings structures on sensors visible
- Half rings could match full rings on original wafers

**Wafer**

![Hit Map, Layer 1](image)

**Layer 1**

- Turned-off readout chains
- Half-Ring Structures
Time Evolution

- Problem(s) getting worse with time
- Affected now:
  Layers 1+2 r-\(\phi\)
  Outer layers still ok,
  z-side still efficient
- Most likely explanation:
  Radiation damage to silicon sensors. Exact mechanism unknown.
Irradiation Studies

- Original studies were performed ~5 years ago on pre-production sensors and concentrated mostly on detector current vs dose.
- Small increase in detector current expected, mostly due to x-ray-induced surface damage.
- Sensors and FE electronics were designed to be radiation hard (Mrad), expected to be operational for at least 10 years.
- We observe the expected increase in detector leakage current, 1-2 μA per sensor so far. CESR’s radiation levels are only a little bit higher than expected.
- Discussed situation with Hamamatsu
- Detailed irradiation studies are underway.....
Sr90 Source Test

Compare CLEO III silicon wafer with SINTEF wafer
Readout P-side using DC coupled Viking electronics
Trigger readout using $\beta$’s that pass through silicon

SINTEF detector

CLEO III detector

$\sim 15\%$ decrease in M.P.
CERN Beam Test

Use existing Si telescope
Map out response of wafer
Use 100 GeV pion beam

2-D map of pulse heights

Readout single strip
Move along strip

Region exposed
To 4krad Sr90
M.P. = 67

Unexposed region
M.P. = 77
LED and Synchrotron Radiation Tests

Red LED probes surface
IR LED and Synchrotron x-rays (16 keV) probe bulk

LED’s scan across wafer (N-side)
Move from strip to strip, constant position along a strip

Ring structure apparent in LED tests!

Before irradiation

IR LED after 100 krad
Red LED before irradiation
Summary and Conclusion

• In operation, FE electronics reached design goals: 400-600 e noise.
• Signal-to-Noise and resolution goals were reached initially.
• Silicon sensors show signs of radiation damage much sooner than expected. \( r-\phi \) side shows ring patterns on the sensors.
• CLEO’s new experimental phase (CLEO-c) does not need a silicon detector, a low-\( X_0 \) solution is favored, silicon detector might be replaced by a small wire chamber (extreme stereo)

Readout Electronics ok

Silicon Sensors not ok

CLEO-c Can deal with it
CLEO-III Detector

- Located at CESR, symmetric $e^+e^-$ collider at $\Upsilon(4S)$ resonance
- New RICH particle ID. CLEO achieves $> 4 \sigma K/\pi$ separation over full momentum range
- New Drift Chamber with same $\Delta p/p$ and smaller tracking volume to accommodate IR Quads and RICH.
- New large 4 layer SI detector
CLEO Physics Program

- **1990-1999:**
  CLEO-II+II.5 collected ~10 fb\(^{-1}\) on the \(\Upsilon(4S)\)

- **2000- June 2001:**
  CLEO-III collected ~ 9 fb\(^{-1}\), 70\% on the \(\Upsilon(4S)\)

- **November 2001-2002:**
  CLEO-III took data on the \(\Upsilon(1S), \Upsilon(2S), \Upsilon(3S)\)

- **2003-5:**
  CLEO will operate in the 3-5 GeV energy range.
  A proposal has been written.
  Recent \(\tau\)-charm workshop:
  http://www.lns.cornell.edu/public/CLEO/CLEO_C
CLEO III Silicon Detector Design Goals

- Integrated tracking system
  - SI measures z, cotθ,
  - Drift chamber measures curvature
  - Both detectors measure φ.

- Tracking of low momentum π’s require small radiation length of SI detector. < 2% X₀ achieved!

- Also required for good tracking:
  - Signal-to-noise larger than 15:1 in all layers
  - Resolution better than 15 μm in r-φ, 30 μm in z for tracking and secondary vertices (τ and D-mesons only, B’s have no boost)
  - 93% solid angle coverage (same as our drift chamber)