A transimpedance amplifier using a novel current mode feedback loop

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Abstract

We present a transimpedance amplifier stage based on a novel current mode feedback topology. This circuit employs exclusively NMOS and PMOS transistors and requires no capacitor to stabilize the transimpedance loop and no resistor for the transresistance feedback and transistor loading. This amplifier circuit is fully compatible with submicron digital CMOS processes. The active feedback network consists of two grounded gate MOS devices which split the output current in the feedback branch and the output branch. The transresistance and the phase margin are adjustable via external DC signals. The measured rise time of the impulse response of the amplifier implemented in an industrial 0.7 \mu m CMOS process is 18 ns for a transresistance of 180 k\Omega and 30 ns for a transresistance of 560 k\Omega. The measured Equivalent Noise Charge (ENC) is 800 rms e\textsuperscript{-} for an input capacitance of 20 pF with the transresistance adjusted to 560 k\Omega.

1. Introduction

Transimpedance amplifier designs with low noise and high speed characteristics are key components in many front-ends, such as optical data link receivers, smart pixel sensor amplifiers and preamplifiers for radiation detectors. The transimpedance configuration circuit is also an attractive approach for fast amplifiers for silicon drift detectors and silicon strip detectors at the LHC experiments. Several current sensitive preamplifiers for silicon strip detector applications have been designed in hybrid circuits with bipolar [1] and MOS [2] technologies. More recently, transimpedance preamplifiers have been designed in bipolar integrated circuit technologies [3–7].

The main features desired for fast front-end amplifiers are low noise, high gain and excellent frequency stability. Moreover, the development of front-end systems in radiation hard CMOS process [8–10] for the future LHC detectors and advances in deep submicron CMOS technology require design circuit techniques more and more compatible with digital CMOS processes. The active current feedback circuit principle presented in this paper, provides a means of improving speed performance of a transimpedance amplifier without sacrificing stability and noise and is fully compatible with digital processes. This novel circuit technique is very compact and enables to control the transresistance gain over a large range (1 to 10), via an external current, without affecting amplifier stability. The amplifier architecture can accept a DC input connection with a leaky sensor, such as silicon strip detector, without impairing its performance. This circuit does not require any additional passive components such as capacitors and resistors and is therefore compatible with deep submicron CMOS processes. Alternatively, the same circuit can be used to implement a high value feedback resistor (> 10 M\Omega) for a charge amplifier, by operating the active feedback at very low current.

The active feedback loop circuit principle is presented in Section 2, and is compared with the traditional transresistance feedback structure. In Section 3 the implementation of the active feedback in a transimpedance amplifier in CMOS technology is presented and crucial design issues are discussed. The first experimental results of the active feedback transimpedance amplifier are presented in Section 4, in particular the noise characteristics. Section 5 concludes on the future development of this circuit.

2. The active feedback principle

Fig. 1 shows a basic circuit diagram for a traditional CMOS or bipolar transimpedance amplifier. Low noise performance is ultimately determined by the parallel input noise current, that is inversely proportional to R\textsubscript{e}. Hence, from the point of view of noise, a high value of R\textsubscript{e} is...
desired, typically above 100 kΩ, to keep the parallel Equivalence Noise Charge (ENC) contribution below 500 μm electrons for a system peaking time of 25 ns to 50 ns. One important consideration is maintaining stability under all operating conditions. Major parasitic capacitances affecting the frequency response of the amplifier are shown in Fig. 1. Assuming that the Miller effect of Cm is negligible, the dominant and the second poles are given by:

\[ \omega_d = \frac{A_o}{C_{IN}R_f} \quad \text{and} \quad \omega_h = \frac{1}{C_i R_f}. \]

where \( A_o \) is the open loop voltage gain, and \( C_{IN} \) represents the detector capacitance, amplifier capacitance and the interconnect parasitic capacitance.

The stability of the amplifier modeled with a two-pole transfer function imposes a minimum phase margin of 58° and ideally more than 76°, requiring \( \omega_d \) to be at least 2.7 times larger than \( \omega_h \). In practice, such an amplifier design requires an additional feedback compensation capacitor to add a right-half-plane zero in order to keep the stability unaffected by the variations of \( R_f, R_i \) and \( C_{IN} \). The drawback of this compensation is a reduction of the amplifier gain–bandwidth product.

This problem is addressed by using an active feedback network based on two MOS devices MPf and MP0 as shown in Fig. 2. The transistor MPf is placed in the feedback path of the transconductance amplifier A at the place of the conventional feedback resistor and the transistor, MP0 loads the output node OUTV. Transistor MPf is in saturation and is biased close to weak inversion by the current source MI. Therefore, MPf acts as a cascode stage across the feedback path in such a way that it replaces the feedback resistor \( R_f \), and the load resistor \( R_i \) and does not require the buffer depicted in Fig. 1. It also maintains adequate biasing conditions of the amplifier A. An additional advantage is that it provides a supplementary current output OUTI.

The transconductance \( g_{ms} \), determines the effect feedback resistor \( R_f \), the effect load, resistor \( R_L \) and the mid-band gain \( A_o \) which can be expressed for weak inversion operation as:

\[ R_i = \frac{1}{g_{ms_i}} \quad \text{and} \quad A_o = \frac{g_{ms_o}}{g_{ms_i}} \quad \text{with} \quad \frac{g_{ms_i}}{g_{ms_o}} = \frac{q}{kT} I \]

where \( k \) is the Boltzmann constant, \( T \) the absolute temperature.

Thus, the dominant and the non dominant poles become

\[ \omega_d = \frac{A_o g_{ms_i}}{C_{IN}} \quad \text{and} \quad \omega_h = \frac{1}{C_i R_f}. \]

where \( \kappa = g_{ms_s}/(g_{ms_i} + g_{ms_o}) \). One can note that both poles can be controlled by \( \kappa \). If one assumes that the transistors pair formed by MPf and MP0 works in peak inversion, the drain currents and \( \kappa \) can be expressed as [8]:

\[ I_d = I_{sat} e^{-\frac{V_d}{V_{th}}} \quad \text{and} \quad I_i = I_{sat} e^{\frac{V_i}{V_{th}}} \]

with \( \kappa = \frac{1}{1 + e^{-\frac{V_o}{V_{th}}}} \).

where \( I_{sat} \) is the saturation drain current, \( V_i \) the voltage of the output node and \( V_o \) the drain voltage of MPf and MP0. Therefore, the phase margin controlled by \( \kappa \) can be adjusted by the differential voltage \( V_o - V_i \).

Assuming that the zeros introduced by Miller capacitances and the internal pole of the stage A are negligible, the gain of the transconductance amplifier can be modeled...
Fig. 3. Output pulse transient response of the active feedback amplifier. The circuit has been modelled for a 0.7 μm CMOS technology as a simplified second order system. K has been adjusted by V_c - V_n to obtain a phase margin of 70°. Time scale is in ns and amplitude normalised to 1.

as a second-order system which can be expressed by a two-pole transfer function:

\[ G(s) = \frac{V_{out}(s)}{I_{in}} = -\frac{1}{g_{ms} s^3} \frac{1}{g_{m2}g_{m1}} + \frac{1}{\kappa g_{m1} + 1}. \]  

(5)

For a phase margin between 58° to 78°, the roots of the denominator occur as complex-conjugate pairs. In this condition, the inverse Laplace transform of Eq. (5) for a step response has the following expression:

\[ G(t) = -\frac{1}{g_{ms} s} \left[ 1 - \frac{1}{1 - 4\xi^2} \sin \left( \omega_c t \sqrt{1 - \frac{1}{4\xi^2}} \right) + \arcsin \left( \frac{1}{4\xi^2} \right) \right]. \]  

(6)

where

\[ \xi = \kappa \sqrt{\frac{g_{m2} C_{IN}}{g_{ms} C_{IN}}} \quad \text{and} \quad \omega_c = \sqrt{\frac{g_{m2} g_{ms}}{C_{IN} C_{IN}}}. \]

The response of the amplifier to an input current impulse obtained by differentiation of Eq. (6) for typical parameters of a 0.7 μm CMOS technology and with an equivalent feedback resistance of 300 kΩ. A peaking time of 15 ns is calculated with a phase margin of 70° for C_n = 20 pF and g_m = 5 mS.

3. Low-noise transimpedance preamplifier with the active GE 5M feedback

The practical implementation of the active current feedback circuit is shown in Fig. 4. It uses the direct cascode configuration built with NMOS or NPN bipolar transistors T1 and T2. In the case of MOS devices the input transistor T1 is sized to match the sensor capacitance for minimum noise, whereas the aspect ratio of the cascode transistor T2 is chosen to reduce the parasitic capacitance on the output node. In the case of bipolar input, the transistor geometry is sized to keep the base spreading resistance negligible compared to the equivalent noise resistance of the collector shot noise.

We study here only the MOS version. The active current feedback loop is implemented by the PMOS transistor MP_t and the current source MI_p. With the load transistor MP_t, transistor MP_f acts as a cascode stage across the feedback loop and loads the output node with its source resistance 1/g_m, MP_f and MP_t sizes are close to the minimum size (C_in minimum) in order to keep g_m as high as possible. The adjustable current source MI_p biases MP_f close to weak inversion for a drain current in the range 50 nA to 1 μA. The mid-band input resistance of the active feedback transimpedance amplifier is determined by the ratio R_f/A = 1/g_m, which is not dependent on R_f.

The DC operating biasing of the amplifier, in Fig. 4, is set by three external voltage sources (V_CAS, V_i and V_o) and two external current sources (I_B and I_D). Drain voltage of T1 and T2 are entirely set by gate voltages V_i and V_CAS. The current balance I_f-I_D is set by V_o. This biasing scheme enables single rail, low supply voltage operation.

The setting and polarity of the input current source I_B defines three dynamic modes of amplification for the output OUTV:

1) Linear mode: when the input signal is sufficiently small compared to I_B then the amplification is practically linear (I_f → 300 nA and input charge ≤ 12 fC)

2) Square root compression: when the polarity of the input signal is negative and large compared to I_B, g_m varies like the square root of the input current (MP in strong inversion). Hence, the amplifier accomplishes a square root compression of the input signal.

3) Non-linear mode: when the polarity of the input signal is positive and I_B is sufficiently small (100 nA), the input signal forces the feedback current I_f to 0, switching MP_f off. Then the feedback is opened and the circuit is

VI. ELECTRONICS
configured like an open loop transconductance, which enhances the gain considerably (about a factor 10). This effect can be used to obtain a non-linear signal processing in such a way that signal and noise level below the switching threshold are dynamically compressed. This technique can be applied to decrease the noise hit rate of readout electronics for a binary system or sparse data scan readout system.

The current output OUTI delivers a linear output signal with a current gain, \(I_{out}/I_{in} = gms/gms_t\). This output can be used in current mode with a low impedance load or in integrating mode with a capacitive output node. In this case, the current output OUTI works like a charge amplifier output.

The noise contributions of transistors MP and MPc operating in weak inversion can be expressed from Eq. (2) as the power density of the noise current at the input:

\[
\langle n^2 \rangle_{in} = \frac{4kT}{gms_t} = \frac{1}{2} \frac{4kT}{R_i}.
\]

Hence, the total parallel input noise current is

\[
\langle n^2 \rangle_{in} = \frac{4kT}{R_i},
\]

which is equal to the noise of a traditional transimpedance amplifier. If the design could be optimised to operate MP and MPc in strong inversion with \(gms < gms_t\), the parallel noise is slightly improved. In this case the total parallel noise current is:

\[
\langle n^2 \rangle_{in} = \frac{4kT}{gms_t} = \frac{1}{2} \frac{4kT}{R_i}.
\]

Thus, the parallel noise is decreased by 30% when compared to a conventional feedback resistor. Noise analysis is done here assuming that the bulk transconductance associated with the bulk noise resistance of MP and MPc does not contribute to the noise. This assumption is justified because MP and MPc have a noise resistance larger than 100 k\(\Omega\), which is much higher than the bulk noise contribution of a small geometry transistor.

The series noise contribution of the active feedback amplifier is essentially identical to the conventional transimpedance or charge amplifier and is mostly determined by the noise characteristics of the input transistor T1. It can be noted that because of its high gain (10 mV/fC), this configuration exhibits a better robustness against second stage noise contribution than a fast charge amplifier.

4. Experimental results

The active feedback transimpedance amplifier circuit of Fig. 4 has been designed and fabricated in an industrial 0.7 \(\mu\)m CMOS technology. The T1 input NMOS device has a size of \(W/L = 2000 \mu\)m/1.2 \(\mu\)m and is biased at 400 \(\mu\)A. The MP and MPc transistors have a size of \(W/L = 2 \mu\)m/4 \(\mu\)m. The preliminary measured output pulse shape response for charge input of 1 MIP(4 fC) is shown in Fig. 5. The measurement has been performed with a test board presenting a minimum input capacitance of 10 pF. In these conditions the active feedback circuit shows an excellent stability. The adjustment of the phase margin with the differential voltage \(V_i - V_o\) has been verified and works as predicted. The results from experimental output pulse responses shown in Fig. 6 fully agree with SPICE simulations.

The transresistance of the active feedback circuit has been measured as shown in Fig. 6. The variation of the

\[\text{Fig. 5. Measured output transient pulse response for } I_i = 120 \text{ nA, 186 nA, 235 nA and 580 nA. The drain current of the cascode amplifier is 400 } \mu\text{A and } C_i = 10 \text{ pF. Rise time varies from 18 ns to 30 ns.}\]

\[\text{Fig. 6. Measured transresistance as functions } I_i. \text{ Result of the fit indicates that for } I_i \text{ above 200 nA, } R_i \text{ is not linear with } I_i \text{ but is a power function, because } MPc \text{ is working in medium inversion.}\]
transresistance by a factor of 3 from 190 kΩ to 580 kΩ is obtained for a $I_n$ variation of a factor 4.7, from 580 nA to 120 nA. This result is slightly different from the calculation of Eq. (2) which predicts a linear dependence. The reason is that the transistor $M_{P1}$ for $I_n$ above 200 nA, begins to operate in moderate inversion.

The Equivalent Noise Charge (ENC) shown in Fig. 7, has been measured as a function of the input capacitance for three different feedback currents and at bias current of the input branch of 400 µA providing an amplifier transconductance of 7 mS. For $C_{in} = 0$, a parallel noise $ENC_p = 250$ electrons rms is measured for the higher feedback resistance of 580 kΩ ($I_n = 120$ nA). The measured noise slope is 30 electrons rms/pF obtained for a rise time of 45 ns. When the same amplifier parameters are used to make the noise calculation for a charge amplifier followed by a CR-RC filter we obtain a noise slope of 32 electrons rms/pF and a value of $ENC_p = 200$ electrons rms at $C_{in} = 0$. The series noise difference can be explained by the rise time variation with the input capacitance, which decreases the measured noise slope. The difference of the calculated and measured parallel noise can be explained by the uncertainty on the absolute value of the total input capacitance, which in our test set up is 10 pF ± 1.5 pF. Taking into account these effects, experimental results and calculation agree very well.

5. Conclusions

A new active feedback technique for transimpedance amplifiers is presented. A CMOS amplifier circuit based on this novel technique has been designed and tested. This circuit employs exclusively n-channel and p-channel devices. The feedback resistance of the amplifier is adjustable from 150 kΩ to 700 kΩ via a DC current. The phase margin of the amplifier is precisely adjustable via a DC voltage. The measured transimpedance gain is 40 mV for an input charge of 25 000 electrons, with a peaking time of 45 ns for a transresistance of 500 kΩ. In these conditions, a total noise of 800 e rms is obtained for an input capacitance of 20 pF, making this circuit very promising for low noise and fast preamplifier applications. Comparable designs using radiation hard CMOS and BiCMOS technologies are in development. Preliminary simulations of these versions indicate the same circuit behavior with a faster rise time.

References