

Specifications for the IceRay Sampler (IRS) ASIC

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Abstract

We present the specifications and design concept for a waveform sampling ASIC tailored to the needs of an extended in-ice Askaryan-effect radio neutrino array. Compared with the LABRADOR3 ASIC flown twice on the ANITA payload, far deeper sampling (65,536 versus 256) is realized, permitting sub-threshold forced readout, which should extend both the reach and flavor-ID of a 10km scale detector.

Key words: Gigasample/s waveform digitization, radio neutrino detection

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1. Background

A first prototype IceRay detector [1] station was fabricated in 2007. It has not yet been deployed at South Pole. At that time the LAB3 ASIC [2], already having successfully flown on the first ANITA mission and also operated in AURA prototypes [3] in the IceCube array, were used. Inasmuch as each IceRay station can be treated as a “mini ANITA”, this is a reasonable choice. However the benefits of being able to read out antennas that might be below threshold to trigger were highlighted in studies of an embedded salt array [4].

Since that time further extensions and improvements to the LABRADOR waveform sampling

ASIC have been realized in a series of devices that explored deeper [5] and faster [6] sampling, on-chip encoding [7], and much higher bandwidth [8]. In particular, it has been pointed out that deep sampling can significantly enhance neutrino flavor identification by observing sub-threshold emission of the lepton during propagation through the array [9]. The required sampling depth for a full IceRay detector is of the order of the transit-time across the array, approximately 10km in length, or about $30\mu\text{s}$.

Specific ways in we plan to optimize the waveform sampler performance to match the needs of IceRay are

- 64k deep sampling on each channel
- improved input bandwidth
- reduced cross-talk
- faster readout

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2. System Overview

An overview of a composite IceCube + IceRay event is illustrated in Fig. 1.

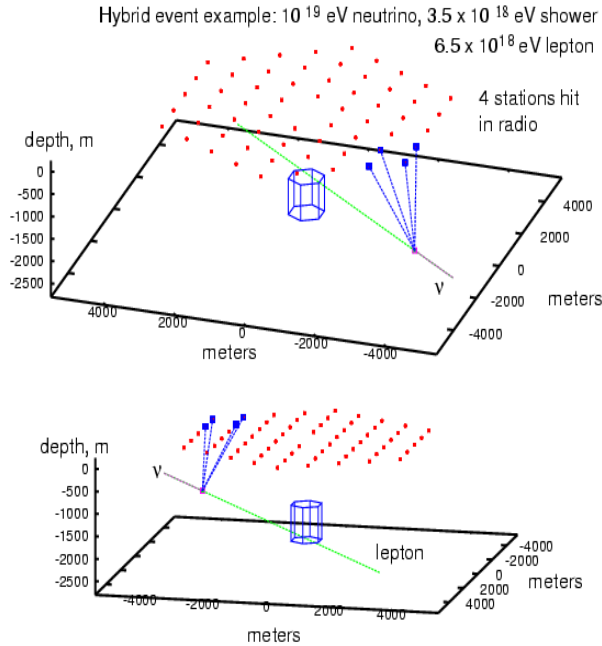


Fig. 1. Overview of one possible IceRay configuration, where a hybrid event with IceCube is illustrated. Each red dot represents a detector station. Improved flavor ID is obtained by reading out each station, even if below self-trigger threshold.

Each station consists of an array of antennas and supporting amplifiers and EMI-shielded read-out housings. The geometry considered for an initial prototype deployment is illustrated in Fig. 2, where it should be noted that future deployments would benefit from embedding the antennas further into the ice (below the firn layer).

Details of the support electronics are sketched in Fig. 3, where the existing LAB3 digitizer ASICs may be seen. While the layout for a new ICRR to support the IRS ASIC will need to change, electrically it is very similar to that shown here.

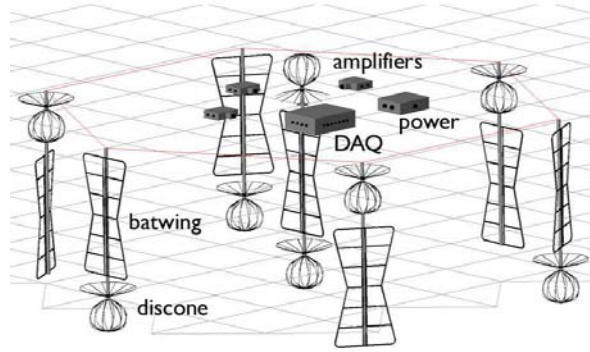


Fig. 2. Layout of an IceRay prototype testbed station.

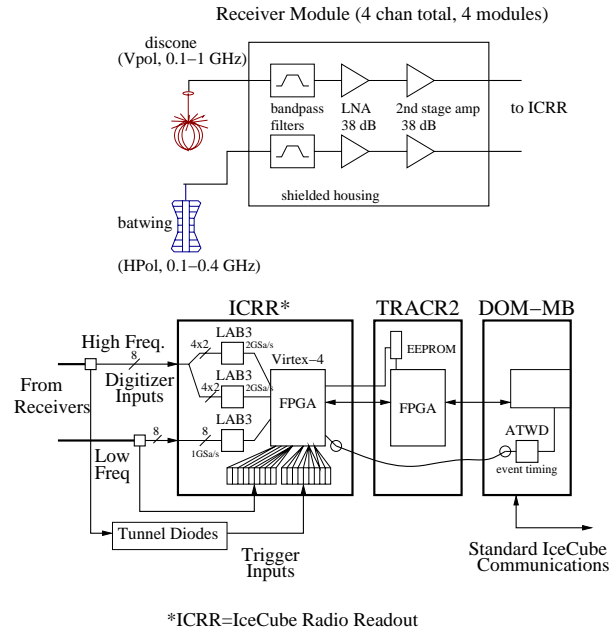


Fig. 3. Layout of an IceRay prototype testbed station.

3. Specifications

In order to meet the requirements mentioned above, an Application Specific Integrated Circuit (ASIC) is being designed to the set of specifications listed in Table 1. An acronym indicative of its functionality has been chosen: the IceRay Sampler (IRS). Of note in this description table is the storage depth, which provides for greater than $65\mu\text{s}$ storage. Moreover, it is possible to cascade IRS ASICs and extend this value to even deeper values.

Table 1
Key Specifications of the IRS ASIC.

Parameter	Value	Comment
Number Channels	8	1 chip/antenna type
Storage cells/channel	65,536	2^{16} total
Timing Strobe	1	Array synchronous
Analog bandwidth	$\geq 1\text{GHz}$	depends on antenna
Sampling Rate	1 – 2 GSa/s	adjustable
Conversion cycle	$\leq 1\mu\text{s}$	for 512 samples
Local hit latency	$\approx 10\mu\text{s}$	for $8 \cdot (256)$ samples
Local event size	$\approx 4\text{kBytes}$	per IRS
Full chip readout	$\approx 12.5\text{ms}$	for $8 \cdot 64\text{k}$ (512k) samples
Max event size	$\approx 1\text{MByte}$	per IRS

Synchronous sampling is provided at each station. Currently synchronization between stations is provided by GPS 1PPS marker, though future deployments may use a dedicated fiber link.

4. Concept Implementation

In the following subsections we describe the circuit subcomponents we have evaluated and chosen, as well as calculations and/or simulations of the expected performance. A conceptual summary is presented in Fig. 4, with key blocks in white board “brainstorm” mode.

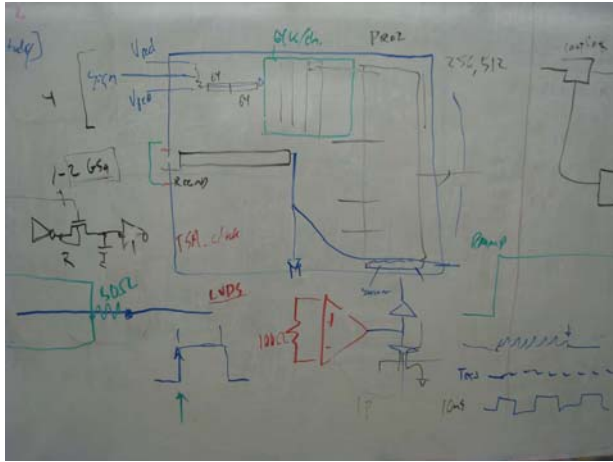


Fig. 4. Sketch of the IRS concept details.

4.1. Input Coupling

Achieving improved analog bandwidth requires a better understanding of both the integrated circuit and board implementation. The latter is crucial though beyond the scope of this paper. From previous experience in similar waveform sampling devices [2,5], we expect that wire bonding will limit performance.

A simple representation of the coupling from the photosensor into one of the storage channels of the IRS is represented in Fig. 5. At the left is the physical circuit representation. At right, the impedance of the input capacitance (C_T) is in parallel with the termination resistor (R_T), $Z_T = R_T + Z_C$ and $R_T = 50\Omega$.

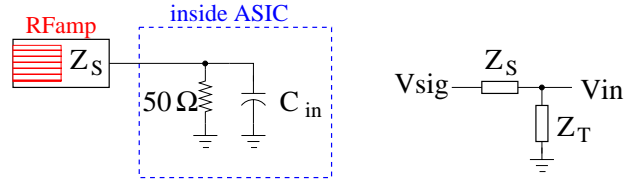


Fig. 5. Simple model of input coupling. At left the physical components, at right the simplified schematic representing the relevant low-pass filter that models the input coupling response.

Using the expression for an impedance divider,

$$V_{in} = \frac{Z_T}{Z_S + Z_T} \cdot V_{sig} \quad (1)$$

we can express the gain of the circuit:

$$\text{Gain} = G = \frac{Z_T}{Z_S + Z_T} = \frac{R_T || Z_C}{Z_S + R_T || Z_C} \quad (2)$$

where $R_T || Z_C$ can be reduced as

$$R_T || Z_C = \frac{\frac{R_T}{j\omega C_{in}}}{R_T + \frac{R_T}{j\omega C_{in}}} = \frac{1}{\frac{1}{R_T} + j\omega C_{in}} \quad (3)$$

The gain can then be expressed as

$$G = \frac{\frac{1}{\frac{1}{R_T} + j\omega C_{in}}}{Z_S + \frac{1}{\frac{1}{R_T} + j\omega C_{in}}} \quad (4)$$

which can be simplified by multiplying through by $\frac{1}{R_T} + j\omega C$ and taking $Z_S = 50\Omega$, yielding

$$G = \frac{1}{R_S \left(\frac{1}{R_T} + j\omega C_{in} \right) + 1} = \frac{1}{1 + \frac{R_S}{R_T} + j\omega R_S C_{in}} \quad (5)$$

In the limit $\omega \rightarrow 0$ the gain is simply the expression

$$G = \frac{1}{1 + \frac{R_S}{R_T}} \quad (6)$$

and for a matched impedance: $R_S = R_T$ obtain $G = \frac{1}{2}$. This static gain factor is always present, in terms of the usual expression for a low-pass filter, we factor out the static resistive divider and define $G = 1$ as $\omega \rightarrow 0$. In this case, the expression simplifies to

$$G = \frac{1}{1 + j\omega R_S C_{in}}. \quad (7)$$

Taking the magnitude of the Gain:

$$|G| = \frac{1}{\sqrt{1 + (\omega R_S C_{in})^2}} \quad (8)$$

where $\omega = 2\pi f$. The frequency dependence as a function of f for $C_{in} = 300\text{fF}$ and $R_S = 50\Omega$ is seen in Fig 6 below.

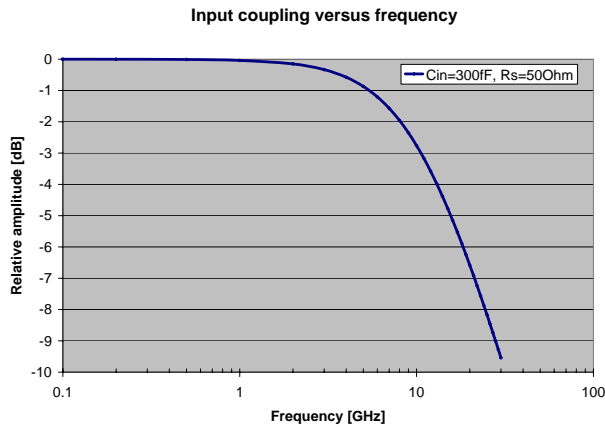


Fig. 6. Input gain into the ASIC as a function of analog bandwidth.

Taking the usual convention that the analog bandwidth is defined by the point where the amplitude of the coupled signal has dropped by 3dB. By inspection of Fig. 6, it is seen that this point is about 10GHz for the assumptions taken. Inspecting the expression for gain, this -3dB point

corresponds to the value where the amplitude has dropped to $\frac{1}{\sqrt{2}}$ of its value. This occurs under the condition where

$$\omega R_S C_{in} = 1 \text{ or } 2\pi f_{3\text{dB}} = \frac{1}{R_S C_{in}} \quad (9)$$

which then reduces to the familiar expression

$$f_{3\text{dB}} = \frac{1}{2\pi R_S C_{in}} \quad (10)$$

For a source impedance of 50Ω , the dependence on the input capacitance is shown graphically in Fig. 7.

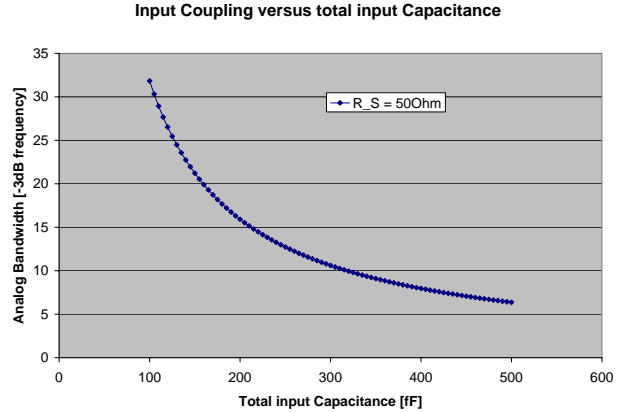


Fig. 7. Analog bandwidth versus input capacitance (C_{in}).

Finally, for an input capacitance C_{in} of 300fF, the analog bandwidth dependence upon source impedance R_S is plotted in Fig. 8.

Depending upon the actual source impedance realized for the photodetector, it may be necessary to use an RF amplifier upstream of the device, in which case the 50Ω point is the relevant point for comparison.

4.2. Packaging Effects

The attainable maximum input coupling frequency of the ASIC will be degraded when actually packaged. In particular the lead inductance can and will limit analog bandwidth. This reality modifies the simplified input schematic of Fig. 5 as shown in Fig. 9, with the addition of an inductance representing the package input connection.

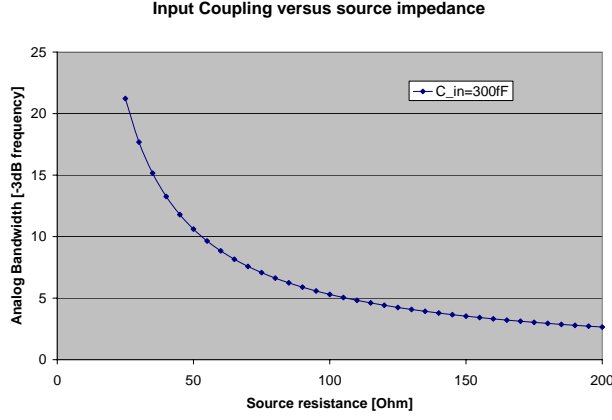


Fig. 8. Analog bandwidth versus source impedance (R_S) for a total input capacitance of 300fF.

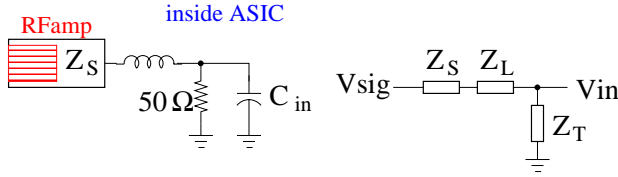


Fig. 9. Modified version of the simplified input circuit for evaluating in coupling to ASIC.

Addition of the bump bond or bonding wire adds a frequency-dependent reactance to the input. Also, in combination with the available capacitances, can lead to resonance structures as a function of frequency. The expression for this reactance is

$$Z_L = j\omega L \quad (11)$$

and the magnitude of which is evaluated as

$$|Z_L| = 2\pi fL \quad (12)$$

and the equivalent resistance of which is plotted for a typical bond-wire (5nH) and bump bond (0.2nH) in Fig. 10. Already at 2GHz, the effective impedance of the bonding wire has become comparable to the termination resistance, thus reducing the signal available on the input, as well as causing an impedance mismatch for a matched source resistance.

At the same time the signal amplitude is already rolling off due the reactance of the input capacitance. To estimate the effect, we can pick up the line of reasoning that lead to Eqn. 7, where now

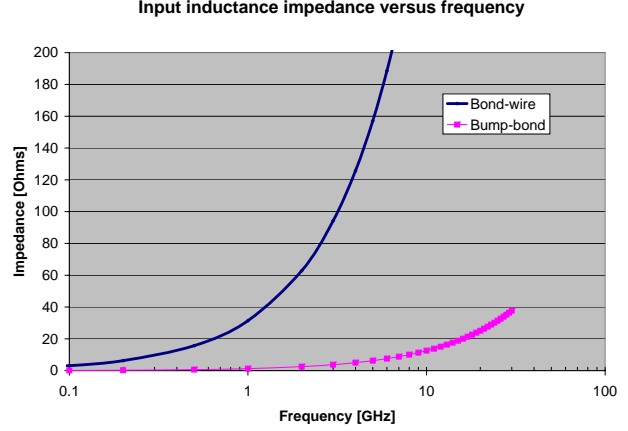


Fig. 10. Impedance of typical input connections as a function of frequency.

we instead replace R_S with $Z_{in} = R_S + Z_L$. Doing so leads to the following expressions for the gain

$$G = \frac{1}{1 + j\omega C_{in}(R_S + j\omega L_{bond})} = \frac{1}{1 + j\omega C_{in}R_S - \omega^2 L_{bond}C_{in}} \quad (13)$$

$$= \frac{1}{(1 - \omega^2 L_{bond}C_{in}) + j\omega C_{in}R_S} \quad (14)$$

Again, taking the magnitude

$$|G| = \frac{1}{\sqrt{(1 - \omega^2 L_{bond}C_{in})^2 + (\omega C_{in}R_S)^2}} \quad (15)$$

Inspecting this expression, it is interesting to note that there is a resonance condition in the case where the squared term in the left bracket vanishes. That is, when

$$\omega^2 L_{bond}C_{in} = 1 \quad (16)$$

Solving for the frequency, we obtain the familiar expression for an L-C oscillator:

$$f_0 = \frac{1}{2\pi\sqrt{L_{bond}C_{in}}} \quad (17)$$

For our two bonding interconnect conditions, assuming $C_{in} = 300$ fF this becomes

$$f_0^{wire} = 4.1\text{GHz} \quad \text{and} \quad f_0^{bump} = 20.5\text{GHz} \quad (18)$$

Actually, to treat this properly, both the signal and reference pad inductances need to be considered. As the inductance of these depends upon the

actual number of reference bonds, a more refined estimate will be attempted later, when other realities are addressed. To get a feeling for this modified gain, we again evaluate Eqn. 15 versus frequency in Fig. 11.

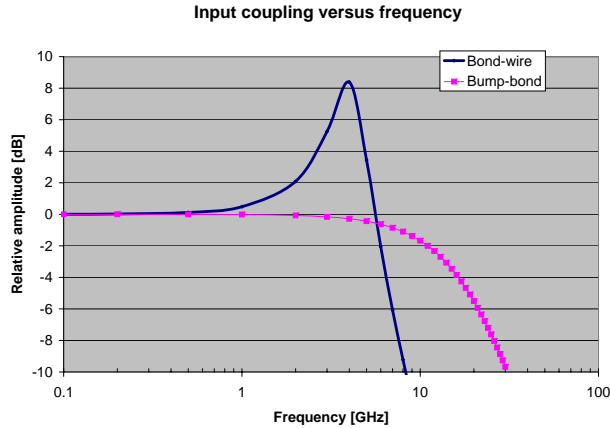


Fig. 11. Input coupling versus frequency for the modified gain due to the addition of inductance due to lead interconnect. Very strong peaking is seen for the bonding-wire case.

The dramatic peaking seen for the bonding wire case is likely to be less prominent in the actual circuit realization due to the reference voltage (termination voltage), as well as effects mentioned next. First it is noted that this expression can be rearranged and solved for the f_{3dB} expressions as was done previously. However, the simplification made to highlight the possibility of resonance on the input coupling was to consider the short-cut that took us from Eqn. 5 to Eqn. 7 is invalid. With the inclusion of the inductor impedance, this assumption breaks down. The term can be inserted, but the complexity of the algebra begins to obscure the pedagogical value of this exercise. Therefore for subsequent full analysis, the SPICE simulation tool will be used to extract results. However it is useful to sanity-check those results compared with these simple estimates. Before throwing everything into a black box, it is useful to perform one additional analytic estimate – that of the input coupling of each storage cell.

4.3. Storage Cell Coupling

Coupling into the storage cell is identical to the simplified earlier case of a low-pass filter presented earlier. When the storage switch is closed, it is characterized by an “on” resistance (R_{on}) and connected to a storage capacitor (C_{store}). The gain is then

$$|G| = \frac{1}{\sqrt{1 + (2\pi R_{on} C_{store})^2}} \quad (19)$$

and the frequency dependence is plotted for 4 representative values of the 2 parameters in Fig. 12. It is interesting to note that these correspond to scaling the previous input coupling case by a factor of 20 (100) in source resistance, leading to a similar scaling in the product for the capacitance at an equivalent -3dB frequency.

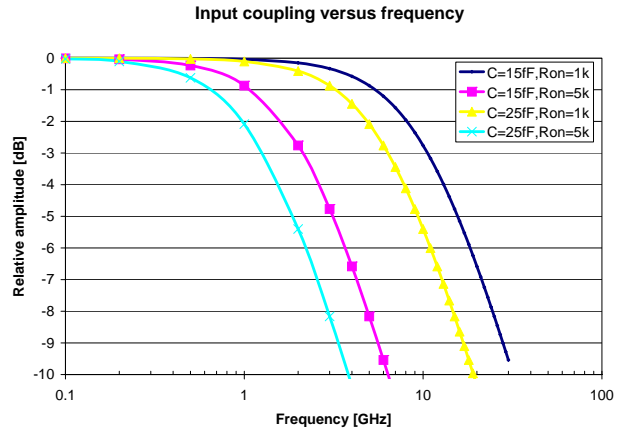


Fig. 12. Input coupling into storage cell for 4 possible switch on resistance and storage cell capacitance configurations.

So obviously we desire to keep the storage capacitance as small as possible. However there is a clear limit to how far this can be taken. That is, counting statistics on the thermal fluctuations in the small number of electrons representing a voltage on this small storage capacitor. This so-called “kTC” noise can be expressed as a voltage fluctuation in what actually get stored when the storage capacitor switch closes:

$$v_{rms} = \sqrt{\frac{k_B T}{C}}. \quad (20)$$

For a 1V nominal dynamic range, this limitation in effective number of bits of resolution as a function of storage capacitance is seen in Fig. 13.

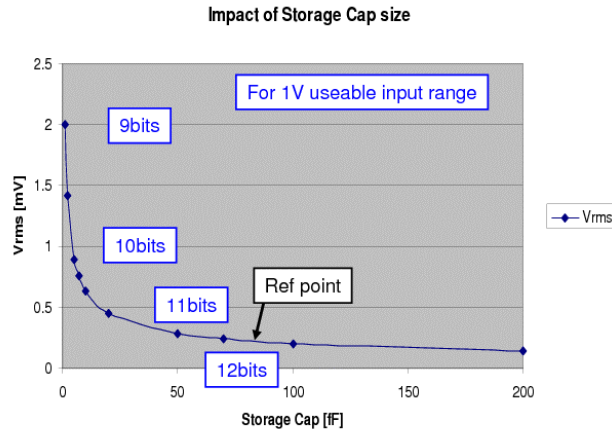


Fig. 13. Dynamic range limitation versus storage capacitance for a nominal 1V storage range.

Below an estimate for the actual storage capacitance of the proposed circuit is used.

4.4. Overall Signal Coupling

The resultant ability to couple in the analog signal depends upon the effects described in the previous two subsections. It is worth emphasizing that if each stage independently degrades the signal by 3dB, the effects are cumulative. Therefore the net result is the crucial one.

5. Simulated Performance

We evaluate by SPICE the expected input performance, modelling the input as precisely as possible. This lumped-element model is certainly lacking in the accuracy one might get from a 3-D EM simulation of the transmission line characteristics of the printed circuitboard and coupling into the ASIC. However it is as detailed a simulation of time and financial constraints permit.

5.1. Throughput coupling

Fig. 14 represents the circuit model of the input coupling.

Fig. 14. Input coupling circuit model for the IRS ASIC.

5.2. Flash Conversion Encoding

In order to speed the readout and reduce the programmable logic resource requirements for implementation of a large number of channels, a flash encoding scheme [7] has been implemented. The timing sequence for each of the conversion channels is displayed in Fig. 15.

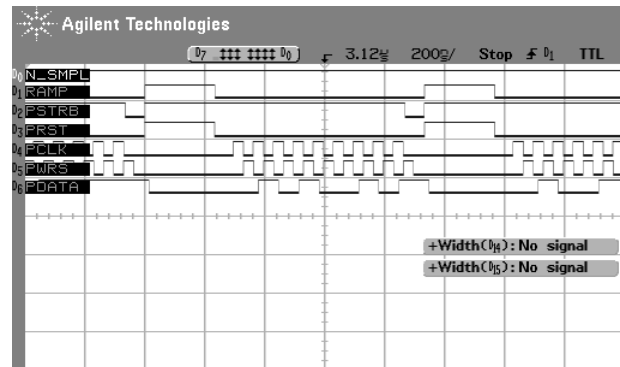


Fig. 15. Fast storage conversion timing diagram.

6. Initial Evaluation System

The evaluation system will initially consists of a small circuitboard, containing a wire-bonded IRS ASIC. It will be read out over USB2.0 by a laptop running a custom data acquisition program based on the wxWidgets tool kit. A photo of similar and previous compact measurement system is displayed in Fig. 16. This compact configuration can turn any PC (or laptop) into a high-performance digital signal oscilloscope.

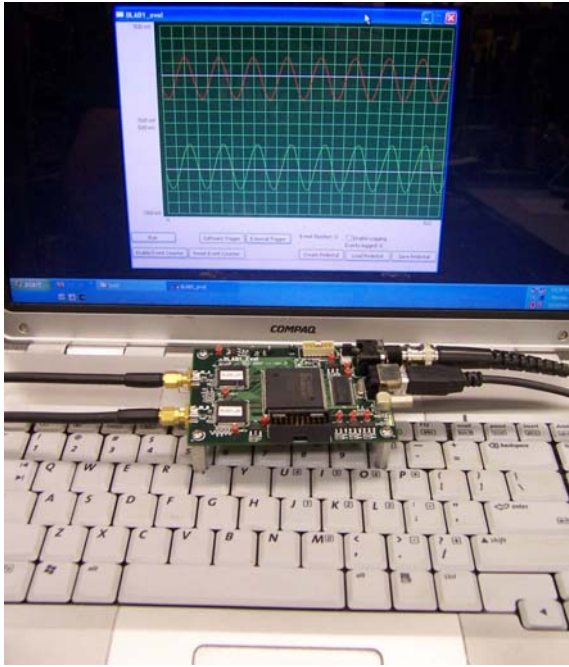


Fig. 16. Photograph of the “oscilloscope on a chip” test set-up, where the sampler ASICs are at the left, near the SMA input connectors.

7. Performance Results

This section to be completed when the test results become available. For now there are reference plots from BLAB2 as placeholders.

7.1. Sampling Rate

One technique experimented with in this version was that of using each stage of the inverter chain as a sample time reference. The power of this potentially allows for significant sampling speed increase in the same process used for BLAB1 [5], and measurement of the sampling pointer speed is reported in Fig. 17.

An example of how the rows of 1024 samples are stitched together for continuous sequencing is found in Fig. 18.

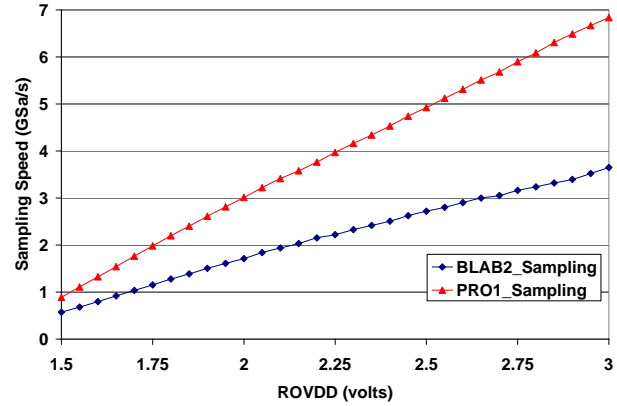


Fig. 17. Measured effective sampling speed of the two reference timing chains...

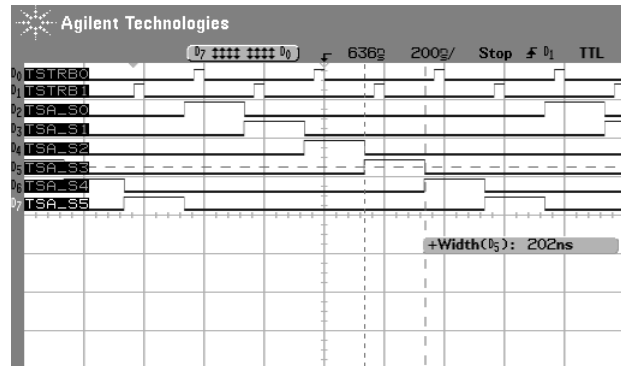


Fig. 18. Recorded overlap sampling of the rows of samples...

7.2. Calibration

As have been noted, the sampling speed of these devices is intrinsically the temperature dependence [5,2]. By monitoring the reference timing chains mentioned above it is possible to make these effects essentially unmeasurable for slow drifts.

Fig. 19. Event-by-event sampling speed comparisons of two BLAB1 ASICs indicating a common temperature dependence term. The sampling speed is continually monitored and used in calibration to achieve the maximum timing performance.

In order to address bin-by-bin timing width differences, a couple of different calibration techniques have been tried. The first utilizes a sine wave zero-crossing technique used for calibrating the LAB3 ASIC[2]. That technique works best

when the frequency of the sine wave is such that the measured interval between zero crossings can be uniquely assigned to a limited number of bins between successive crossings.

Fig. 20. Aperture width determination for individual sample cells via the histogram occupancy technique described in the text.

Due to sine wave curvature, this technique has an irreducible systematic error that is a function of sample rate. A more successful technique is to histogram the zero crossings of a sine wave and use the bin occupancy to derive the effective aperture width, as may be seen in Fig. 20.

When a sampling strobe is inserted into the BLAB1, the strobe propagates across a Switched Capacitor Array (SCA) row and exits the ASIC via a monitor pin. The sampling speed is determined by measured this propagation delay, a method implemented by creating a feedback loop with the insertion-extraction chain and an inverter located inside the companion FPGA. This feedback inverter is only connected after waveform readout of a triggered event and then disconnected once the sampling speed has been measured for that particular triggered event. A so-called Ripple Carry Out (RCO) period may then be expressed as

$$T_{\text{total}} = 2 * (T_{\text{latency}} + T_{\text{waveform}}) \quad (21)$$

where the factor of 2 comes from the FPGA feedback inverter toggling the RCO period, T_{waveform} is the SCA propagation time, and T_{latency} is the additional time accrued due to internal FPGA routing, circuit board routing, and routing to and from the SCA within the ASIC. To measure T_{total} an FPGA-based Time-to-Digital Converter (TDC) is used [10]. Both phases of a 250 MHz clock are used by the TDC to obtain a least count of 2ns. Improved resolution is obtained by integrating the RCO period for 2048 cycles, corresponding to an aggregate single-cycle least count of 0.977 ps. T_{latency} is obtained by subtracting T_{waveform} from T_{total} , where T_{waveform} is determined from a fit to a fixed frequency sinusoidal signal. The sampling speed is then

$$f_{\text{SPD}} = (T_{\text{waveform}}/\text{Rowlength})^{-1} \quad (22)$$

where f_{SPD} is the sampling speed and Rowlength is the number of SCA cells in a row, which for the BLAB1 ASIC is 512 cells. As reported in Ref. [5], the sampling timebase is temperature dependent. This effect may be seen as the correlated portion of Fig. 19. By measuring the BLAB1 timebase, these timebase shifts can be monitored and corrected of-line.

7.3. Pixel Level Noise

In order to achieve the desired timing performance, the Signal-to-Noise Ratio (SNR) is crucial. As the signal gain is limited (for aging and BW limitations), it is important that reasonable noise levels be obtained. The measured noise for a single pixel, which is very representative of the ensemble average, is displayed in Fig. 21.

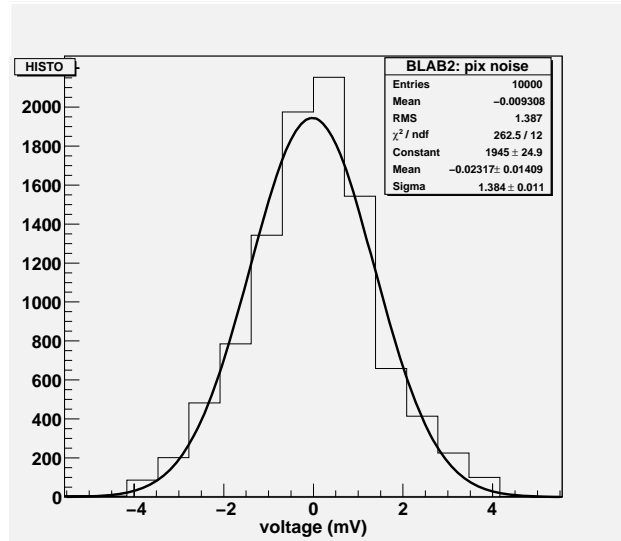


Fig. 21. Measured noise for a single pixel.

7.4. Linearity

In addition to having low noise, it is also important that the linearity of the sample conversion be of high quality. In Fig. 22 is shown the basic response of the converted values versus input values (amplifier output is offset to about 1300mV).

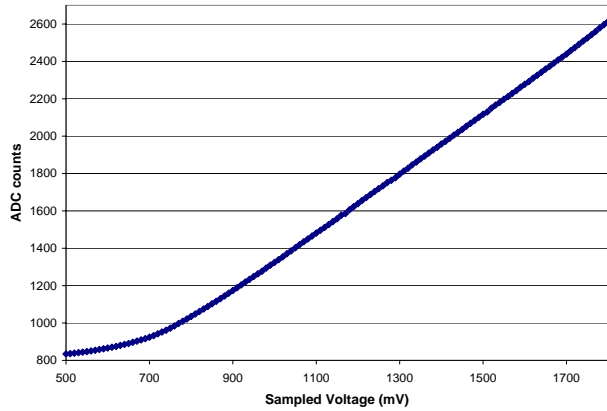


Fig. 22. Transfer response of the stored voltage values.

A linear fit to the main (usable) part of the curve is made and the residual is plotted in Fig. 23.

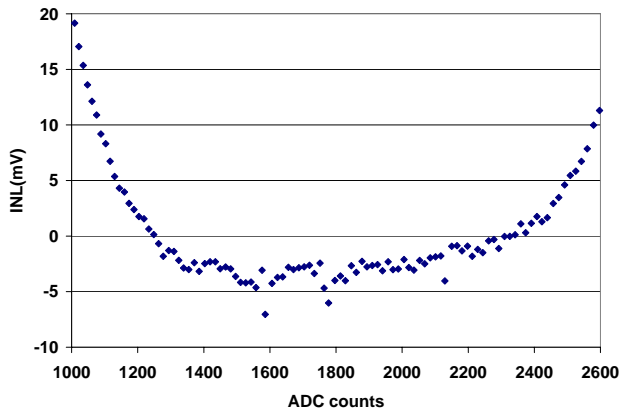


Fig. 23. Simple linear residual for the main part of the transfer curve.

Because it is computationally more efficient, a Look Up Table is applied to the data that corrects the residual non-linearity at the edges of the comparator dynamic range.

7.5. Frequency Response

Another critical component of excellent timing precision is the ability to couple in the high-frequency components of the signal of interest. In BLAB2 a number of configurations were tried to evaluate their relative coupling performance. The variation in frequency response is plotted in Fig. 24.

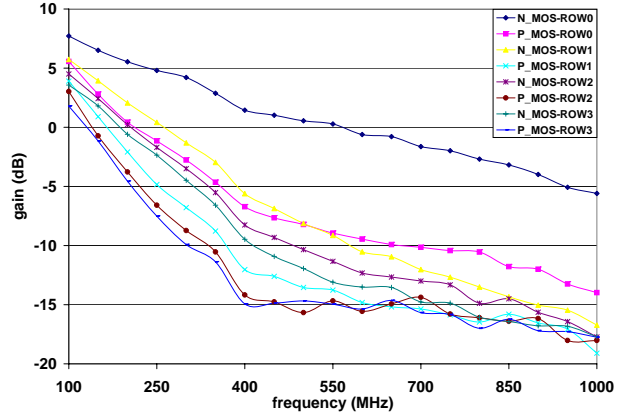


Fig. 24. Frequency response of various storage configurations in the BLAB2 ASIC. Positive gain is seen at lower frequencies due to the input TIA.

7.6. Analog Crosstalk

As a practical matter, the possible interference from nearest neighbor channels, strongly observed in the LAB3 ASIC [2] can be important. A measurement of the observed signal level in Channel 2 as a function of input frequency in Channel 1 is plotted in Fig. 25.

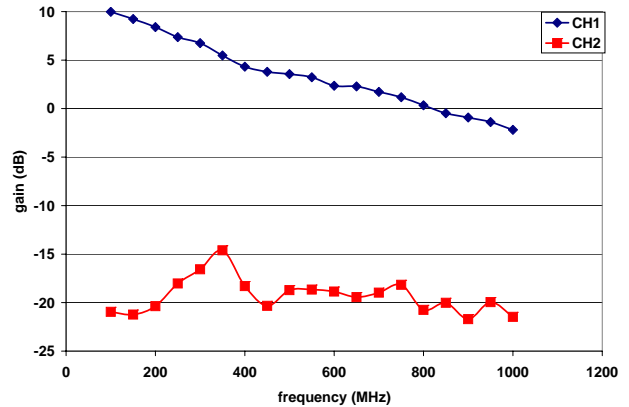


Fig. 25. Observed crosstalk signal in channel 2 as a function of RF sine frequency signal amplitude in channel 1. A modest though interesting resonance is seen at about 350MHz.

7.7. Fast on-chip ADC

In order to speed up the digitization clock, one option is to use the PRO [7] technique ...

The ramp speed is increased in this case and the sampling of the timing edge is produced via a delay chain with effective sampling speed given in Fig. 17.

In this case the measured noise increases for a ramp of **100ns??** as may be seen in Fig. 26

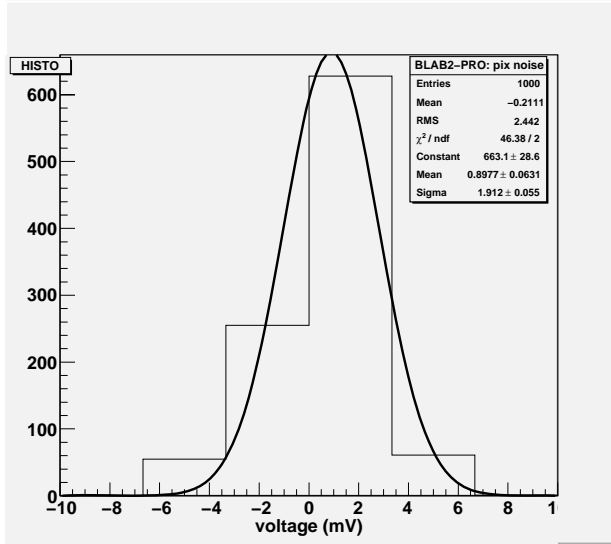


Fig. 26. Measured pixel noise when the so-called “PRO” readout encoding is used, which increases over the off-chip encoder though runs almost an order of magnitude faster.

The raw linearity of this flash encoder is shown in Fig. 27, and the linear fit residual is presented in Fig. 28.

Another issue discovered during the use of fast ramping mode is that there is a net baseline shift across the array when performing multiple, fast successive conversions. This effect is seen in Fig. 29. Operation with a slower ramp ... should help???

8. Expected Limitations

While the analog bandwidth of the BLAB1 is adequate for many RF recording applications, a higher bandwidth device will be explored, based upon the lessons learned from this first device. In

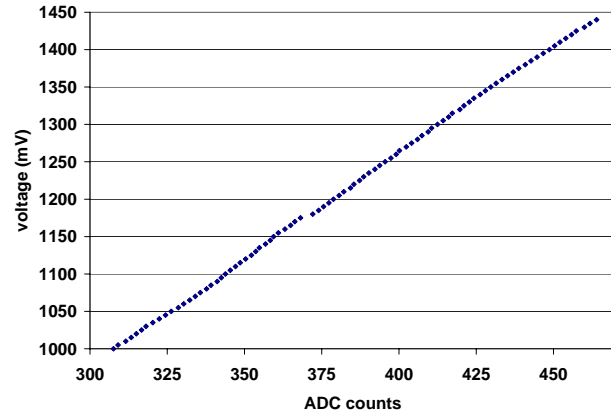


Fig. 27. Measured linearity of so-called “PRO” readout encoding, where it is noted that due to offset issues only a small portion of the encoding range could be used.

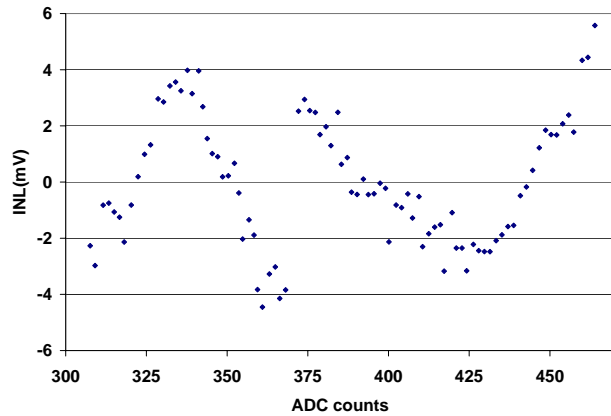


Fig. 28. Measured residual after linear fit to the “PRO” readout encoding, where again the dynamic range is limited by operating parameters of the input sampler offset.

particular, the fanout structure and design of the analog amplifier tree is being scrutinized and improved in simulation. It is hoped that an almost arbitrarily large storage depth can be accommodated up to 1GHz of analog bandwidth through a careful layout of the buffer amplifier cascade array.

8.1. Sampling Timebase Jitter

While the pedagogical illustrations above are helpful in understanding what limits the time resolution that can be obtained, there is an additional contribution that is an artifact of the use of

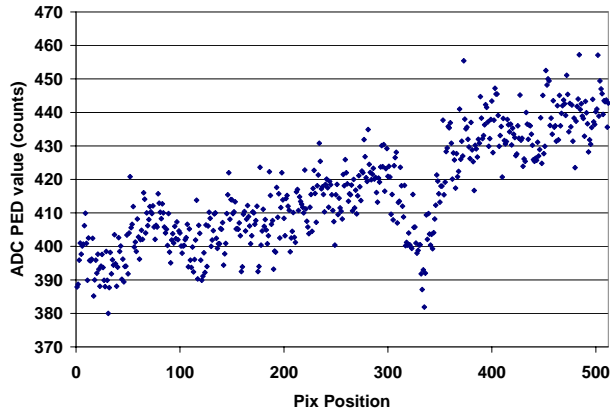


Fig. 29. Baseline shift observed as a function of samples digitized across the array. Such a shift is not observed when using the external (FPGA-based) TDC.

the BLAB1 ASIC. Specifically, it contains no dedicated Delay Lock Loop (DLL) circuitry, and thus the sampling timebase is sensitive at the level of about $0.2\%/^{\circ}C$ [5]. Even though an event-by-event correction is performed, as described previously, it is quite probable that a residual correction error contributes to the time resolution. A simulation is performed as shown in Fig. 30, where 1mV of noise is added in quadrature with 1ps of sample aperture jitter on top of an overall event-by-event sampling timebase jitter. This jitter is assumed to be uncorrelated between the two ASICs.

Fig. 30. Time resolution with 1mV noise, 1ps of sample jitter, and as a function of event-by-event uncorrected timebase jitter.

In the limit that the known 1mV noise only contributes 2ps to the overall time resolution and that the sample aperture jitter is negligible, this effect is seen to be dominant. Quantitatively, this corresponds to about a 10% error on correcting the event-by-event sampling timebase. If true, this can be improved through better timebase stabilization in a next version of the ASIC [5], or through the use of other devices as described next.

9. Summary

The IRS ASIC will represent a significant extension of the capabilities of an IceRay detector and this document provides those specifications.

10. Acknowledgements

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