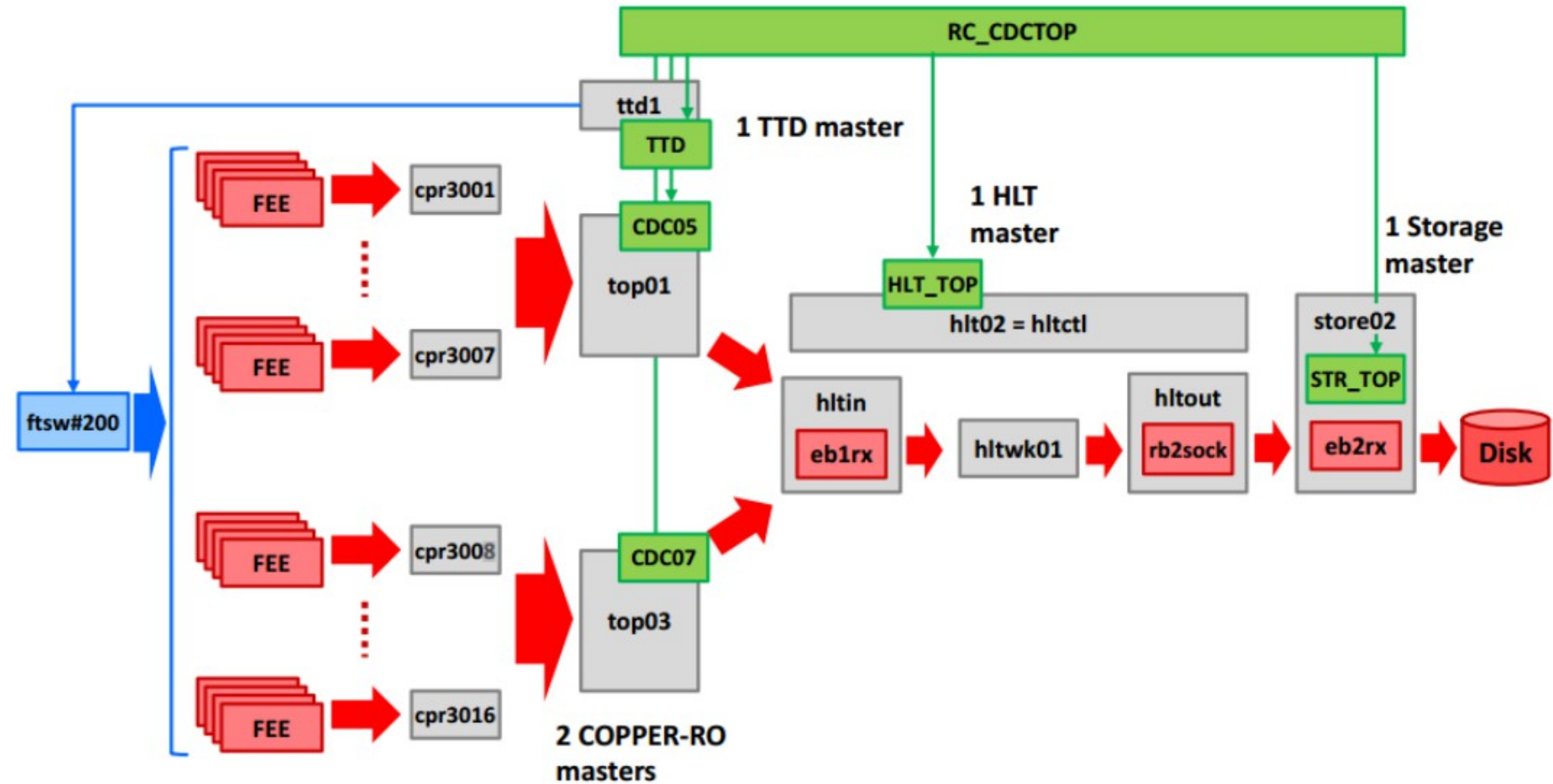
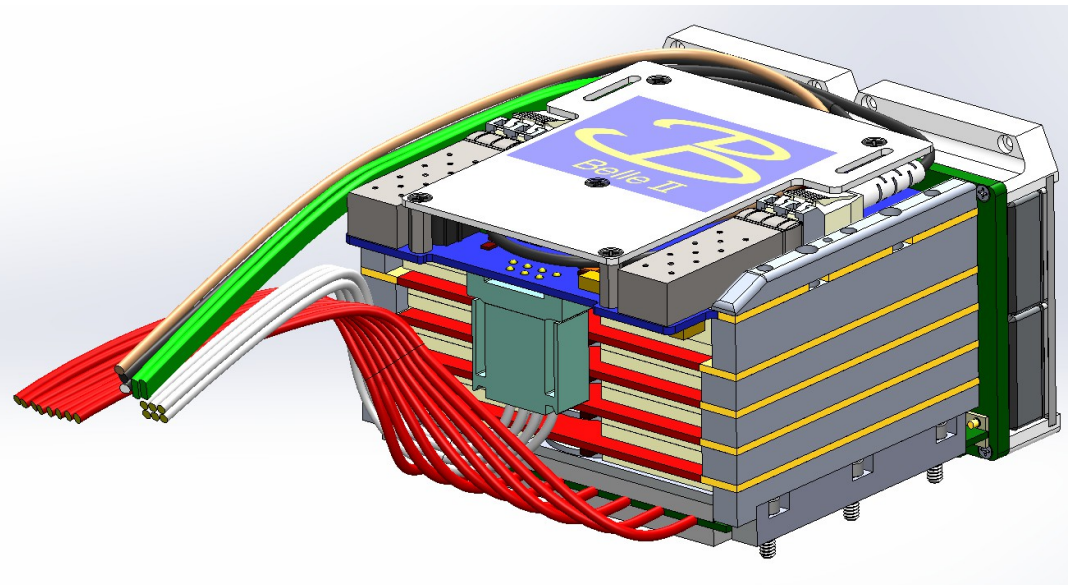
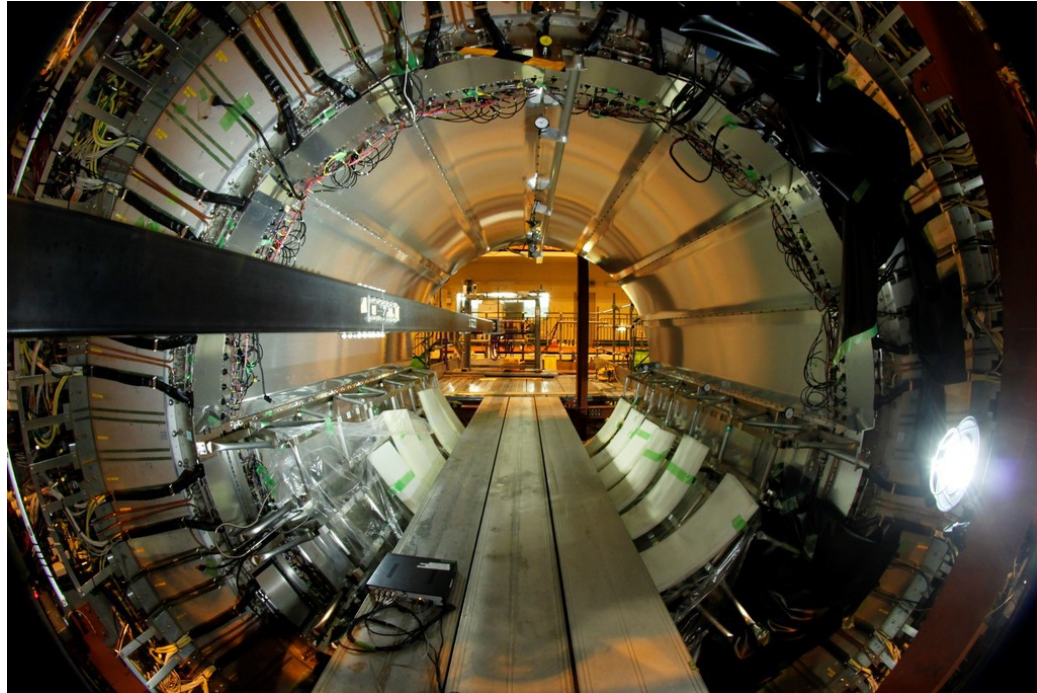


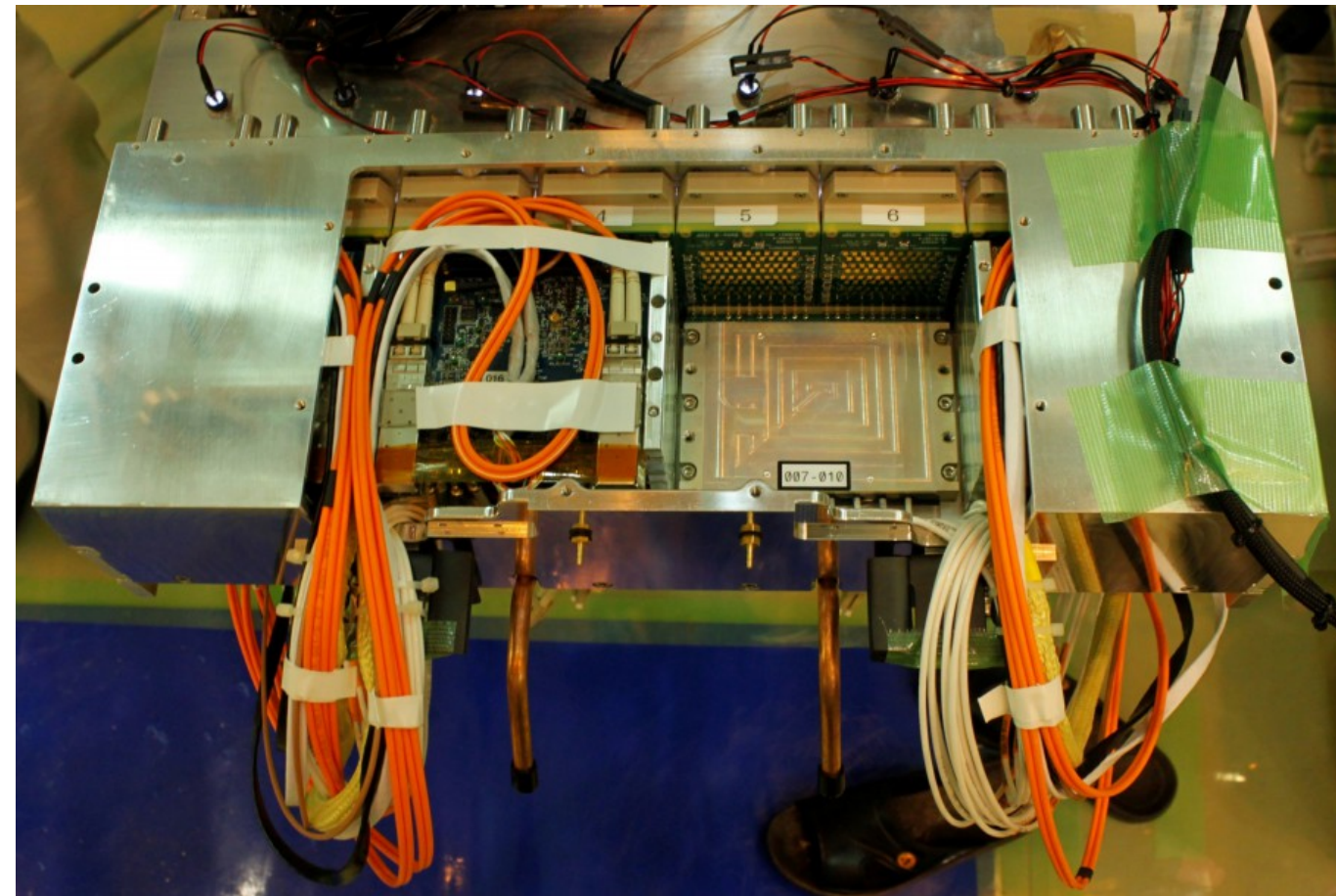
TOP TRG/DAQ status



2016-09-07 updated with text of responses from DAQ members

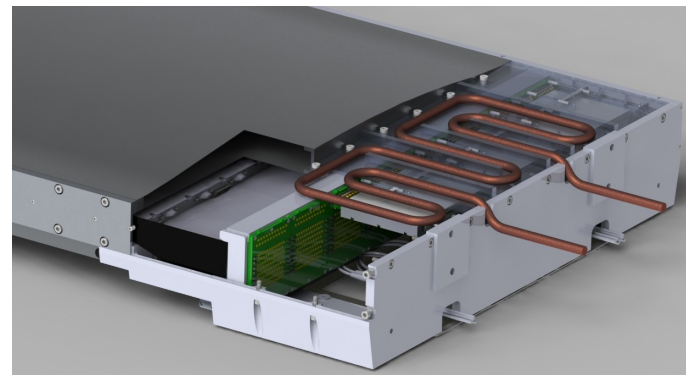
environment monitoring

- via snmp:
 - Wiener LVPS (192 currents, 384 voltages)
- via TCP/IP socket:
 - Caen HVPS (512 currents, 512 voltages)
- via copper local bus / hslb / fee:
 - humidities (1/scrod)
 - temperatures (20/scrod)
 - voltages (74/scrod)
 - currents (37/scrod)



interlock

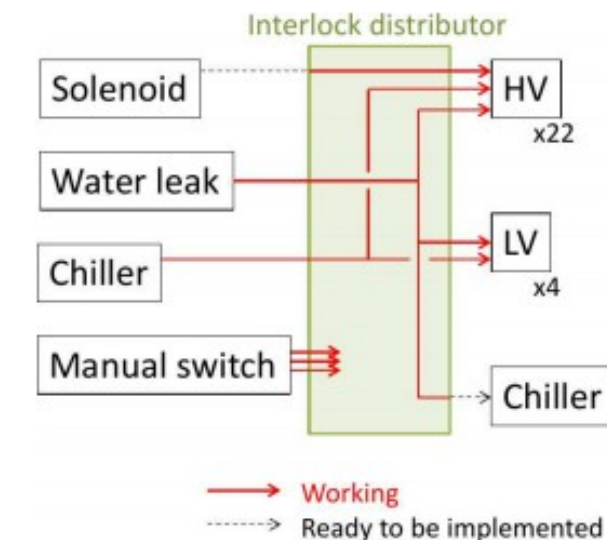
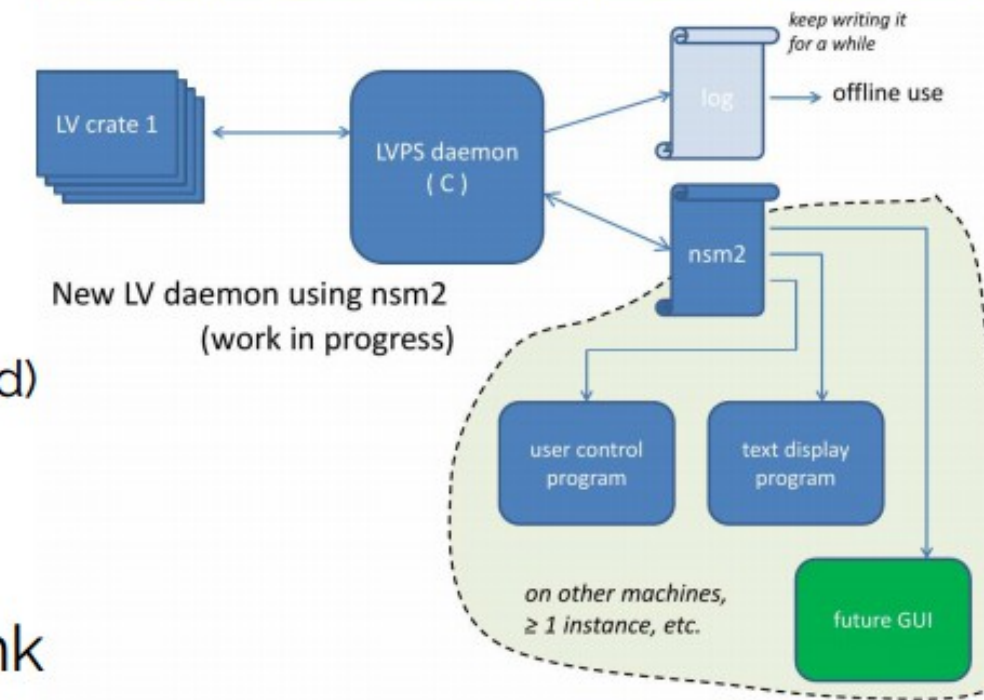
- hardware interlock:
 - magnet quench
 - chiller failure
 - water leak
- software interlock:
 - LVPS
 - I over/under/trip
 - V over/under
 - HVPS
 - I trip
 - V over/under
 - temperature
 - humidity
 - PMT hit rate



- LVPS, HVPS, interlock are in operation
- HV control is based on ARICH system developed by Konno + Yonenaga (no GUI yet but to be straightforward)
- LV control is in operation (GUI should be similar to HVPS)
- Info collected from Belle2link is needed
- Same water leak sensor to be used in the other place of the detector

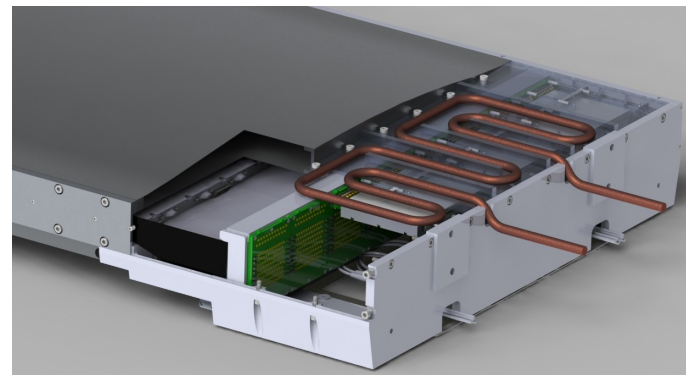


HW crate	TOP slot	PMT ID	Switch	Vdemand[V]	Vlimit[V]	Climit[mA]	Sample[Hz]	Rampdown[V]	State	Vmeas[V]	Clamp[mA]
01-01-00	01-01	01-01K79300	OFF	2144	3200	150	50	300	UNLOCKED	0.0	0.0
01-01-01	01-02	01-01K79300	OFF	2135	3200	150	50	300	UNLOCKED	0.0	0.0
01-01-02	01-03	01-01K79300	OFF	2232	3200	150	50	300	UNLOCKED	0.0	0.0
01-01-03	01-04	01-01K79300	OFF	2288	3200	150	50	300	UNLOCKED	0.0	0.1
01-01-04	01-05	01-01K79300	OFF	2135	3200	150	50	300	UNLOCKED	0.0	0.0



interlock

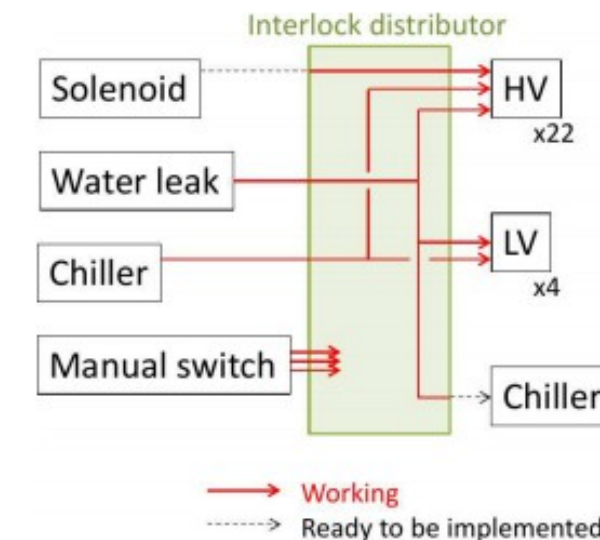
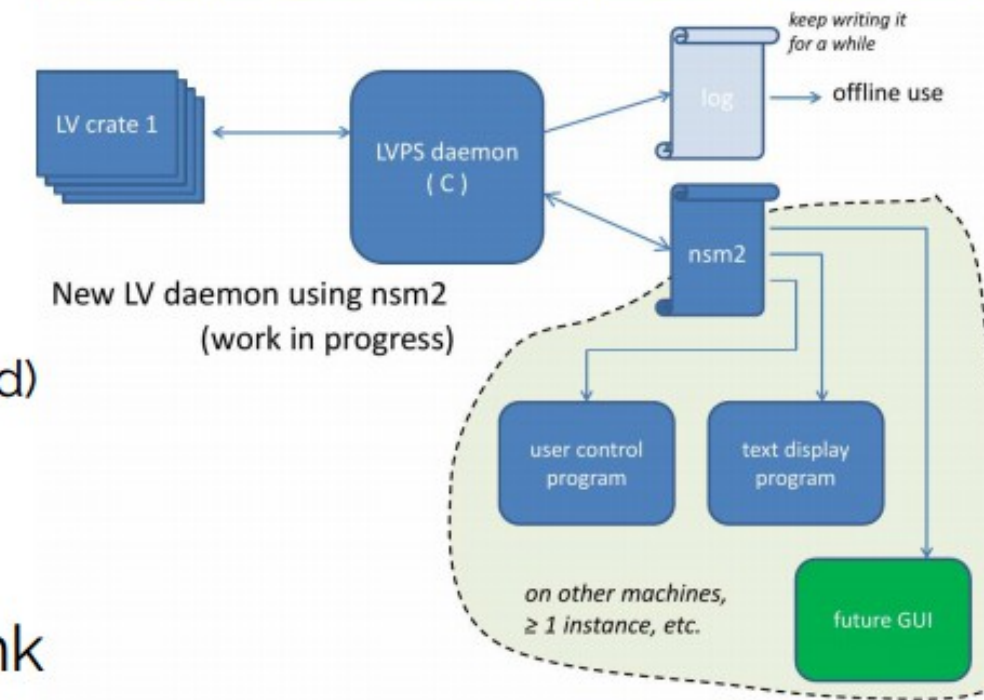
- hardware interlock:
 - magnet quench
 - chiller failure
 - water leak
- software interlock:
 - LVPS
 - I over/under/trip
 - V over/under
 - HVPS
 - I trip
 - V over/under
 - temperature
 - humidity
 - PMT hit rate



- LVPS, HVPS, interlock are in operation
- HV control is based on ARICH system developed by Konno + Yonenaga (no GUI yet but to be straightforward)
- LV control is in operation (GUI should be similar to HVPS)
- Info collected from Belle2link is needed
- Same water leak sensor to be used in the other place of the detector



HW crate	TOP slot	PMT ID	Switch	Vdemand[V]	Vlimit[V]	Climit[mA]	RampUp[V]	RampDown[V]	State	Vmeas[V]	Clamp[mA]
01-01-00	01-01	01-01K79300	OFF	2144	3200	150	50	300	UNLOCKED	0.0	0.0
01-01-01	01-02	01-01K79300	OFF	2135	3200	150	50	300	UNLOCKED	0.0	0.0
01-01-02	01-03	01-01K79300	OFF	2232	3200	150	50	300	UNLOCKED	0.0	0.0
01-01-03	01-04	01-01K79300	OFF	2200	3200	150	50	300	UNLOCKED	0.0	0.1
01-01-04	01-05	01-01K79300	OFF	2135	3200	150	50	300	UNLOCKED	0.0	0.0

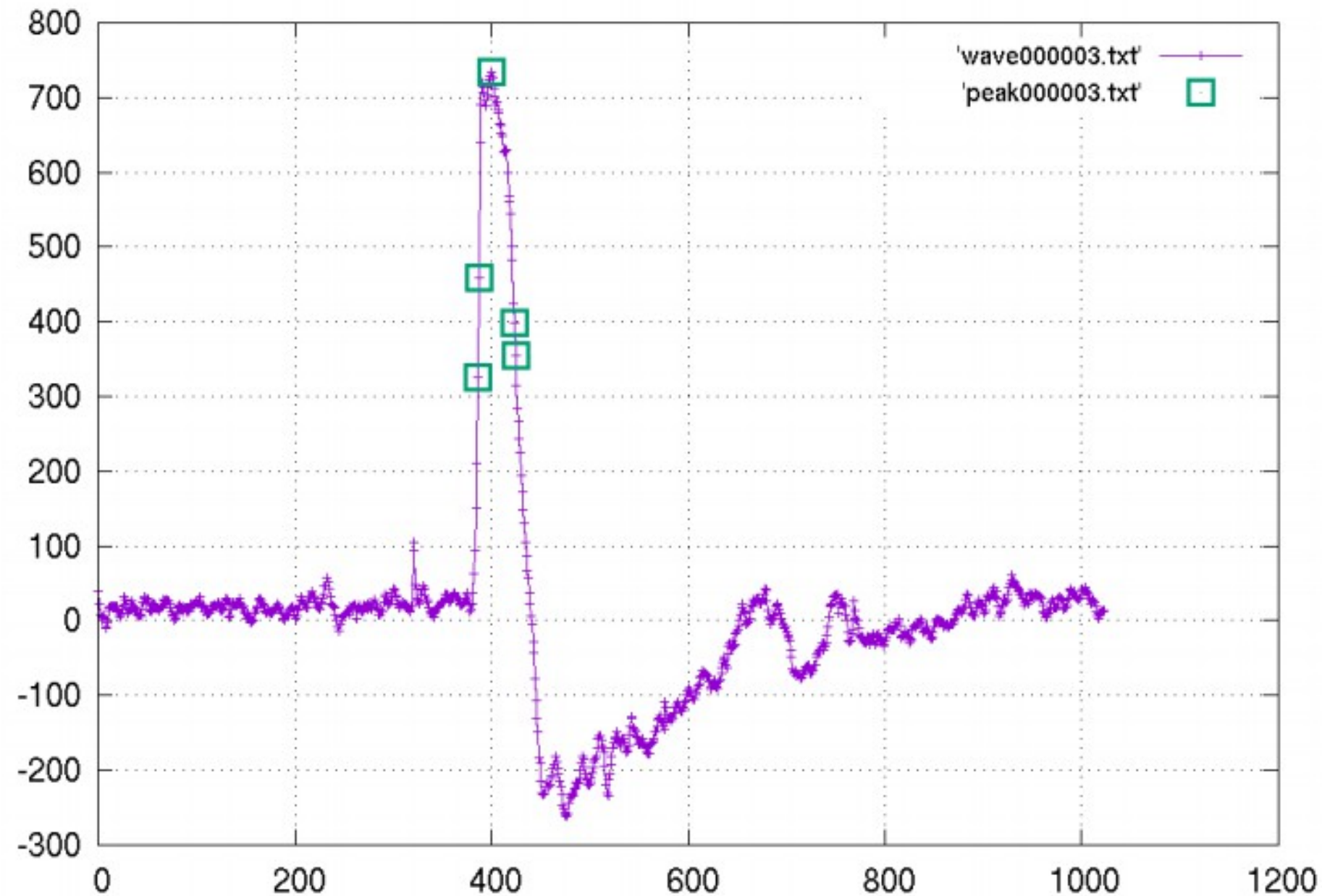


Hawaii PocketDaq (HPD)

- currently has 4 COPPERs (3 COPPER-II + 1 COPPER-III)
 - two COPPER-II and one COPPER-III work
 - 4th board is missing tt-rx
- created documentation on use on confluence page for HPD:
 - <https://confluence.desy.de/pages/viewpage.action?pageId=42342328>

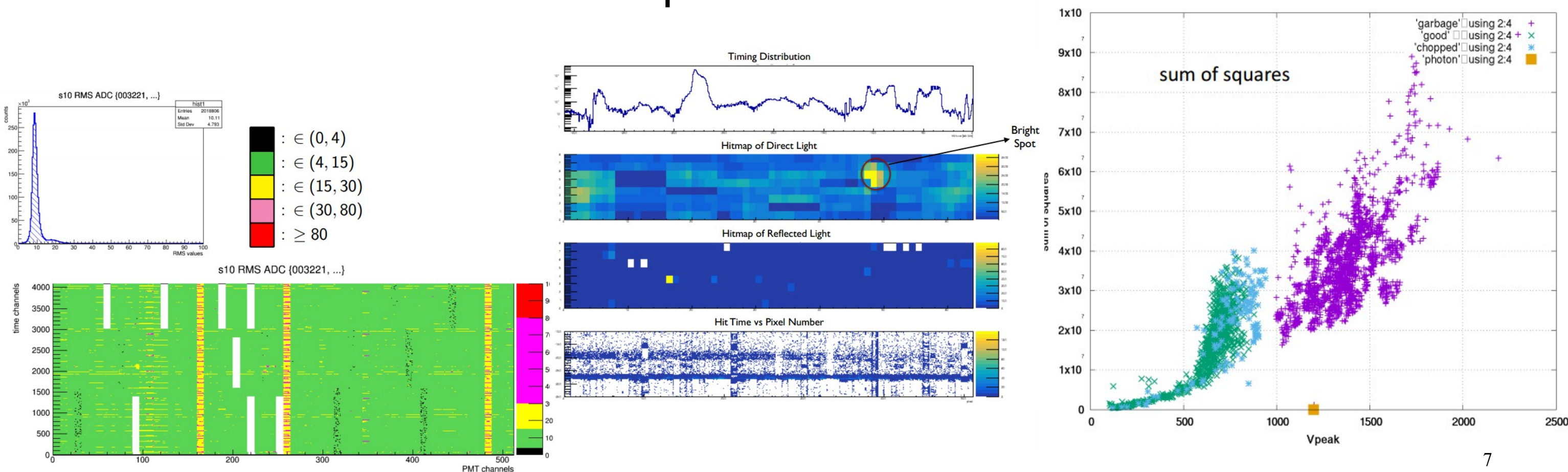
online feature extraction (FE)

- pedestal subtraction
- peak detection
- both implemented in "c"



DQM

- official version maintained by M. Staric and others:
 - needs the firmware/readout software to be in a more final state before it will be meaningful
- several alternate versions in place in the meantime:



local runs

- ASIC health monitoring, pedestal (re-)acquisition
- other boardstack ADC (I,V) / temp / hum monitoring
- laser data acquisition
- calibration pulse data acquisition

belle2link (b2l)

- b2l timeout (a16d32ff):
 - all causes not known for certain
 - anecdotal evidence of several things being the cause
- deadbeef (related to timeout error):
 - simultaneous copper local bus access while streaming data from copper fifo
 - at least we're pretty sure that's what the (only) cause is
- need test for each that is simple, yet repeatable:
 - for troubleshooting these sorts of problems,
 - "run testbench/deadbeef.py to see if the error is present in this firmware"
 - is a million times better than a report along the lines of:
 - "doing x and y together sometimes causes deadbeef"

b2tt

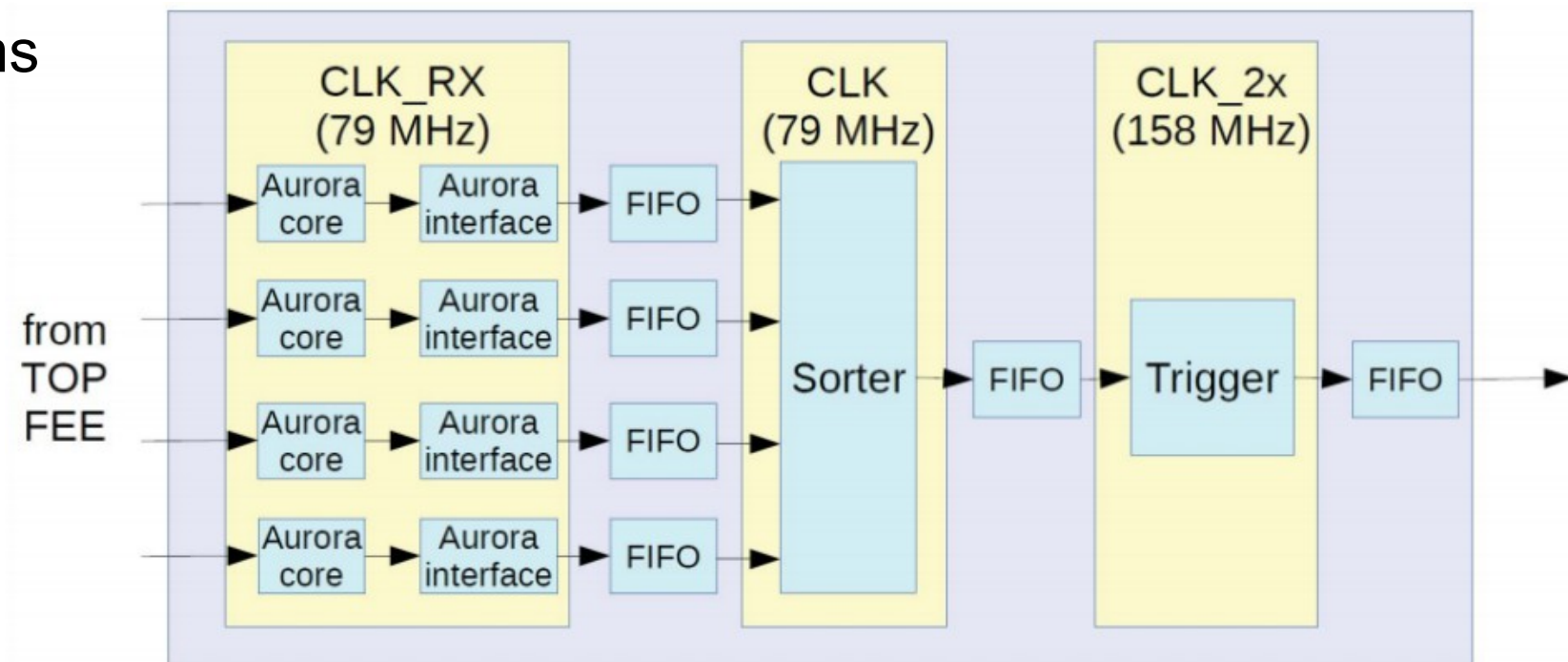
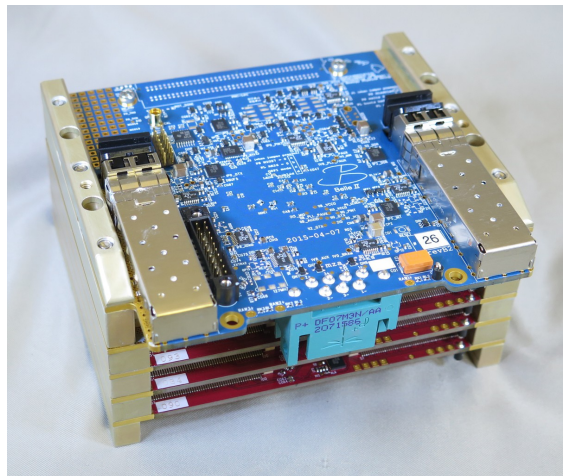
- initial event # = -1
 - hopefully solved by migration to 0.48 (from 0.45) [pending confirmation]
- sent a report on vivado compilation strangeness with 0.48 related to USE254IN generic in email to Nakao-san:
 - 'b2tt 0.48 "strange error" for TOP/scrod firmware' on 2016-09-06

data acquisition (DAQ)

- Yamada-san's question from yesterday about our event/hit size:
 - I don't know; asked M. Barrett, M. Staric and L. Wood for clarification
 - Staric: occupancy has increased due to new background estimates
 - our latest spreadsheet on data formats is posted on confluence
 - sheet "production data" which shows event size is $\sim 3.285\text{k bytes/event} = 4 \cdot (4 \cdot \# \text{hits} + 2)$
 - <https://confluence.desy.de/display/BI/TOP+Module01Firmware> file [data_format_v2_0.xlsx](#): Data Format v2.0
 - but this includes slow control info, so archived size can be less...
 - Nakao: slow control info will have to be removed from data stream, so size *will* be less; Wood: current format includes extra FE info, so size *will* be less
- example python COPPER/HSLB/slow control code:
 - our code is in python2, but calls reghsx to do the local bus reads/writes
 - example code mentioned at B2GM24 (cdcfee.py and b2daq.py, etc) use python3, so there's a (small) bit of effort required there to port things
 - but probably worth doing in the short term...

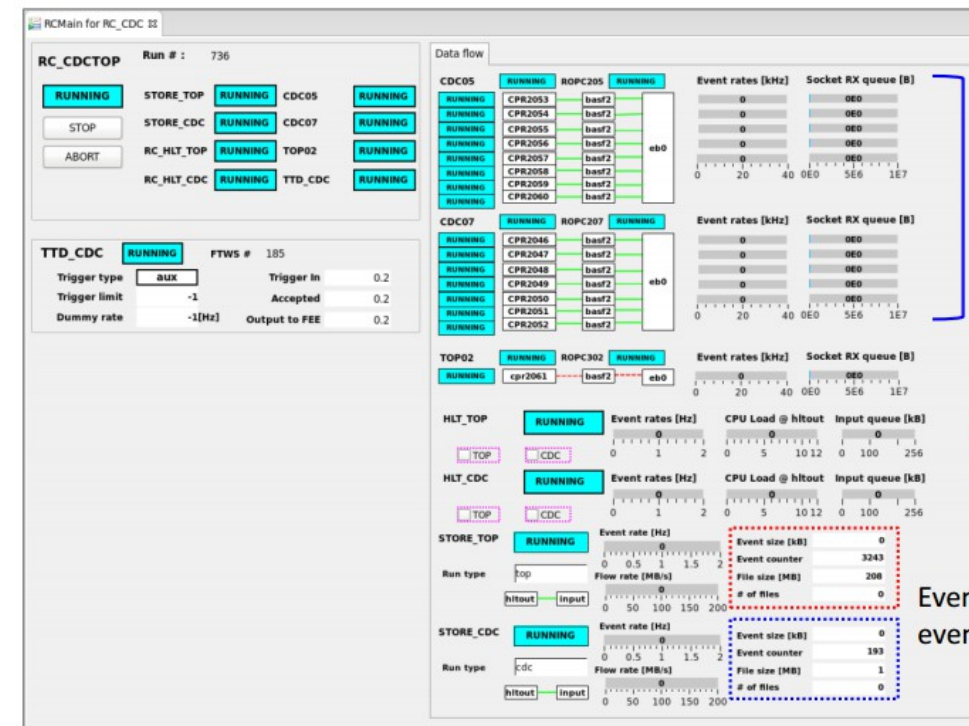
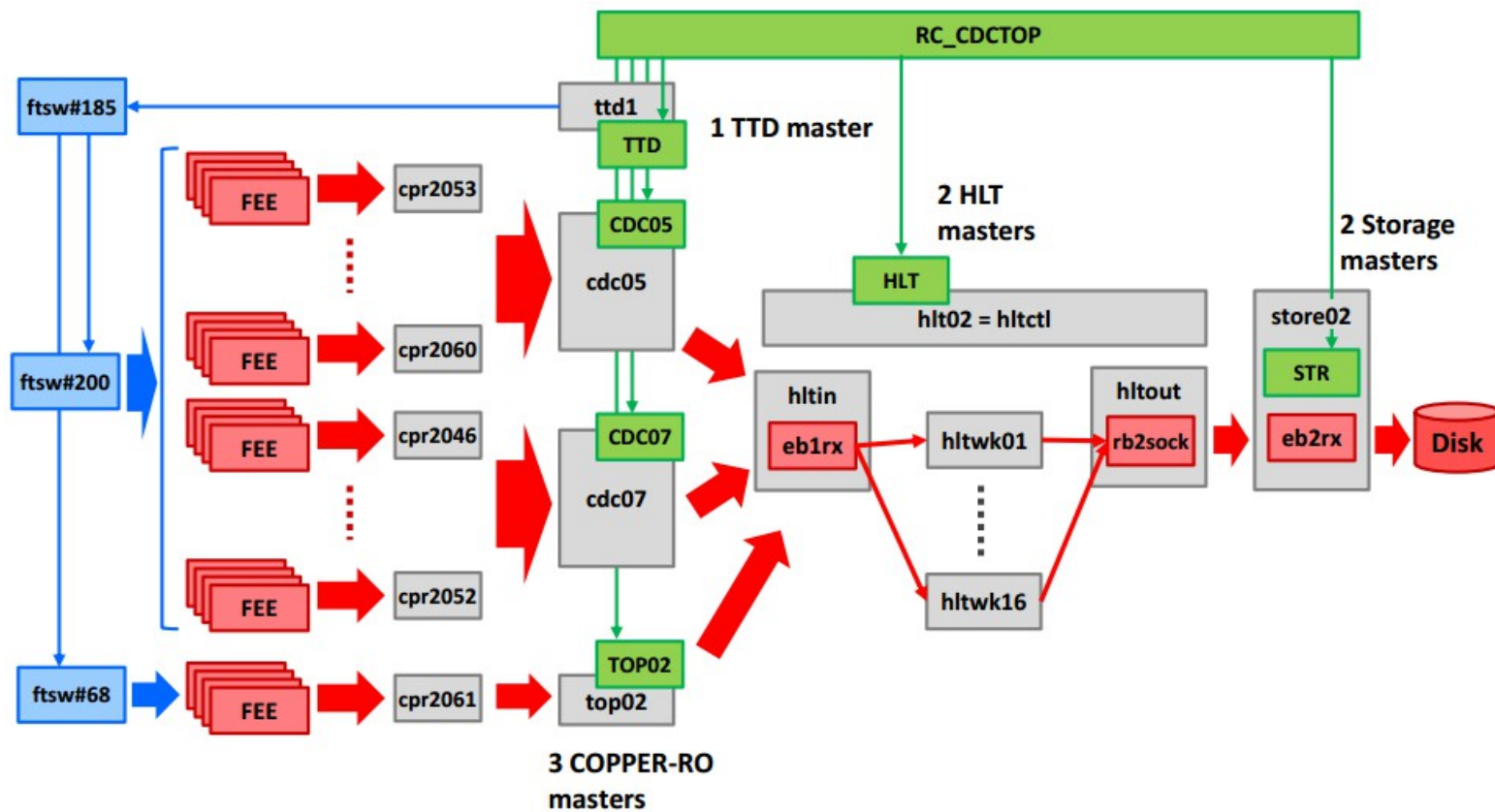
trigger -> GDL

- UT3 component:
 - being worked on by Nisar @ Pitt (formerly by Istvan @ Pitt, Xin/Luca @ Hawaii)
 - see N. Nellikunnummel's talk (yesterday) for more details...
- FEE component:
 - nobody has had time to implement the FEE part yet
 - "TRIG" fiber links were tested with an IBERT loopback (to the "DATA" link)
 - so we don't expect any (hardware) problems



CDC+TOP

- need to sort out bugs with RoI firmware + FE software (ongoing)



COPPER-ROPC for CDC

COPPER-ROPC for TOP

HLT for TOP

HLT for CDC

Event counts differ since TOP event is divided into 16 pieces

should be fixed in FE version 13

database

- configuration/logger databases:
 - I'd like to try putting our ASIC register settings into the database (currently they are in text files in our svn repo, one file per boardstack, e.g. "sstoutFB/SCROD98.fb" and "thresholds/SCROD98.dat")
Konno: send .fb and .dat to Konno-san so he can make example code for us
 - and I'd like to try storing our scalers for ASIC feedback monitoring in the database, too
 - can someone point me to some example code for the REST/apache interface?
 - perhaps https://confluence.desy.de/display/BI/DAQ+SC_DB with some modification?
Konno: database: no need for REST/apache in principle

E-hut

- currently:
 - top01 used for DAQ on slots01-08
 - top03 used for DAQ on slots09-16
 - top02 used for DAQ on "module01" (CDC+TOP test)
 - toptest01 used for programming boardstacks, controlling LVPS(/HVPS?), etc
- would be nice if the filesystem were common (ldap+nfs)
 - Yamada: doubling up on nfs mounts (bdaq to ROPC; then ROPC to COPPER) is not planned at this time
 - at least common between top01 and top03 would help
 - homes mounted from bdaq would be ideal
 - Nakao: bdaq home is exported but not mounted (update: now mounted)
 - is this possible for "b2top" user as well, or is that prohibited?
- is there a plan to change the administration method on topNM (and other subdetectors' DAQ machines) during the SL5->SL6 upgrade?

15

JTAG programming

- reminder: need regular bit file programming, plus various xmd commands to program elf + start ARM/PS on Zynq
 - ~~what is the current status of the Zynq effort by Y. Yook?~~ (answered by Nakao-san yesterday)
 - we in Hawaii would be happy to test whatever you have
- subdetector-wide programming from the official FTSW tree:
 - are we using xilinx/digilent programmers for this in final Belle II?
 - [if not] what is the current schedule for developing this b2svf-player?
 - again, we're happy to help test

Nakao: jtag/zynq situation will remain until end of year at least

FTSW trigger types

- need some way to synchronize reset of clock divider on 4 boardstacks simultaneously:
 - these clock dividers are on carrier boards, and the intra-boardstack synchronization is already handled by the reset signal being asserted by SCROD
 - first choice is to use one of the special types of FTSW trigger (currently 4 types called out in b2tt_symbols.vhd for PID), since it further could allow alignment with the beam orbit* which we may want eventually
 - alternative is to let them be randomly reset, and then let backend software issue resets on (up to) 3 boardstacks until synchronization is achieved (would require a signal + digitization + signal analysis which is *not* preferred)
 - * = b2tt.pdf document says revo may be out of phase with beam orbit - still true? [if true, are they at least synchronized across all bPID FTSWs?]

Nakao-san: divided clock in b2tt a possibility to do the divider reset; facility already exists

Nakao-san: signal is same across entire detector, offset provided as digital number

backup

E-hut

- [need to find updated diagram]

