# Realtime Independent Three-bit Converter (RITC): Description and Interface

The realtime independent three-bit converter (RITC) is an application specific integrated circuit that digitizes RF input signals with 3-bit resolution at gigasample per second rates. RITC was submitted as part of May 9, 2011 MOSIS multi-project wafer run in the 130 nm IBM 8RF-DM process. The ASIC operates in a streaming mode, such that all input signals are digitized and streamed off the chip. This document describes the basic functionality, pinouts, and interface requirements for RITC.

## I. DESCRIPTION

The real-time independent three-bit converter (RITC) a 3-bit, three channel flash analog-to-digital converter (ADC) capable of operation at up to 3 GSa/s. Each channel consists of an array of 32 sampling and digitizing cells, each utilizing a sample-and-hold stage and a three-bit flash ADC. Digital outputs from all cells are multiplexed to allow a streaming readout at 1/4 the sampling rate, $f_s$. These outputs are sent off-chip through 36 LVDS pairs (12 per channel). The timing signals necessary to perform the sampling, digitizing and multiplexing are derived from an on-chip timing generator. This timing generator requires a single clock input of frequency $f_s/32$. A reference pseudo-clock is available as an LVDS pair, which can be used to monitor the sampling rate and as a phase reference for the multiplexed data signals.

Two test structures are also available. One is a standalone version of the comparator used in the sampling cells to allow linearity scanning and verification of performance.

On-chip 12-bit digital-to-analog converters (DACs) allow independent control over the seven comparator thresholds for each channel (21 DACs), the internal sampling rate (2 DACs), and biases for the prototype charge-sensitive amplifier (10 DACs). The interface to the DACs is by serial shift register, the interface to which uses a single data line, a clock, and a latch. A data ouput line is available to monitor bits shifted out.

RITC requires analog and digital 1.2 V, as well as digital 2.5 V. Digital and analog grounds on the PCB should also be independent, connected only with a low-pass filter.

A block diagram of the general architecture is shown in Figure 1. The schematic of this interface is shown in Figure 2. The final pinout is shown in Figure 3. The die is wire-bonded into an LQFP128A package.

## II. RF INPUTS

All RF inputs to RITC are differential. The internal sample-and-hold cells and the comparators continue this differential structure, which is intended to reduce common-mode noise on the inputs. Signals should range between 0 and 1.2 V, preferrably near the middle of this range. Thus, the negative terminals can be connected to a "pedestal" voltage at the board level of roughly 600 mV. RF signals are **not** terminated on-chip, so 50 Ω termination should be done on the board near the input to the chip. A list of RF input pins with brief descriptions is shown in Table I.

The analog bandwidth of the RF inputs has been simulated in Cadence both pre- and post-layout, and is shown in Figure 4. Please note that these simulations assume a perfect 50 Ω termination off-chip, and 5 nH inductance for each bond wire connecting the bond-pad to the package pin. Any further losses from the input coupling on the board or due to the board design itself are **not** included.

| Pin Number | Pin Name | Description |
|---|---|---|
| 3 | CMP_IN_P | + analog input to test comparator |
| 4 | CMP_IN_M | − analog input to test comparator |
| 6 | RF_IN_CH0_P | + analog input to channel 0 |
| 7 | RF_IN_CH0_M | − analog input to channel 0 |
| 10 | RF_IN_CH1_P | + analog input to channel 1 |
| 11 | RF_IN_CH1_M | − analog input to channel 1 |
| 14 | RF_IN_CH2_P | + analog input to channel 2 |
| 15 | RF_IN_CH2_M | − analog input to channel 2 |

TABLE I: RITC RF input pins.

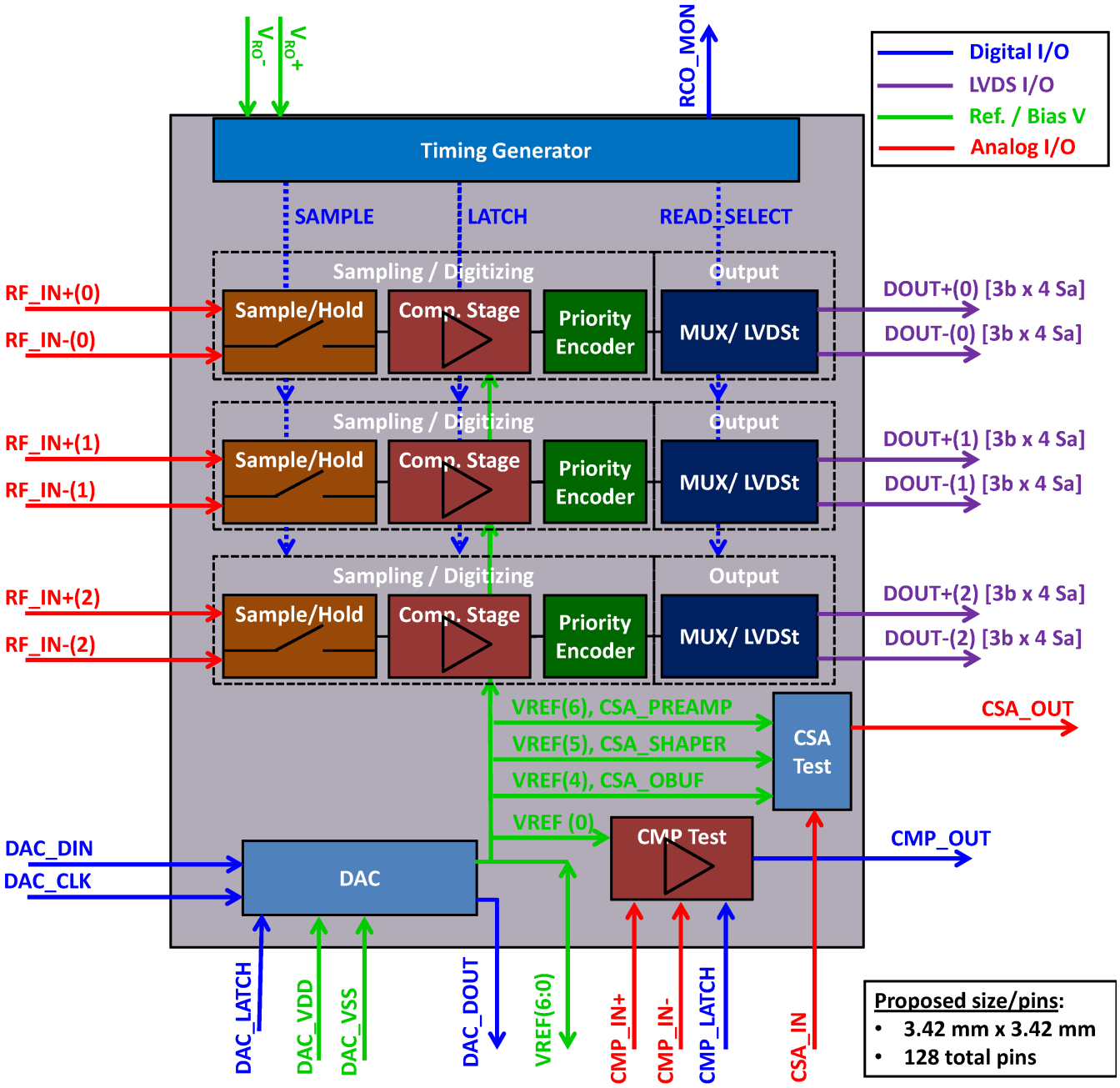


FIG. 1: A logical block diagram of the underlying elements of RITC.

## III. DAC INTERFACE

The interface to the DACs is handled by a single serial shift register. Each DAC has 12 input bits and provides a voltage between 0 and 1.2 V. Since there are a total of 33 DACs, this corresponds to 396 input bits. Input bits from DAC_DIN are clocked into the DAC shift register on a rising edge of DAC_CLK. Bits are not transferred to the DACs themselves until a rising edge of DAC_LATCH. Data being shifted out of the DAC shift register can be monitored on the DAC_DOUT pin. A description of pins for the DAC interface is given in Table II. The sequence of DACs and bits is given in Table III.

Analog output voltages for the DACs controlling voltage thresholds in channel 2, as well as the sampling rate NFET and PFET control voltages, are available on output pins. These pins can be used to monitor and verify DAC

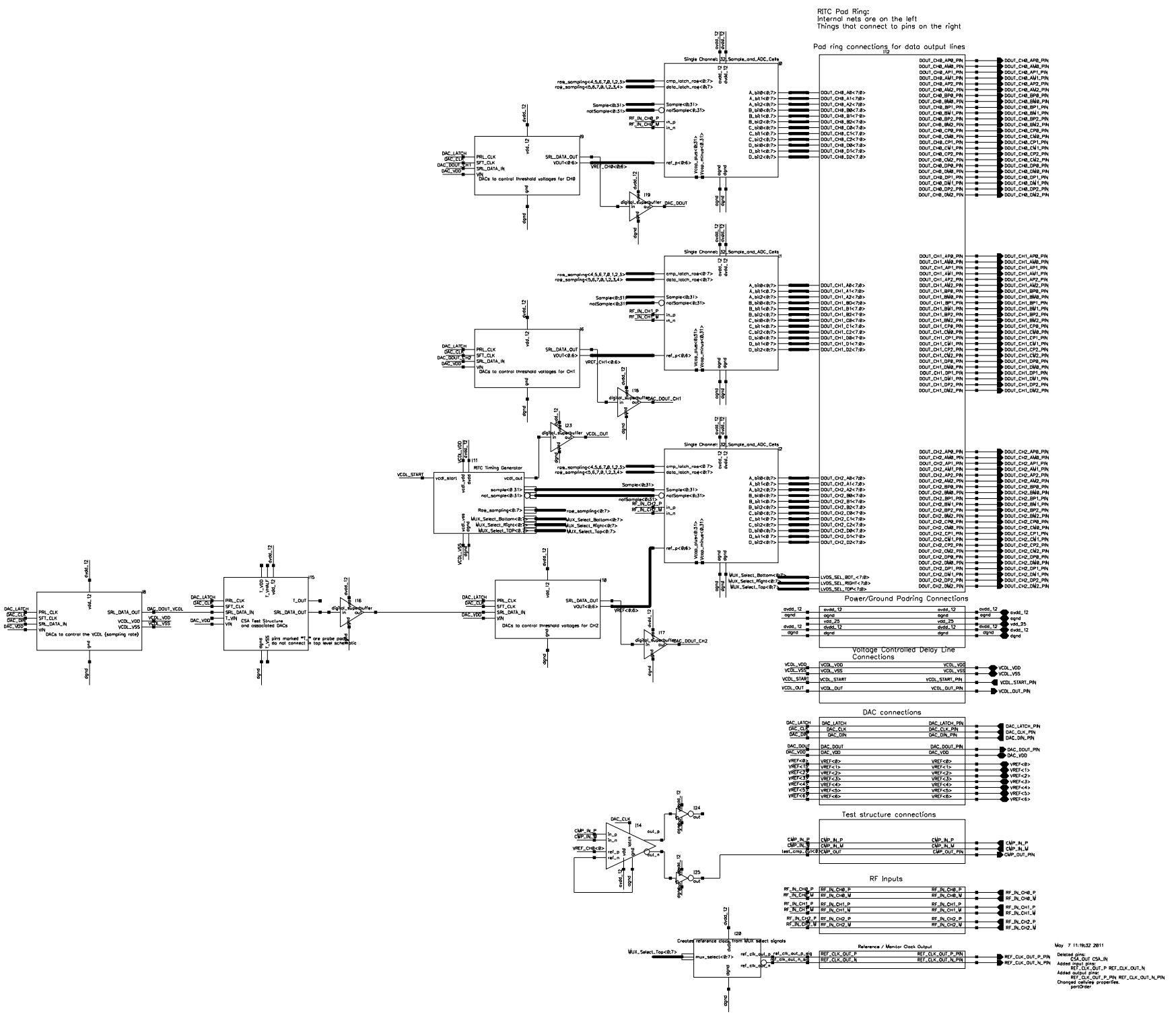


FIG. 2: The top level schematic of RITC.

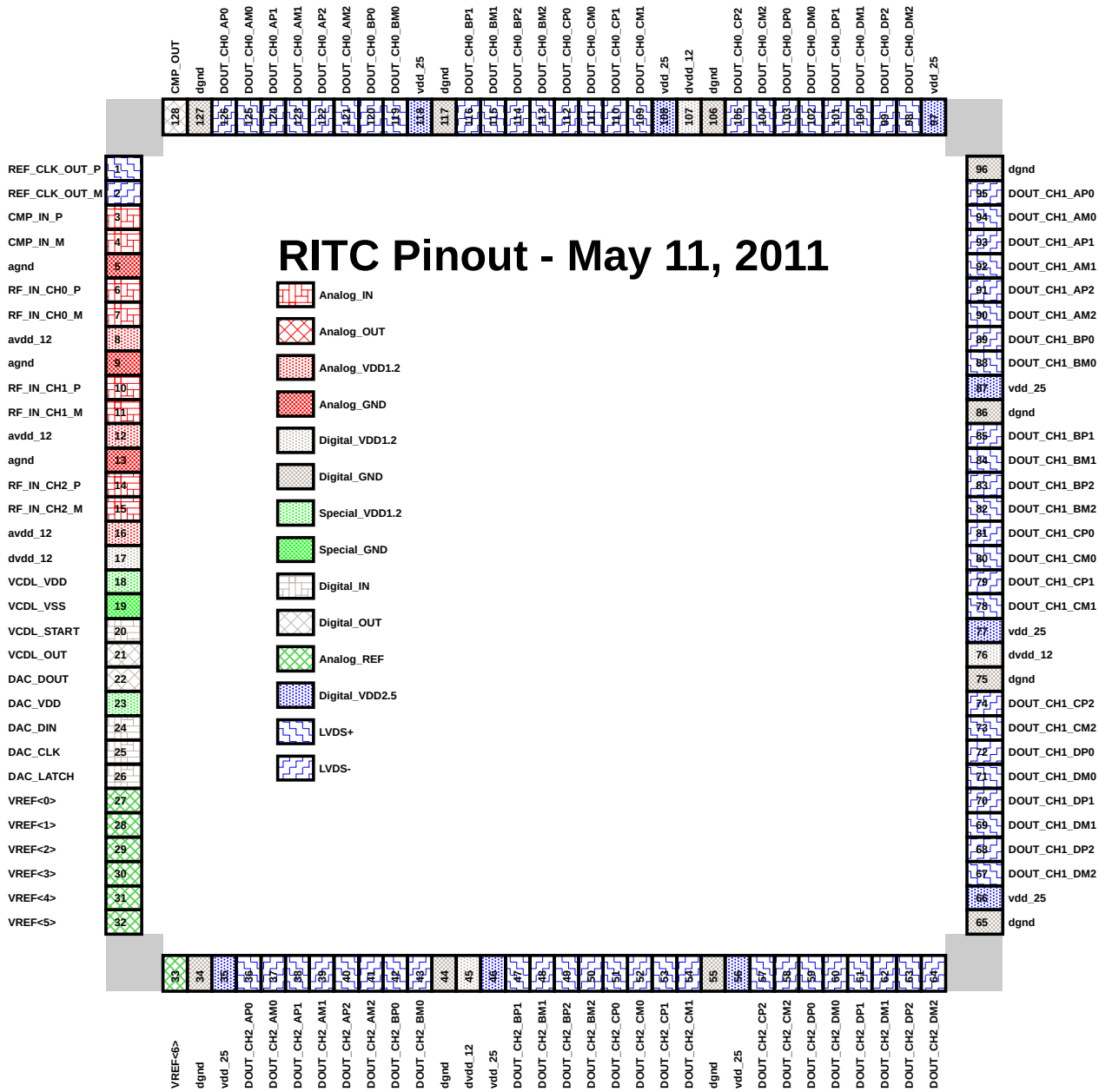


FIG. 3: The pinout of RITC, as fabricated.

performance, or, in the event of DAC failure, can be driven externally to allow limited functionality.

## IV. SAMPLING, DIGITIZING, AND READOUT

An internal timing generator is used to generate most of the signals that control the sampling, digitizing, and output digital multiplexing within RITC. The user must supply a single-ended, 1.2 V clock on the VCDL_START pin. This signal travels down a delay line and ultimately emerges on the VCDL_OUT pin, again as a single-ended digital 1.2 V signal. This start signal should be sent at a frequency $f_s/32$. Control over the speed of propagation of this signal down the delay line, and thus the ADC sampling and digitizing rates, are handled by the analog control

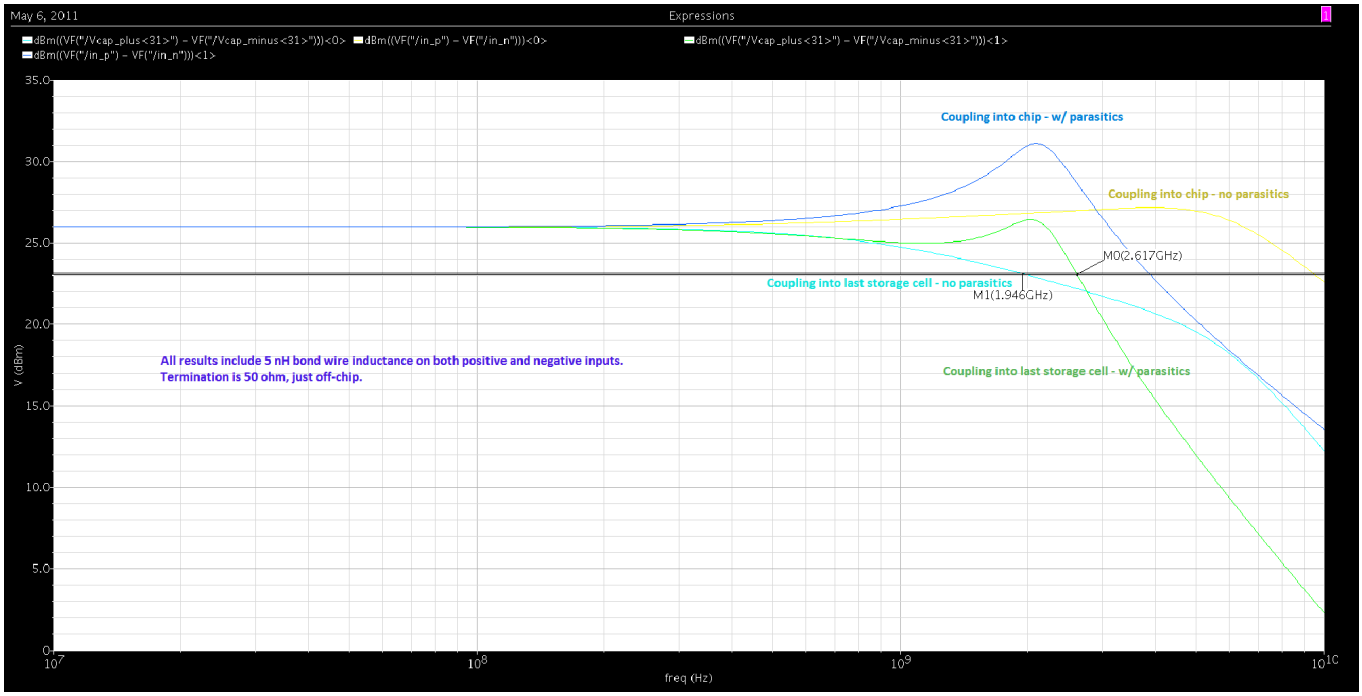


FIG. 4: Simulated analog-bandwidth for the RITC sampling arrays. These bandwidths are taken at the last cell of the array. Bandwidth from cell to cell may vary slightly.

| Pin Number | Pin Name | Description |
|---|---|---|
| 25 | DAC_CLK | 1.2 V digital input - clock to shift data into DAC shift register chain[a] |
| 24 | DAC_DIN | 1.2 V digital input - input bit to DAC shift register chain |
| 22 | DAC_DOUT | 1.2 V digital output - output bit of DAC shift register chain |
| 26 | DAC_LATCH | 1.2 V digital input - latches DAC shift register values to DACs |
| 18 | VCDL_VDD | analog DAC output (sampling rate NFET control voltage) / analog input |
| 19 | VCDL_VSS | analog DAC output (sampling rate PFET control voltage) / analog input |
| 27 | CH2_VREF0 | analog DAC output (lowest threshold for CH2) / analog input[b] |
| 28 | CH2_VREF1 | analog DAC output (second threshold for CH2) / analog input |
| 29 | CH2_VREF2 | analog DAC output (third threshold for CH2) / analog input |
| 30 | CH2_VREF3 | analog DAC output (fourth threshold for CH2) / analog input |
| 31 | CH2_VREF4 | analog DAC output (fifth threshold for CH2) / analog input |
| 32 | CH2_VREF5 | analog DAC output (sixth threshold for CH2) / analog input |
| 33 | CH2_VREF6 | analog DAC output (highest threshold for CH2) / analog input |

[a]This signal also serves as the latch for the test comparator
[b]This voltage is also used as the reference voltage for the test comparator.

TABLE II: RITC DAC I/O pins.

voltages VCDL_VDD and VCDL_VSS (see previous section on DAC controls). These voltages must work in concert with the VCDL_START signal so there are no gaps in sampling or any oversampling.

Monitoring the sampling and digitization rate can be accomplished by two mechanisms. First, the delay of VCDL_OUT relative to VCDL_START is directly indicative of the time it takes for 32 samples to be captured and digitized. However, insertion and extraction delay complicate this calculation, and without further calibration this line may be most useful as a qualitative check that the biases on the delay line allow propagation of the sampling signal. The second mechanism to monitor the sampling rate is from the LVDS pair REF_CLK_OUT_P and REF_CLK_OUT_M. This signal is a reference "clock" that is generated from the internal signals used to multiplex the output data, as shown in Figure 5. It toggles at 1/2 the rate of the digital output lines, which corresponds to $f_s/8$. Please note that this signal is not a true clock, as it will toggle only upon receiving a VCDL_START signal. When VCDL_START is being sent regularly, VCDL_VDD and VCDL_VSS should be adjusted to obtain the proper $f_s$.

Digitized output data is read out in parallel, with all bits of four samples from each channel read out simultaneously. Each cell is designated by a letter: A (earliest cell), B, C, or D (latest cell), and each bit from those cells is identified

| Word number | Description |
|---|---|
| 0 | CH 0, reference voltage 6 |
| 1 | CH 0, reference voltage 5 |
| 2 | CH 0, reference voltage 4 |
| 3 | CH 0, reference voltage 3 |
| 4 | CH 0, reference voltage 2 |
| 5 | CH 0, reference voltage 1 |
| 6 | CH 0, reference voltage 0 |
| 7 | CH 1, reference voltage 6 |
| 8 | CH 1, reference voltage 5 |
| 9 | CH 1, reference voltage 4 |
| 10 | CH 1, reference voltage 3 |
| 11 | CH 1, reference voltage 2 |
| 12 | CH 1, reference voltage 1 |
| 13 | CH 1, reference voltage 0 |
| 14 | CH 2, reference voltage 6 |
| 15 | CH 2, reference voltage 5 |
| 16 | CH 2, reference voltage 4 |
| 17 | CH 2, reference voltage 3 |
| 18 | CH 2, reference voltage 2 |
| 19 | CH 2, reference voltage 1 |
| 20 | CH 2, reference voltage 0 |
| 21 | Charge sensitive amplifier bias X |
| 22 | Charge sensitive amplifier bias X |
| 23 | Charge sensitive amplifier bias X |
| 24 | Charge sensitive amplifier bias X |
| 25 | Charge sensitive amplifier bias X |
| 26 | Charge sensitive amplifier bias X |
| 27 | Charge sensitive amplifier bias X |
| 28 | Charge sensitive amplifier bias X |
| 29 | Charge sensitive amplifier bias X |
| 30 | Charge sensitive amplifier bias X |
| 31 | Sampling speed PFET control voltage |
| 32 | Sampling speed NFET control voltage |

TABLE III: Order of programming for the 33 12-bit DAC words. Lower numbers are programmed first. For each DAC, the first bit in corresponds to the most significant bit.

by a number, with 0 being the least significant bit and 2 being the most significant bit. A summary of these signals and their pin numbers is shown in Table IV.

## V. BOARD LAYOUT SUGGESTIONS

- As the timing of the data lines is crucial to reading in the data stream correctly, it is recommended that the trace lengths for all LVDS pairs are approximately the same.
- To minimize leakage of digital noise into the analog signals, the digital power and ground should be separated from the analog power and ground. The ground for digital 2.5 V and 1.2 V is shared on-chip, so this can be shared on the board as well.
- RF inputs require 50 Ω termination, preferrably as close to the ASIC inputs as possible.
- Negative analog RF inputs should be tied to a "pedestal" voltage, which is recommended to be approximately mid-range (0.6 V). Linearity is expected to be slightly better in the upper part of the range, so this can be adjusted as necessary.
- The analog output voltages from the on-chip DACs should be wired to test points for monitoring, and one or more could also be connected to an ADC for automated scans of DAC performance.
- In the event of on-chip DAC failure, drive the on-chip DAC voltages with external voltage sources or DACs.

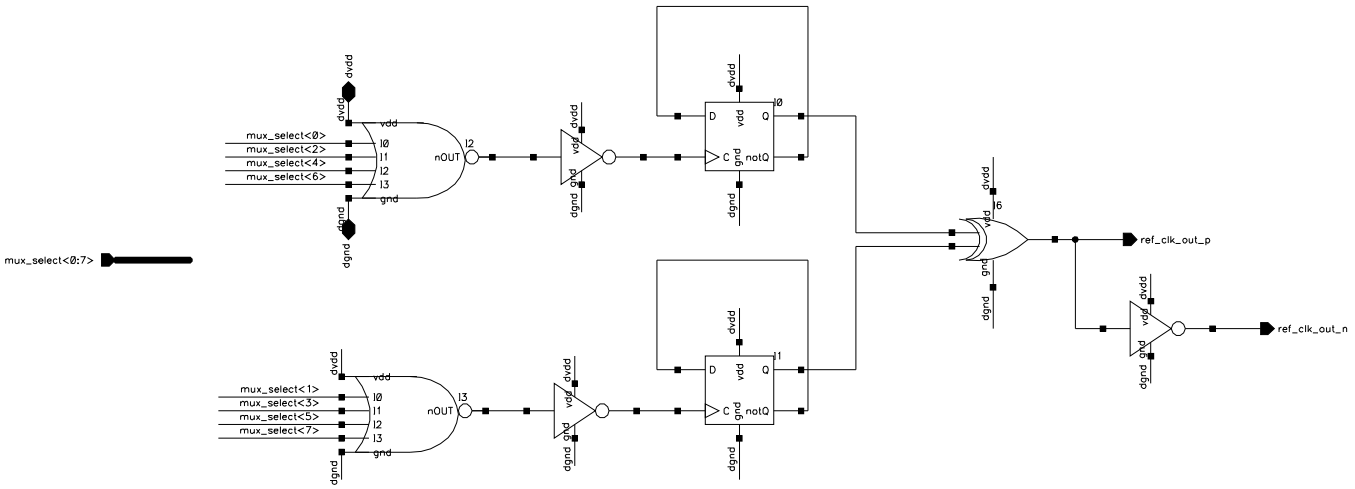


FIG. 5: Schematic for the reference clock generator.

| Pin Number | Pin Name | Description |
|---|---|---|
| 20 | VCDL_START | 1.2 V digital input - initiates ADC sequence, clock this at $f_s/32$ |
| 21 | VCDL_OUT | 1.2 V digital output - copy of VCDL_START after traversing delay line |
| 1 | REF_CLK_OUT_P | + LVDS output - reference clock |
| 2 | REF_CLK_OUT_M | − LVDS output - reference clock |
| 121-126 | DOUT_CH0_A(P,M)[0,1,2] | (+,−) LVDS outputs - CH0 digital data, cell A, bits [0,1,2] |
| 113-116,119-120 | DOUT_CH0_B(P,M)[0,1,2] | (+,−) LVDS outputs - CH0 digital data, cell B, bits [0,1,2] |
| 104-105,109-112 | DOUT_CH0_C(P,M)[0,1,2] | (+,−) LVDS outputs - CH0 digital data, cell C, bits [0,1,2] |
| 98-103 | DOUT_CH0_D(P,M)[0,1,2] | (+,−) LVDS outputs - CH0 digital data, cell D, bits [0,1,2] |
| 90-95 | DOUT_CH1_A(P,M)[0,1,2] | (+,−) LVDS outputs - CH1 digital data, cell A, bits [0,1,2] |
| 82-85,88-89 | DOUT_CH1_B(P,M)[0,1,2] | (+,−) LVDS outputs - CH1 digital data, cell B, bits [0,1,2] |
| 73-74,78-81 | DOUT_CH1_C(P,M)[0,1,2] | (+,−) LVDS outputs - CH1 digital data, cell C, bits [0,1,2] |
| 67-72 | DOUT_CH1_D(P,M)[0,1,2] | (+,−) LVDS outputs - CH1 digital data, cell D, bits [0,1,2] |
| 36-41 | DOUT_CH2_A(P,M)[0,1,2] | (+,−) LVDS outputs - CH2 digital data, cell A, bits [0,1,2] |
| 42-43,47-50 | DOUT_CH2_B(P,M)[0,1,2] | (+,−) LVDS outputs - CH2 digital data, cell B, bits [0,1,2] |
| 51-54,57-58 | DOUT_CH2_C(P,M)[0,1,2] | (+,−) LVDS outputs - CH2 digital data, cell C, bits [0,1,2] |
| 59-64 | DOUT_CH2_D(P,M)[0,1,2] | (+,−) LVDS outputs - CH2 digital data, cell D, bits [0,1,2] |
| 128 | CMP_OUT | 1.2 V digital output - test comparator output bit |

TABLE IV: Pins related to ADC timing and readout.

- External DACs may also be desirable in order to automate comparator performance scans. A total of 11 DAC channels would allow control over all failsafe bias voltages, if needed, as well as two channels to run comparator scans.
- It may be useful to see REF_CLK_OUT on an oscilloscope, so test pads (or at least accessible traces) are preferred.
- Same as above, but for one of the digital data output pairs.

## VI. SUGGESTED TESTING SEQUENCE

It is suggested that the performance of individual components be tested as much as possible before testing the full system. The following is a recommended sequence to test.

1. Test the DAC shift registers. Shift a pattern of 396 bits in, then shift all 396 bits out and check the output against the input.
2. Perform a scan of DAC voltages, verifying proper loading of DAC values and DAC performance.

3. Perform a measurement of comparator performance, using the dedicated test comparator. Set the comparator threshold to the desired value (by use of VREF_CH0 threshold 0). Set an analog value for the CMP_IN voltages, and assert the comparator latch (by use of the DAC_CLK pin). Check the status of the output bit CMP_OUT. Sweep the input voltages to find the point where CMP_OUT changes from a '0' to a '1'. Repeat for various values of threshold voltages.

4. Set VCDL_VDD and VCDL_VSS to provide power to the delay line. Send in a single pulse on VCDL_START. A set of pulses should appear on the REF_CLK_OUT lines (a single delayed pulse should also appear on VCDL_OUT). If one or both of these signals do not appear, adjust VCDL_VDD and VCDL_VSS until they do. VCDL_VDD can be set from 0-1.2 V, and VCDL_VSS should generally be set symmetrically (so VCDL_VSS = 1.2 V − VCDL_VDD).

5. Once a stable rate is found where REF_CLK_OUT reliably gives a set of pulses for an input VCDL_START, change VCDL_START to be a clock signal. The proper clock rate can be determined by measuring the frequency of the REF_CLK_OUT pulses. VCDL_START should be sent at 1/8 of the measured reference clock frequency. [1]

6. Monitor REF_CLK_OUT with VCDL_START clocked at the frequency found in the last step. Implement feedback in the control firmware to stabilize the sampling rate (i.e., keep REF_CLK_OUT stable).

7. With sampling ongoing continuously (from the last step), check any of the digital output pairs on an oscilloscope to verify the data rates and validity with an eye diagram (or similar). Check the delay between the data valid and the REF_CLK_OUT transitions.

8. Implement SERDES with delays estimated from the previous step... hopefully things are sort of working now? Try to read out some waveforms.

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[1] Avoid measuring the reference clock frequency on the last pulse of each train that accompanies a VCDL_START pulse. This final pulse corresponds to "wraparound" sampling, and will only give the proper frequency after all control voltages are propely tuned.