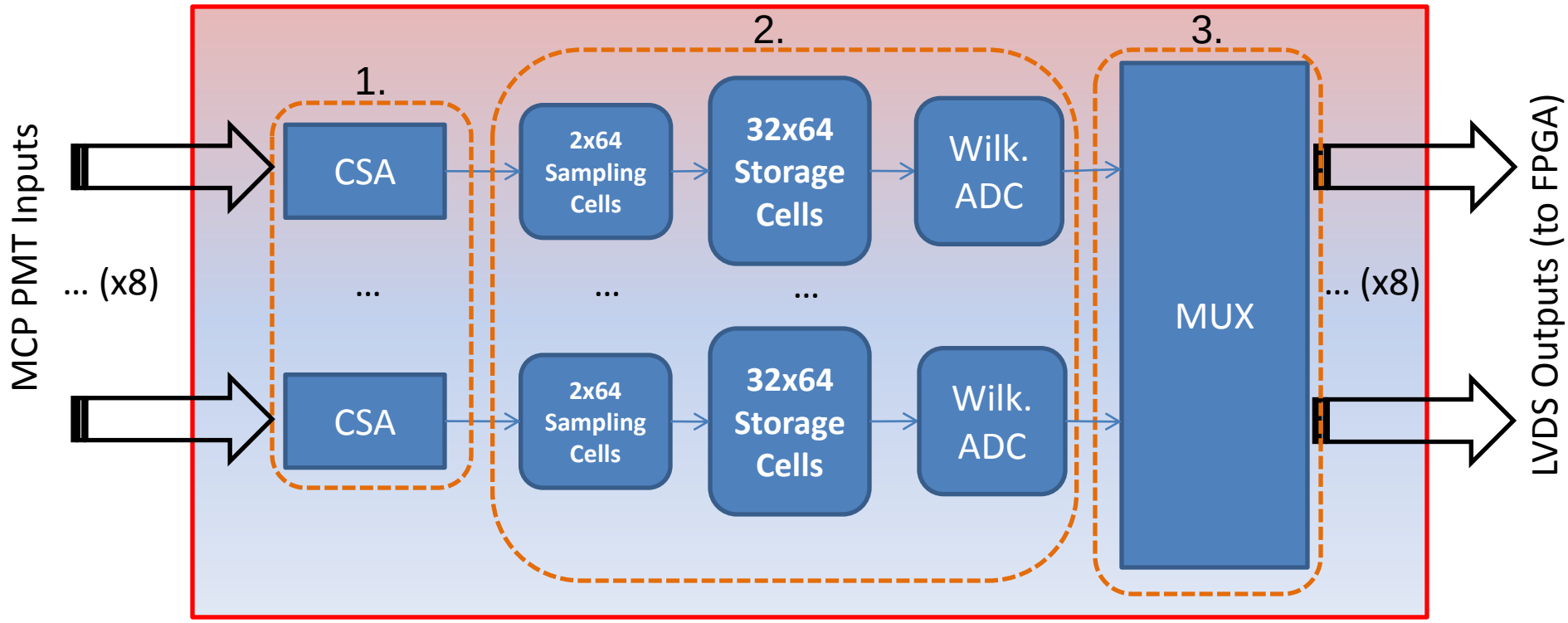
Gigasample Recorder of Analog waveforms from a Photodetector (GRAPH) ASIC



The full GRAPH block diagram is represented above, and has 3 primary challenges:

1. Charge sensitive amplifier (CSA) performance
2. Noise and dynamic range of the sampling/digitization
3. Fast throughput to the FPGA

Primary goal for this project:
ASIC to prototype 2 (and some of 3).

- Typical input characteristics:

Specification	"Typical" Values
MCP Gain	500,000
Input strip capacitance	6 - 17 pF
Input noise	800 – 1300 electrons
Event Rate	~32 MHz

- ASIC specifications:

Specification	Value (Existing w/ RD20)	Value (Proposed ASIC)
Channels	32 channels each	8 channels each
CSA Rise time	~40 ns	~10-20 ns
CSA Fall time	~200 ns	
Conversion gain	0.72 mV / 1k electrons	
Noise floor	~(500 + 50/pF * C_{load}) electrons	
Sampling Rate	50 MSa/s	1 GSa/s
ADC	External 12 bit/50 MHz AD5271	Internal 10 bit Wilkinson ADC