Large Analog Bandwidth Recorder and Digitizer with Ordered Readout (LABRADOR) ASIC

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ABSTRACT

This article describes the most recent generation of full-custom analog integrated circuit that is intended for low-power, high-speed sampling of Radio-Frequency (RF) transients in excess of the Nyquist minimum. A direct descendant of the Self-Triggered Recorder for Analog Waveforms (STRAW) architecture, and earlier variants of the LABRADOR (Large Analog Bandwidth Recorder and Digitizer with Ordered Readout) architecture, this design is distinguished in that readout speed is improved and dynamic range extended by providing direct digitization inside each storage cell. While direct analog access to the stored values is lost, the simplifications gained by not transferring the small analog storage values result in operational ease. In addition to the 8 RF channels, a 9th "timing" channel has been added to provide better system timing. A nominal conversion cycle requires 100μs, with an additional 50μs required for data transfer.

Keywords: Askaryan Impulse detection, high speed digitizer, GSa/s, Ultra-High Energy (UHE) neutrino detection

1. Introduction

High efficiency acquisition of band-limited impulsive transients, such as those from the desired Askaryan effect [1] neutrino events, requires multiple Giga-Sample/second (GSa/s) recording in excess of 1 GHz of analog bandwidth. An integrated circuit capable of both triggering on and recording of such signals was proposed [2] in conjunction with the ANITA project [3]. In the process of developing and evaluating the STRAW [4] architecture, it was realized that operation of simultaneous triggering and sampling required significant complexity, without significant benefit. This is due in part to resource conflicts in the design, which is 5-layer metal routing and Input-Output pin constrained. By changing the emphasis of the STRAW architecture to be predominantly triggering, a split-off of the design could focus on optimizing sampling and digitization performance.

Staying within the same 100-pin Thin Quad Flat Pack (TQFP-100) packaging adopted for the STRAW series (motivated by economics of packaging and die size), a natural architecture that evolves is a chip with 8 differential RF inputs and 12-bits of digitized data output. In support of sampling and digitization, a number of pins are added which allow for random access of storage cells. The benefits and difficulties of this architecture choice were explored in 2 previous generations of LABRADOR architecture. All closely similar in design, the items specifically addressed in moving to a 3rd generation are the following:

1. improved dynamic range: by providing digitization of each stored sample directly within each storage cell, there are a number of benefits:
    a. decreased sensitivity to noise pick-up in transferring signals around the chip
    b. extended linearity by not involving a transimpedance stage
    c. shorter digitization time by making maximally parallel
    d. simplified acquisition cycle, insensitive to analog cross-talk on readout buses

2. improved wrap-around: augmenting the nominal 256 storage cells are 4 cells of "tail catcher" to fill in the sampling details during the interval in which the write pointer is wrapping back around to the beginning of the array

3. front-end termination scheme: allows maintaining a proper 50Ω stripline across the chip, while avoiding IR drop issues across the array.

4. addition of a 9th channel: provides for a copy of the system timing reference, which is distributed globally via the TURF (for ANITA) and can be interpolated to the requisite precision, event-by-event, to aid precise event timing reconstruction

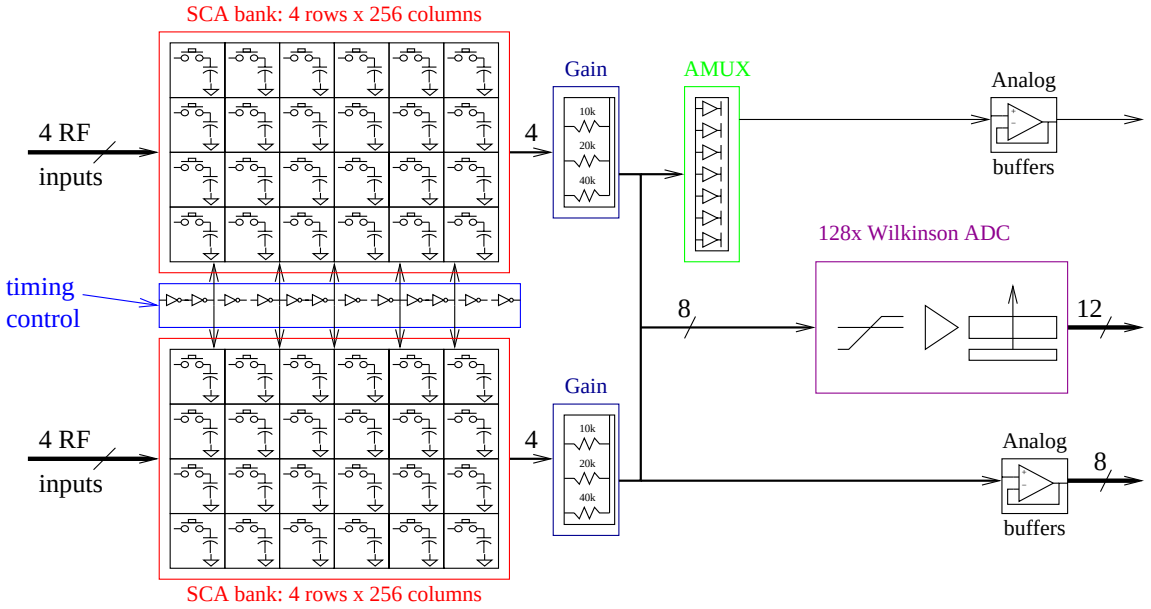
5. improved power supply connections: by simplifying the control requirements, a reduction in the number of control pins was attained. These subsequently freed pins have been used to improve the power and ground contacts for the die.

6. simplified biasing: by reducing the number of bias items required for manipulation of the transfer of analog signals, reduction in operational complexity is realized.

2. Architecture

At the top of Figure 1 is found a block diagram of the LABRADOR/LABRADOR2 architecture; at the bottom of this same figure the LABRADOR3 architecture is shown for comparison. As seen, the key difference is the simplification of not moving the samples to an array of ADCs. Instead, each storage cell contains an ADC. Sampling of the RF inputs is obtained by a narrow write-pointer moving across a standard Switched Capacitor Array (SCA) arrangement, the principle of which is demonstrated in Figure 2, and the basics of this SCA sampling are described in detail elsewhere [5].

LABRADOR(2) architecture



LABRADOR(3) architecture

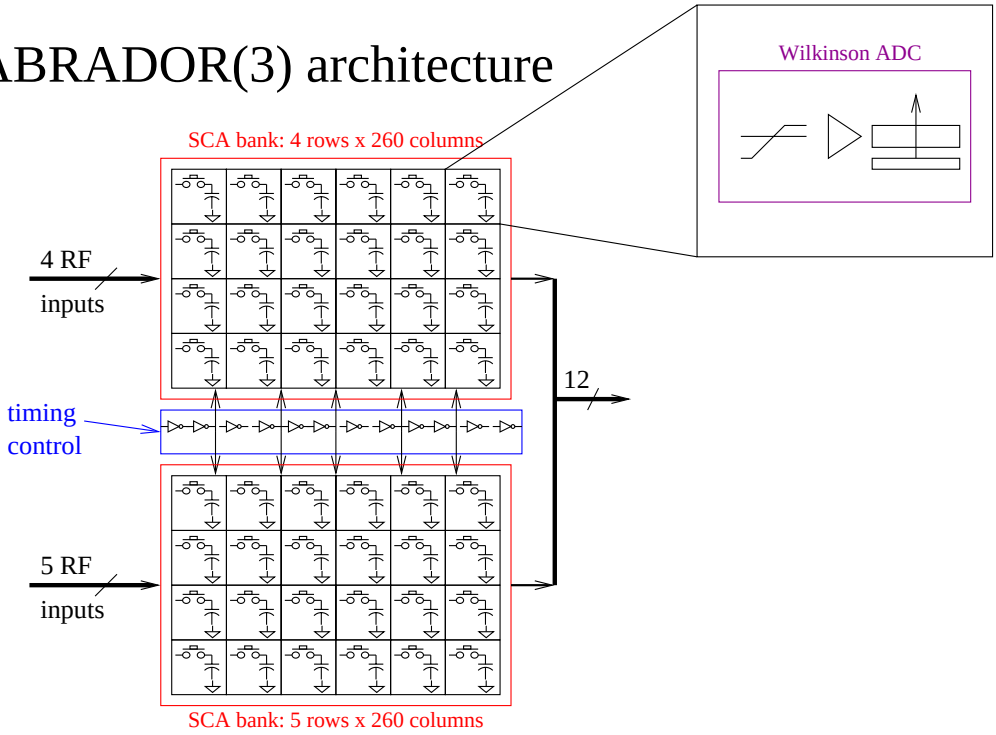


Figure 1: A block diagram comparison of the LABRADOR/LABRADOR2 chips (top) and LABRADOR3 chip (bottom). Note that in the latter case, a bank of 256+4 = 260 sampling Switched Capacitor Array (SCA) cells observes each of the 8 input RF signals, and an additional timing signal. For maximum possible digitization speed and simplification in readout, each SCA storage cell contains a 12-bit Wilkinson ADC.

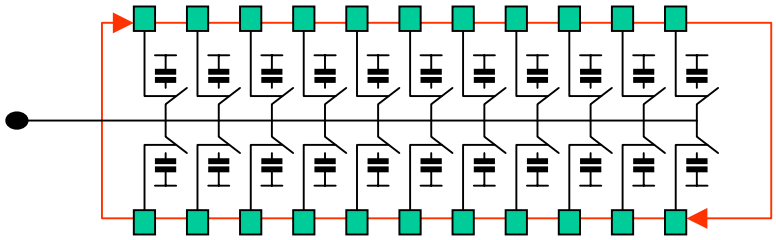


Figure 2: A rough illustration of the Switched Capacitor Array (SCA) sampling upon which the LABRADOR design is based. The write pointer circles endlessly, charging storage capacitors to the instantaneous bus voltage and holding the sampled value when the write pointer moves on, opening the switch.

2.1. Sampling Frequency

Sampling into the SCA array is continuous, with the values held and subsequently digitized only when a trigger signal is received. In doing so, a drastic reduction in the required power for sampling is achieved. Adjustment of the sampling rate is obtained by tuning the VDD and VSS power supply rails for a ripple oscillator chain, the sampling speed response for which may be seen in Figure 3. This is in contrast to the STRAW chip, where the sampling frequency could only be adjusted by varying VDD. As a result, the sampling frequency may be adjusted to a much lower value and positive-negative transition effects minimized. For many applications, it is more convenient to set ROGND to ground, the response curve for which is shown in Figure 4.

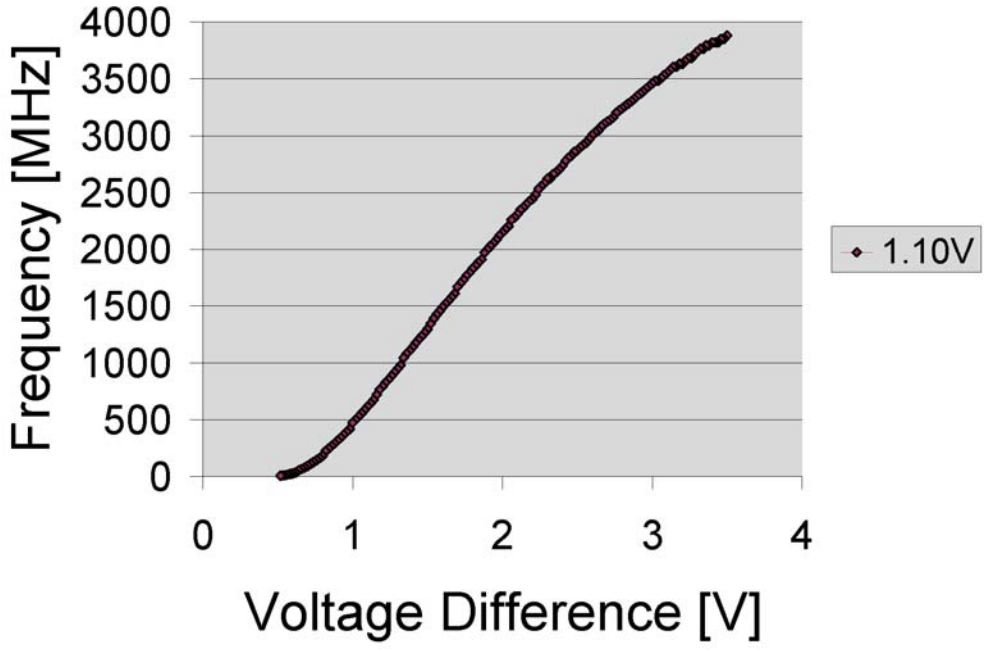


Figure 3: Sampling frequency versus applied adjustment voltage difference, nominally centered about VDD/2 ~ 1.25V (1.1V case shown). The simplified case for ROGND grounded is illustrated in Figure 4.

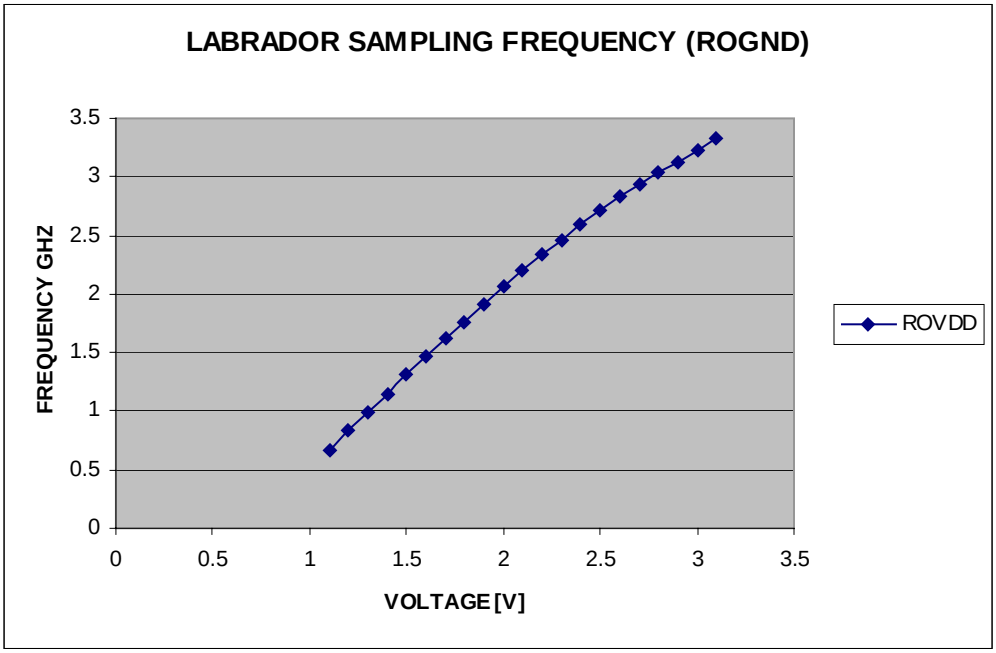


Figure 4: Sampling frequency for ROGND grounded, essentially reproducing sampling rates observed with the STRAW architecture.

Upon receipt of a trigger, a readout cycle begins and consists of an ADC conversion cycle, described in Sub-section 2.2 and a transfer cycle, described in Sub-section 2.3. As noted in Figure 1, the on-chip ADCs can digitize all 9 x 260 samples (2,340) in parallel, which greatly speeds the analog to digital conversion process. Compared with the complexity of LABRADOR/LABRADOR2 analog transfer, digitization, and readout this simplified readout consists solely of one digitization cycle, followed by transfer of the signals out from the array as fast as possible.

2.2. ADC Conversion cycle

A Wilkinson ADC makes use of a voltage ramp, a counter (Gray Code) and a comparator to convert a voltage into a count value. The count value stored is the instantaneous one when the comparator threshold is crossed. Analog biases (discussed in the next section) should be adjusted to accommodate a ramp that is matched to a 12-bit counter full count period. At 33MHz, this corresponds to approximately 100μs. Faster conversion times have been obtained at higher clock rates and increased slew rates. No significant degradation has been observed with a 100MHz clock, corresponding to a conversion time of 40μs. A detailed description of working, reference firmware is described below and shown graphically in Figure 5.

Firmware timing cycle: as detailed in Table 1, LCNT_Done starts Block "Lab_ADC". Q_DG1 and Q_DG2 are the internal signals to generate DRC and GCCLR signal. DRC is the signal to clear the data register, while GCCLR is the clear signal to clear the gray code counter. Several clocks after DRC and GCCLR signal, Ramp signal starts. In the meantime, GCK, the Gray Code Counter Clock starts. Since this is a 12-bit Wilkinson ADC, after 4096 clock (CLK) cycles, Ramp and GCK stop while ADC_Done signal is on. ADC_Done starts next block: "Lab_ADC2FIFO". When the 16-bit counter finishes counting, Clear_Cnt is on for a WCLK to clear the counter.

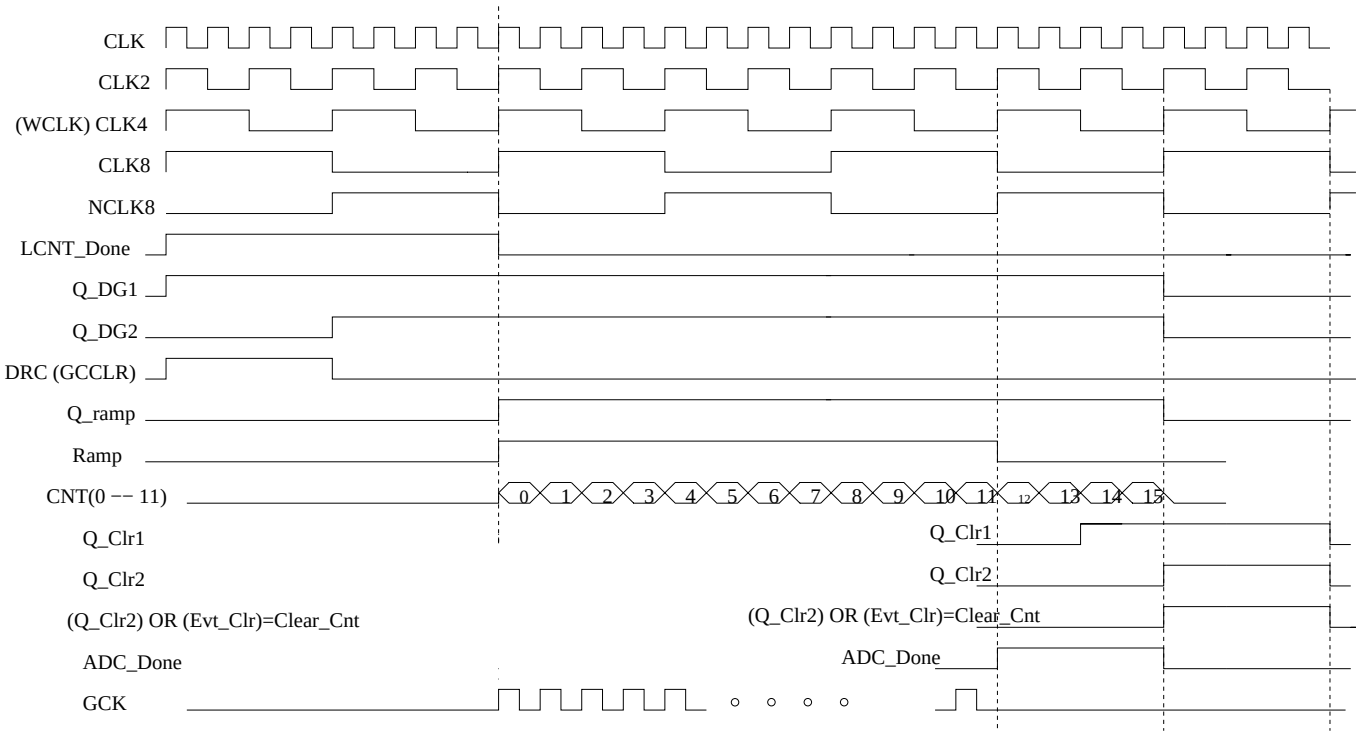


Figure 5: Timing diagram for ADC Conversion. (Corresponding .sch file: Lab_ADC)

Table 1: Signal Functional Description for Figure 7 (Block "Lab_ADC").

Signals	Description
LCNT_Done	Enable signal to start Block "Lab_ADC"
Q_DG1, Q_DG2	Internal signal to generate DRC and GCCLR signals
DRC	To clear the data register. It should be on before the Ramp signal happens.
GCCLR	To clear the gray code counter. It should be on before the Ramp signal happens.
Q_ramp	Internal signal to generate Ramp signal
Ramp	ADC Ramp signal
CNT(0 – 11)	Counter signal
Q_clr1, Q_clr2	Internal signal to generate clear_cnt signal
Clear_cnt	Clear signal to reset the 16-bit counter
ADC_Done	CNT(12) is used as "ADC_Done" signal here.
GCK	Gray code counter clock

2.3. ADC Data transfer

Data stored in the ADC registers may be randomly accessed, which can reduce readout latency in the case where not all channels need to be read out. Select lines **S0** through **S7** select one of 256 columns when **SELmain** is active. Lines **S0** and **S1** decode one of the 4 "tail" sample columns when **SELtail** is active. Note: **SELmain** and **SELtail** must not be active at the same time in order to avoid a bus conflict.

With a column selected, all 9 possible channel samples are available to an output multiplexer. Select lines **CS0** through **CS3** determine which of these channels are presented at the output of the LABRADOR3 chip. Ultimate readout speed will be determined by the internal and external bus skew and settling time. With careful timing considerations, readout at 100MHz should be possible, corresponding to about 25μs.

3. Implementation Details

Acquisition of high quality RF data from the LABRADOR3 chip requires careful attention to detail in the implementation of the accompanying control and biasing circuits. A major improvement in the third version of the LABRADOR chip has been the simplification of the biasing circuitry. Input coupling is also simplified by a modification to the internal termination structure, which should provide a proper 50Ω termination, as well as removing a DC slew across the sampling array.

3.1. Input Biasing Circuits

Correct operation of the SCA sampling array requires the biasing of the DC offset of the ac-coupled RF inputs. A low impedance, low inductance connection to a power reference at the desired offset voltage is suggested. In practice, a microstrip or stripline can be used with analog ground as the reference plane up until the ac-coupling capacitor. After this natural break, and continuing under the input section of the LABRADOR3 chip is this offset voltage, which may be coupled into the reference voltage input. For symmetric signals, the optimal value for this offset is in the range of 1.2-1.3V. In the case of a single-ended signal, for instance for a PMT signal, this offset can be adjusted to maximize the usable dynamic range.

The choice of ac-coupling capacitor depends upon the desired signal cut-off frequency. For RF sampling, there is no benefit to allowing lower frequencies than useful. At 10MHz this corresponds to about 260pF and at 100MHz about 26pF. As a high-pass filter, the choice of capacitor may be calculated as:

$$C = 1/(2\pi * 50\Omega * f_c)$$

Where the 50Ω corresponds to the termination resistance of the LABRADOR3 and fc is the desired cut-off frequency.

3.2. Suggested Chip Bias Values

The suggested set chip biases for the LABRADOR2 are listed in Table 2, which have proven optimal for operation and are those used in the subsequent performance plots shown.

Resistor name	Chip pin	Nom. value	comment
Rbias	Vbias	50k	Sets Wilk ADC comparator bias
RSBbias	SBbias	50k	Sets Ramp Gen. Buffer amp bias
RIsel	ISEL	68k (27k fast)	Sets slope of Wilk ADC ramp

Table 2: Suggested LABRADOR3 analog bias resistor values.

3.3. ECOs from the STUD and SURFv2 Implementations

Refer to the updated schematics located at http://www.phys.hawaii.edu/~idlab/ for the most current ECOs implemented on various test boards.

4. Performance Expectations

To allow a designer to estimate the performance that may be expected of the various aspects of the LABRADOR3 analog performance, a few measurement plots are shown below. A more comprehensive summary may be found in the STUD or SURFv2 Testing Summaries, which will be prepared and will be made available on the ID Lab web site when they are completed.

4.1. ADC Performance

Figure 6 below shows a linearity scan for the Calibration ADC inside the LABRADOR, which is identical to those that comprise the rest of the Wilkinson ADCs of the main sampling array. Excellent linearity is observed over 0.4-2.1V with the standard parameters shown in Table 2. The fitted gain is approximately:

1.6 counts/mV or 0.6mV/least count

Compression occurs at the upper and lower end of this plot and some additional calibration may be required to make use of this range.

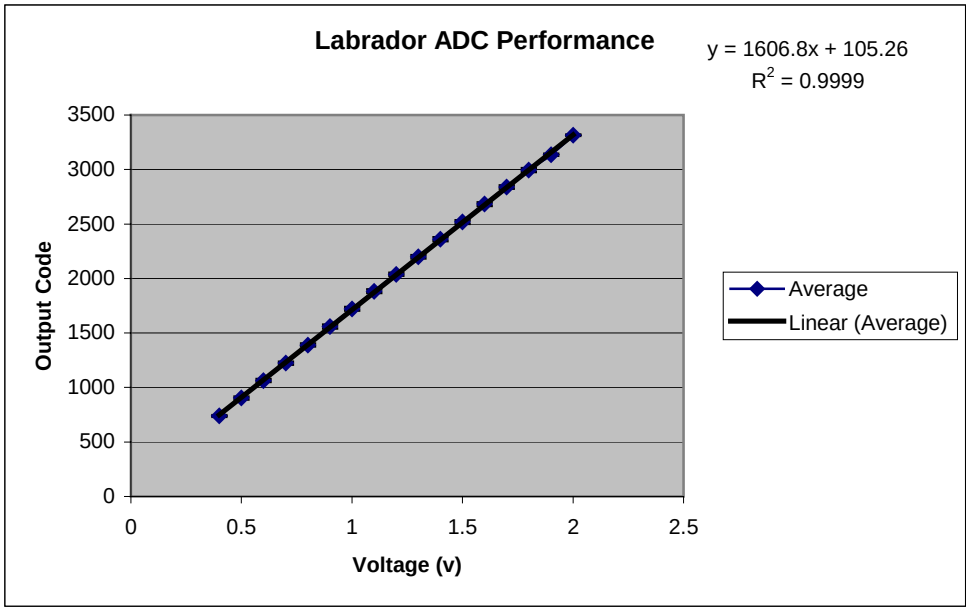


Figure 6: Measured on-chip ADC response to a calibration input voltage. A 12-bit code is latched when a comparator determines that the input ramp voltage has exceeded the reference voltage threshold. Compression occurs near the upper and lower power rails.

4.2. Dynamic Range

From previous performance measurements with LABRADOR and LABRADOR2, a few counts of noise are attainable for the gain indicated in the previous subsection. For 12-bits, corresponding to 4096 total counts, this places the usable dynamic range in the range of 9-10 bits above noise. Optimizing the signal range to match these is the job of the design engineer who will employ the LABRADOR3 chip. This optimization involves a combination of choosing input signal gain, ramp speed and encoding range.

4.3. Frequency Response

A key parameter for the successful operation of the LABRADOR as a GHz bandwidth, greater than Nyquist sampler, is the frequency response. As seen in Figure 7, there is some amount of resonance being developed for periodic signals between about 600 – 850 MHz for the LABRADOR chip as implemented on the SURFpro board. This is believe to be attributable to an LC resonance between the TQFP bonding wires and the internal capacitance and is under investigation. Confirmatory evidence is seen in Time Domain Reflectrometry measurements where there is a peak in the VSWR in this same range. Repackaging the die onto a BGA package may improve the situation. The situation may be somewhat modified for LABRADOR3 as the internal termination scheme is different. Detailed testing will be performed.

Further test results will be posted on the Instrumentation Development Laboratory web site as they become available, though since the RF part of the LABRADOR3 is almost identical to LABRADOR(2), only modest differences are anticipated.

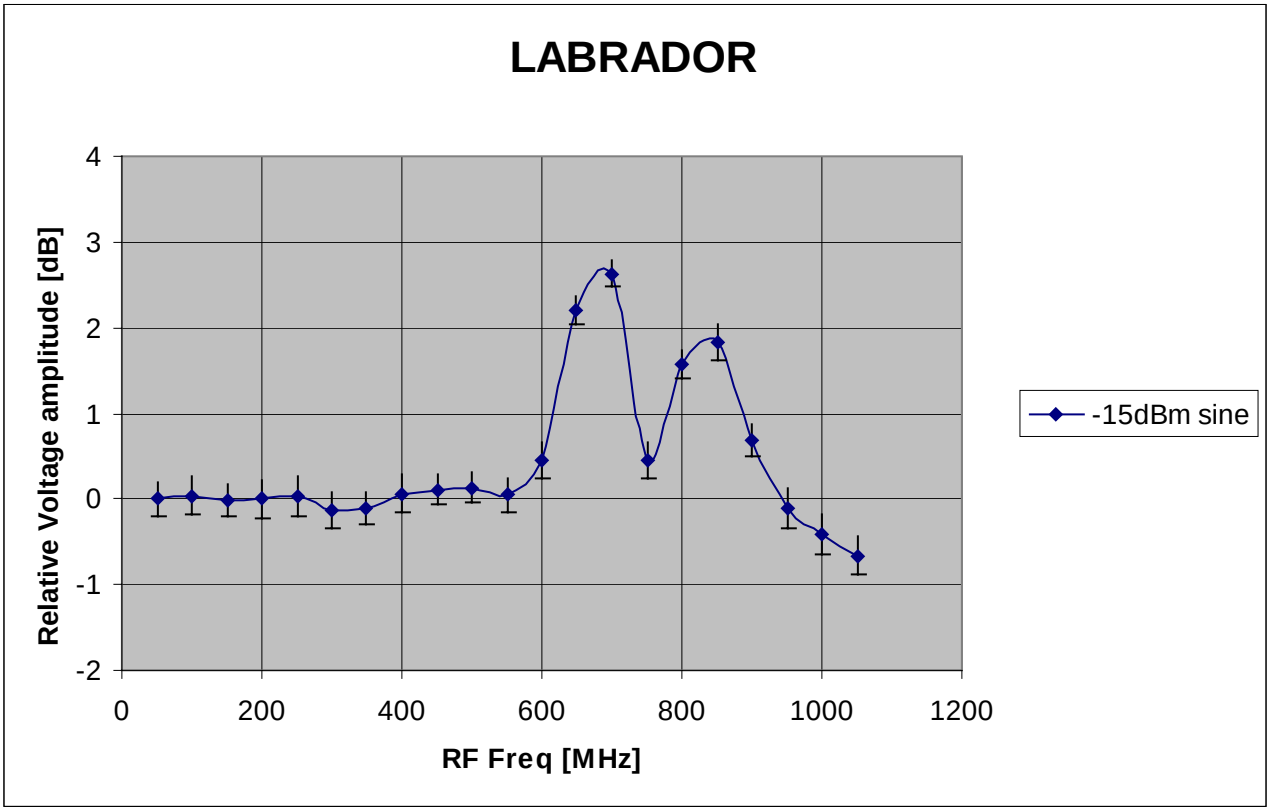


Figure 7: Frequency response roll-off of the LABRADOR input as a function of sine wave frequency.

5.Pinout

In order to implement the LABRADOR3 a listing and description of the pins may be found in the following tables:

- Table 3 – a listing of RF inputs and Frequency control
- Table 4 – a listing of DC power pins
- Table 5 – a listing of biasing and ADC control pins
- Table 6 – a listing of readout and readout control pins

Table 3: Pin numbering and pin functional description for the RF related parts of the LABRADOR3 chip.

Section	Pin #	Pin name	Description	Comments
RF inputs	1	VIN1	RF input #1	50 Ω between pair
	2	VREF1	ground reference for RF in #1	
	4	VIN2	RF input #2	50 Ω between pair
	5	VREF2	ground reference for RF in #2	
	6	VIN3	RF input #3	50 Ω between pair
	7	VREF3	ground reference for RF in #3	
	9	VIN4	RF input #4	50 Ω between pair
	10	VREF4	ground reference for RF in #4	
	14	VIN5	RF input #5	50 Ω between pair
	15	VREF5	ground reference for RF in #5	
	16	VIN6	RF input #6	50 Ω between pair
	17	VREF6	ground reference for RF in #6	
	19	VIN7	RF input #7	50 Ω between pair
	20	VREF7	ground reference for RF in #7	
	21	VIN8	RF input #8	50 Ω between pair
	22	VREF8	ground reference for RF in #5	
	24	VIN9	Timing reference input (Ch #9)	50 Ω between pair
	25	VREF9	signal reference for Ch #9	
Sampling Freq.	57	RCO	Ripple Carry Out	see section 2.1
	11	ROVDD	Ripple Oscillator VDD	
	12	ROGND	Ripple Oscillator GND	

Table 4: Pin numbering and pin functional description for the RF related parts of the LABRADOR3 chip.

Section	Pin #	Pin name	Description
VDD	8,18,27,29,40,42,48,58,66,74,79,87,88,90,92,94,96,98,100	VDD	+2.5V supply
GND	3,13,23,26,28,39,41,46,53,56,59,67,76,85,86,89,91,93,95,97,99	GND	[VSS] -- tie to AGND

Table 5: Pin numbering and pin functional description for the analog biases and ADC control and monitoring.

Section	Pin #	Pin name	Description	Comments
Biases (Table 2)	47	Vbias	Wilk Comparators bias	pull-up R
	50	SBbias	Ramp signal buffer	pull-up R
	52	ISEL	Wilk Comparators bias	pull DOWN R
ADC Control and Monitoring	44	TCS	Test Channel Select	0 = off; 1 = selected
	45	CalSnH	Calibration Sample not Hold	0 = hold; 1 = sample
	49	VrampMon	Monitor port for Wilk Ramp	buffered output
	51	VrampRef	Ramp connect pin	attach external C
	54	RAMP	Ramp generation signal	0 = discharge; 1 = Ramp
	55	RSS	Ramp Source Select	0 = direct; 1 = indirect
	77	GCCLR	Gray Code Counter Clear	1 = reset
	78	GCK	Gray Code Counter Clock	increment on rising edge
	84	nRUN	not RUN	0 = SCA sampling; 1 = Hold

Table 6: Pin numbering and pin functional description for the readout and readout control pins.

Section	Pin #	Pin name	Description	Comments
Data Bus	73	DAT0	Data bus lsb	12-bit binary samples
	72	DAT1	Data bus bit 1 (count from 0)	
	71	DAT2	Data bus bit 2	
	70	DAT3		
	69	DAT4		
	68	DAT5		
	65	DAT6		
	64	DAT7		
	63	DAT8		
	62	DAT9		
	61	DAT10		
	60	DAT11	Data bus bit 11 (msb)	
Column Addressing	30	SELmain	Column Select Enable (256)	see section 2.3
	31	S0	Column Select bit 0 (lsb)	
	32	S1		
	33	S2		
	34	S3		
	35	S4		
	36	S5		
	37	S6		
	38	S7	Column Select bit 7 (msb)	
	43	SELtail	Column Enable (tail 4)	
Row Addressing	83	CS0	Channel Select bit 0 (lsb)	
	82	CS1		
	81	CS2		
	80	CS3	Channel Select bit 3 (msb)	

Misc.	75	HitBus	Write pointer marker	Stop Marker (output)

6.Chip Layout and Packaging

All LABRADOR are currently packaged in a square TQFP-100 package and a die photograph is shown below, with dimensions of approximately 2.5mm^2.

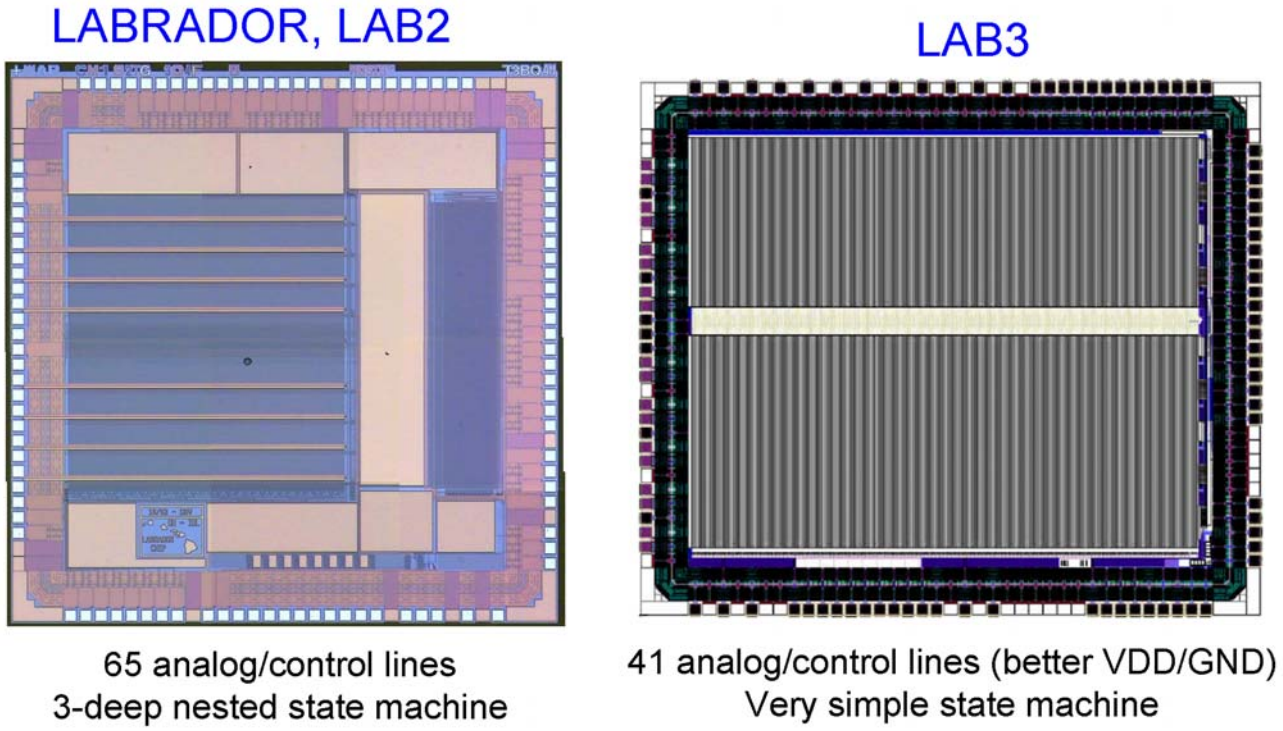


Figure 8: A roughly to scale comparison of generations of the LABRADOR chip. Stripline RF inputs couple in at the left. A column of 128 Wilkinson ADCs are found to the right of the sampling arrays for LABRADOR and LABRADOR2, while the LABRADOR3 has the array densely packed with ADCs. As a result the die is slightly wider, though maintains the same height.

7.References

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