Evaluation of Giga-bit Ethernet instrumentation for SalSA electronics readout

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Abstract

An instrumentation prototype for acquiring high-speed transient data from an array of high bandwidth antennas is presented. Multi-kilometer cable runs complicate acquisition of such large bandwidth radio signals from an extensive antenna array. Solutions using analog fiber optic links are being explored though are very expensive. We propose an inexpensive solution that allows for individual operation of each antenna element, operating at potentially high local self-trigger rates. Digitized data packets are transmitted to the surface via commercially available Giga-bit Ethernet hardware. Events are then reconstructed on a computer farm by sorting the received packets using standard networking gear, eliminating the need for custom, very high speed trigger hardware. Such a system is completely scalable and leverages the enormous capital investment made by the telecommunications industry. Test results from a demonstration prototype are presented.

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1. Motivation

Detection of Ultra High Energy (UHE) neutrino interactions requires immense effective target volumes due to the miniscale flux of such highly energetic, weakly interacting particles. Recently a number of initiatives [1,2] have been proposed to exploit the electromagnetic impulsive signature for UHE neutrino interactions, named in honor of Askaryan [3] who predicted the phenomenon. Any dense material may serve as a target, however, for the shower-induced radio impulse to be observable, a radio transparent target material is required. Two candidates that have been extensively explored are ice and salt [4]. A concept drawing for an antenna array is shown in Fig. 1. The readout system presented here can work with either media.
though the extreme low-temperature operating environment of the Antarctic ice [1] makes the off-the-shelf component solution less attractive. Therefore the initial effort has focused on developing a prototype for doing an exploratory borehole test in a salt dome. In order to detect the pulses of interest with high sensitivity, direct digitization of a large bandwidth is required. Also, the ability to trigger with thresholds right at the thermal noise limit is required. A full-custom CMOS integrated circuit has been designed to meet these requirements [5]. The architecture of this Self-Triggered Recorder for Analog Waveforms (STRAW) contains functionality for both triggering as well as sampling the RF pulses, as indicated in Fig. 2.

A number of readout architectures have been considered, including direct copper cable transmission, analog fiber optic link and high-speed differential copper links, both digital and analog. Since the transmission distances can be many kilometers, frequency-dependent attenuation can become severe. To minimize this, higher quality cable may be used, though the bundle thickness becomes an issue, especially since it must pass through all subsequent antennae en-route to the surface. A number of commercial analog fiber optic links are available, though these products typically have marginal dynamic range and are very expensive. Provided the concept of antenna local triggering and digitization is acceptable, it is much easier to deliver select data to the surface digitally. Within this framework, many commercial data transmission standards are available. Given the ubiquitous nature of the Ethernet standard and the desire to reconstruct and process events in parallel, aided by hardware packet sorting, the Giga-bit Ethernet (GbE) standard is an attractive option. To explore the performance and limitations of this approach a Giga-bit Ethernet Instrument for SalSA Electronics Read-
out (GEISER) was conceived. A drawing of a single antenna readout is shown in Fig. 3. Subsequent sections describe the design, fabrication and test of this GEISER prototype.

2. Specifications

In order to fulfill the functionality dictated by the configuration of Fig. 3, the ability to self-trigger is essential. At the time of the design of the initial readout prototype based on GbE, only the first fabrication iteration of the STRAW chip (STRAW2) was available. The requirements are summarized below.

Required design features for GEISER:

- better than Nyquist limit sampling of the dual RF antenna inputs at the thermal noise limit over the 100’s of MHz of signal BandWidth (BW),
- ability to trigger on band-limited transients,
- computer controlled RF trigger thresholds,
- continuous monitoring of the RF received power,
- low power, fast triggering,
- precise synchronization with a global timing reference,
- less than 1 ms latency.

Of these, constraints on simplifying the initial prototype precluded meeting these last two items. A block diagram of the GEISER is shown in Fig. 4. A trigger condition is actuated when the received pulse exceeds a DAC selectable threshold. Acceptance of a trigger causes analog samples held by the STRAW chip to be digitized. As STRAW2 was used in this prototype, an external ADC was
used. The STRAW chip has 16 RF input channels, each of which has 256 switched capacitor array storage cells. In order to maximize the sampling window while maintaining effective sampling rates in excess of the Nyquist limit, each RF input channel is interleaved sampled on 4 STRAW inputs. At 2GSa/s effective sampling, this corresponds to a sampling window \( \frac{C}{24} \approx 500 \text{ns} \) wide. As beam test results prove the received RF pulses will be band-limited, the required sampling window is more than adequate to capture the pulse as well as provide pre- and post-baseline sampling.

As seen in Fig. 4, the digitized data is collected from a FIFO located in the STRAW2 Digitizing Module block and formed into frames, which are transmitted as blocks by the LSI Controller. The output of this packetizer has been put through 8–10b encoding for error coding and is transmitted over the 10bit interface shown to a Serializer/Deserializer (SERDES) which converts the data into a bit serial stream. This bit stream is then put through an Electro–Optical converter, which broadcasts the data over a single-mode fiber optic cable. In order to facilitate synchronization of the link, the GbE link is actually bi-directional. This feature will be essential in flow control and timing synchronization amongst antennas in an actual system test and deployment but the downstream link was not explored in this first pass.

3. Board design

As the impetus of this design was to evaluate the functional performance of components and concept, little effort was made to make the board compact. In addition, as some of the functionality that should have been integrated inside the STRAW2 was implemented externally, additional space was required. A photograph of the completed board is provided in Fig. 5, with the key components highlighted.

4. Debug and evaluation

As betrayed by the wires added to the board in Fig. 5, some amount of modification to the original design was required in order to fix implementation flaws. Initial testing as part of a student project demonstrated that the board was essentially working. However, subsequent, arduous and painstaking debugging was required to fix a serious problem with dropped packets. A valuable lesson learned is that in future revisions, the ability to cache and retransmit dropped packets will be quite valuable. As the external readout of the STRAW2 chip is serial analog, followed by digitization, a significant amount of deadtime is incurred. This was expected, since 16 channels of 256 samples is 4k digitization samples.
Given the analog settling time plus the ADC conversion time, about 4 ms is required per triggered event. With processing overhead, the total latency is about 5 ms, corresponding to a maximum trigger rate of about 200 Hz. In Table 1 is tabulated the results of a series of measurements performed of the data transfer vs. trigger rate.

For these measurements a PC running Red Hat Linux Release 9, kernel version 2.4 was used. A custom acquisition program was written by one of the authors (C. Zhu), which is based on the Packet Capture library (PCAP), major version 2, minor version 4. The sampled waveform was a multi-cycle burst 25 MHz sine wave with an amplitude matched to full-scale of the STRAW input. As can be seen, many of the failure modes and rates are tabulated. A summary of the overall Packet Error Rate vs. trigger rate is shown in Fig. 6. A definite trend is seen as the trigger rate approaches complete saturation of the processing capability of GEISER. Note that this is intentionally well below the GbE bandwidth, with the thought of minimizing trigger information transmission latency. At worst the value is still well below 0.1% and in certain circumstances might be acceptable. Addition of packet caching and retransmit capability would greatly improve the robustness of this data pipeline. Careful investigation of possible sources was inconclusive, though this level of error may already be acceptable. For reference, a Packet Error Rate of $5 \times 10^{-4}$ corresponds to an effective Bit Error Rate of about $10^{-9}$. At 200 Hz trigger rate, the average sustained transfer rate is $15$ Mbit/s, with a packet consisting of 9 frames, 8 of which are 1 kB and the 9th with 144 byte.

5. Outlook

As the functionality of individual GEISER boards has been demonstrated, the next logical step is to procure a router and attempt to build events from multiple GEISER boards. Given future resources this will be explored, preferably with a smaller form-factor that will more easily fit down a standard diameter drill hole. Addition of
Table 1
Evaluation of the GEISER performance as a function of trigger rate

<table>
<thead>
<tr>
<th>GEISER performance evaluation</th>
<th>1</th>
<th>2</th>
<th>5</th>
<th>10</th>
<th>20</th>
<th>50</th>
<th>100</th>
<th>200</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trigger rate (number of triggers per second) (R)</td>
<td>1E+05</td>
<td>8E+05</td>
<td>2E+06</td>
<td>4E+06</td>
<td>8E+06</td>
<td>2E+07</td>
<td>4E+07</td>
<td>8E+07</td>
</tr>
<tr>
<td>Number of frames received by filter (Nf)</td>
<td>4.0E+05</td>
<td>8.0E+05</td>
<td>2.0E+06</td>
<td>4.0E+06</td>
<td>8.0E+06</td>
<td>2.0E+07</td>
<td>4.0E+07</td>
<td>8.0E+07</td>
</tr>
<tr>
<td>Number of frames dropped by kernel (Nd)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>1479</td>
<td>12479</td>
<td></td>
</tr>
<tr>
<td>Number of misordered frames (Nm)</td>
<td>1</td>
<td>1</td>
<td>7</td>
<td>8</td>
<td>29</td>
<td>51</td>
<td>152</td>
<td>2212</td>
</tr>
<tr>
<td>Number of frames with incorrect type (Nt)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Number of frames with incorrect length (Nl)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>67</td>
</tr>
<tr>
<td>Number of correct packets received (Np)</td>
<td>44,443</td>
<td>88,887</td>
<td>222,216</td>
<td>444,437</td>
<td>888,863</td>
<td>2,222,176</td>
<td>4,444,291</td>
<td>8,886,920</td>
</tr>
<tr>
<td>Capturing duration (second) (T)</td>
<td>4.44E+04</td>
<td>4.44E+04</td>
<td>4.44E+04</td>
<td>4.44E+04</td>
<td>4.44E+04</td>
<td>4.44E+04</td>
<td>4.44E+04</td>
<td>4.45E+04</td>
</tr>
<tr>
<td>Fraction of frames misordered (Nm/R/400,000)</td>
<td>2.50E–06</td>
<td>1.25E–06</td>
<td>3.50E–06</td>
<td>2.00E–06</td>
<td>3.63E–06</td>
<td>2.55E–06</td>
<td>3.80E–06</td>
<td>2.77E–05</td>
</tr>
<tr>
<td>Fraction of packets corrupted (1–Np/R/T)</td>
<td>1.99E–05</td>
<td>8.62E–06</td>
<td>2.44E–05</td>
<td>1.56E–05</td>
<td>2.61E–05</td>
<td>2.02E–05</td>
<td>7.10E–05</td>
<td>3.78E–04</td>
</tr>
</tbody>
</table>

Input sine wave specification: 25 MHz, 700 mVpp, 1 cycle per burst period.
packet caching and multiple analog buffering will greatly improve the robustness against data loss. Subsequent versions of the STRAW architecture [6] have significantly reduced digitization time and

there is ample bandwidth yet available on the GbE link to accommodate significantly higher self-trigger rates if needed.

References

[6] G. Varner et al., The large analog bandwidth recorder and digitizer with ordered readout (LABRADOR) ASIC, physics/0509023, manuscript in preparation for submission to Nucl. Instr. and Meth. A.