The Belle Trigger System with the new Silicon Vertex Detector SVD 2.0


The Belle SVD Group

Abstract—During the summer shutdown of 2003 the new silicon vertex detector SVD2 was installed in Belle at the KEKB factory and started to take data in October 2003. It provides important improvements in the tracking capabilities and includes trigger functionality. In addition a new hardware trigger Level 1.5 was designed and installed which takes advantage of the digitized SVD hit data. The resulting improvement in the Belle trigger system will be important to deal with the increasing luminosity and higher beam currents of the KEKB factory which will produce expected Level 1 trigger rates of more than 1kHz.

Index Terms—Belle, KEKB, silicon vertex detector, VA1TA, trigger.

I. INTRODUCTION

The upgrade to the new Silicon Vertex Detector SVD2 in Belle [1] includes substantial improvements in the tracking and triggering capabilities of the Belle detector. Compared to the old silicon vertex detector SVD1 the polar angle acceptance has been increased from 23°-139° to 17°-150°. The chosen geometry includes a significantly smaller beam pipe which allowed the first layer to move closer to the primary interaction point (2.0 cm compared to 3.0 cm for SVD1). In addition a fourth layer of silicon was included in the design. More details about the mechanical structure of SVD2 can be found in [2].

One important issue of the old vertex detector was the limited radiation tolerance of the VA1 front-end readout chip. It was replaced with the VA1TA [3] chip by IDEAS [4] implemented in a 0.35 μm CMOS process. It is expected to have a stable performance up to a radiation dose of at least 20 MRad.

This VA1TA chip includes a digital trigger circuit which adds the capability of a fast trigger decision from the SVD. The trigger signals from these chips are produced about 300 ns after the beam crossing and will add additional tracking information to the Level 0 and Level 1 trigger system.
In addition, a new hardware trigger level is introduced as Level 1.5 which uses digitized hit information from the flash ADC system (FADC). These information are available about 25 $\mu$s after the positive Level 1 trigger decision and will be used to abort the readout of the subsystems of Belle. With high beam currents and depending on the occupancy of the subdetectors the readout of Belle takes in average about 50 $\mu$s with readout times up to 100 $\mu$s. With the Level 1.5 system the dead time of the detector can be therefore decreased significantly.

The Level 1.5 trigger can be further improved by merging the track information from SVD2, the central drift chamber (CDC) and the Time-of-Flight (ToF) system and results in a powerful rejection against remaining beam gas background events.

Without the update of the Belle trigger system the Level 1 trigger rates would reach rates of more than 1 kHz with the increasing luminosity and rising beam currents from the KEKB factory. With the improvements in the Belle trigger system the rates should be kept in the range 300-400 Hz.

More details about the SVD2 DAQ system can be found in [5]. The Belle detector is described in detail in [6].

II. THE GEOMETRY OF THE SVD2

The SVD2 is a 4-layer silicon vertex detector. The layers 1, 2, 3 and 4 consist of 6, 12, 18 and 18 full ladders, respectively. The geometry in r-$\phi$ can be seen in Fig. 4. Each full ladder is build by 2 half ladders in forward and backward direction which are made of 1, 2 or 3 silicon wafers (Double Sided Silicon Detectors, DSSD):

<table>
<thead>
<tr>
<th>number of DSSDs in</th>
<th>forward</th>
<th>backward</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer 1:</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Layer 2:</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Layer 3:</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Layer 4:</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>

All DSSDs have 512 readout strips in r-$\phi$ and r-z. As multiple DSSDs are merged in some half ladders there is an ambiguity of hits in the r-z readout (as can be seen in Fig. 5). Each half ladder is readout by one hybrid which contains 4 VAITA readout chips that can handle 128 channels each. The signals from a total of 110592 channels are readout by the hybrids, send to the repeater system which is located inside the Belle detector and from there passed on to the flash ADC system.

III. DESIGN OF THE FRONT-END READOUT ELECTRONICS

The architecture of the VAITA front-end readout chip [3] is shown in Fig. 1. Each chip handles 128 input channels and includes the analog circuitry for the pre-amplification and readout of the analog hit data (VA) as well as the implementation of a fast trigger logic (TA).

The input signals are processed by a preamplifier and a shaper with shaping times around 800-1000 ns. In a classical stop-and-hold architecture the analog signals are fed into a multiplexer. The analog values are then read out in series with a clock of 5 MHz and send for digitization to the FADC system.

The TA part uses the same preamplifier but uses a fast shaper whose shaping time can be selected between 75 or 300 ns. It is followed by a level-sensitive discriminator whose threshold can be set externally. A global threshold is valid for all channels of one chip and with 4-bit DACs, the so called trim DACs, each channel can be modified from this global value.

A High Pass filter reduces offset-spread across the chip and the trigger signal for each channel is produced by an edge-triggered monostable flip-flop. Finally all 128 channels are OR’ed and result in 1 trigger signal from each chip.
IV. THE FLASH ADC SYSTEM (FADC)

The FADC system plays a central role for all the trigger information coming from the SVD. It receives the TA fast trigger information from the front-end electronics, feeds them into a dedicated Level 0 processor and sends them to the global Level 0 and Level 1 trigger system.

The analog VA signals of the 4 VA1TA chips on one hybrid are readout in parallel with 5 MHz and then digitized in 10-bit flash ADCs. The digitized data are sent to the DAQ system via a PCI link for sparsification and event building (see [5]). The serial scan of one VA1TA chip takes about 25 $\mu$s.

The FADC system also prepares the digital hitmap for the Level 1.5 system from the same digitized data. For each strip a threshold is applied and the resulting digital hitmap send to the main Level 1.5 board with a 20 MHz clock.

V. THE LEVEL 0 TRIGGER

The Level 0 Trigger system makes use of the fast trigger signals from the TA part of the VA1TA front-end readout chip of the SVD. The 300 ns fast shaper was chosen and a global threshold set. Then the thresholds for each channel were tuned with the trim DACs. The strip efficiencies for each of the 4 layers in the backward side is shown in Fig. 2. After tuning the TA thresholds in the readout chips the following TA hit efficiencies in the 4 layers are achieved:

<table>
<thead>
<tr>
<th>Layer</th>
<th>Forward</th>
<th>Backward</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer 1</td>
<td>96%</td>
<td>92%</td>
</tr>
<tr>
<td>Layer 2</td>
<td>94%</td>
<td>93%</td>
</tr>
<tr>
<td>Layer 3</td>
<td>89%</td>
<td>73%</td>
</tr>
<tr>
<td>Layer 4</td>
<td>77%</td>
<td>77%</td>
</tr>
</tbody>
</table>

The efficiencies for layer 3 and layer 4 backward are lower, as 3 silicon wafers are combined to one half ladder and the signal-to-noise ratio becomes lower. The TA hit information are fed into a dedicated Level 0 processor which is included in the FADC system. Tracks are reconstructed with the given resolution which is defined by the 128 OR’ed strip signals. For each track 2-out-of-3 hits are demanded in the outer layers and the inner layer is always required. The single track efficiency from the SVD Level 0 system was estimated to be around 88% with the given TA hit efficiencies in the upper table. These numbers result from a data set of cosmic muon events taken during summer 2003. Tests with colliding beam data are currently performed.

The Level 0 decision from the SVD is merged with the decisions from the central drift chamber (CDC) and the Time-of-Flight system (ToF) to result in the global Level 0 trigger decision for Belle. This takes about 600 ns and is used to send the ‘Hold’ signal to the analog part of the VA1TA chip.

VI. THE LEVEL 1 TRIGGER

For the Level 1 trigger, the Level 0 tracking information are explicitly merged between the subsystems of SVD, CDC and ToF. For the global Belle Level 1 trigger decision also more information from other subsystems of Belle are included. The Level 1 decision is taken about 2.5 $\mu$s after the beam crossing and is used to start the readout of all Belle subsystems in general and the serial readout of the 128 analog channels via the multiplexer in the SVD2 in particular. The scan is done with about 5 MHz and is completed after roughly 25 $\mu$s. Studies on the efficiency of the Level 1 trigger are currently performed with colliding beam data.

VII. THE LEVEL 1.5 R-Z TRIGGER

The Level 1.5 trigger is based on the digitized strip data from the FADC system. The threshold that is applied to each strip signal is calculated from the pedestal plus five times the total noise for each strip. The total noise results from the square root of the squared sum of the common mode noise and the single
Fig. 5. Example of a cosmic event triggered by the L1.5 system. In this display the ambiguity of the hits in r-z is obvious. The hits shown in each layer correspond to 1 real hit in the layer. As 2 or 3 DSSDs are readout in parallel for the outer half ladders the location of the real hit is unknown.

strip noise. The digital hitmap is produced in parallel with the digitization during the serial scan of the analog 128 channels from the VAITA chip and immediately send to the main Level 1.5 board. Therefore the full hit information are available about 25 $\mu$s after a positive Level 1 decision. In order to keep the data volume in a reasonable size in the Level 1.5 board, 32 strips are merged to 1 trigger segment.

As tracks from beam gas background are homogenously distributed in the z-direction and the colliding beam data come from a narrow region around the nominal interaction point of less than 3 cm, the rejection of beam gas background is very powerful in r-z.

18 trigger wedges are defined by one of the 18 outer ladders as it is shown in Fig. 4. For the trigger logic 3 different geometries have to be considered as they are shown in the figure. Subsequent geometries are just rotated by 60°, otherwise they are identical.

In each of these 18 wedges tracking can be performed in r-z and an independent trigger decision taken.

The simulation in Fig. 3 shows that the single track efficiency is well above 90% for tracks coming from close to the interaction point ($|z| < 3.2$ cm in the simulation). The implemented logic demands hits in 3-out-of-4 layers, where the first layer always is required, in order to eliminate ghosttracks due to the ambiguity in the outer layers where 2 or 3 silicon wafers are combined to form one half ladder. In the simulation tracks with a transverse momentum between 200 Mev and 5 GeV were used.

From the simulation so called trigger terms are generated which are 4-tuples of trigger segment IDs, one number for each layer. These trigger terms are implemented in Verilog code and downloaded into 18 Xilinx Virtex II 1000 FPGAs, one for each trigger wedge. Some algorithms are applied to reduce the number of trigger terms which otherwise would be to large and not fit into the FPGAs.

The 18 independent trigger decisions from the the trigger wedges are then send to a so called Level 1.5 buffer board, where further track information from the central drift chamber (CDC) and the Time-of-Flight (ToF) system are collected. In addition the complete set of Level 1 trigger bits from the global trigger system can be received. In this board the logic is implemented in a Xilinx Virtex 600 chip which allows for very quick and flexible changes in the system.

If an event is rejected by the logic of the Level 1.5 system a signal is send to all Belle subsystems and the readout is aborted, decreasing the dead time of the DAQ system and reducing the final event rate.

Fig. 5 shows an example of a cosmic event that was selected by the Level 1.5 trigger in a cosmic muon run in summer 2003. Here the ambiguities of hits in the outer layers become obvious.

In fig. 6 the number of positive Level 1.5 triggers are shown for each of the 18 wedges. In total 400 events were collected in this run. A clear dependence of the angle of the incoming track is apparent. The wedges 0 and 9 are the ones which have a horizontal alignment, so clearly more up-down tracks can be observed than horizontal tracks.

Further studies are under way with the colliding beam data which started mid of october 2003. Especially efficiency studies and the rejection of background events is investigated in order to ensure good performance before including the Level 1.5 system into the global Belle trigger system.

VIII. Conclusion

With the upgrade of the Belle Silicon Vertex Detector a couple of major improvements in the tracking capabilities of Belle and the radiation hardness of the front-end readout electronics are achieved. The additional upgrade of the global Belle trigger system with information from the SVD for the Level 0 and 1 trigger system and the new hardware Level 1.5 trigger will be essential to handle the increasing luminosity and rising beam currents from the KEKB factory. The implementation of a large fraction of the trigger system in programmable FPGAs provides a very flexible and powerful working environment. First tests with cosmic events in summer 2003 show that both the detector
as well as the trigger system are working fine. Further studies with colliding beam data are under way and will show the functionality of the new system.

REFERENCES