RadFET Reader Sample Sequencer

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Timing Diagram

- TRIG
- Incr = T0
- Asel
- RSn
- Cena
- phi0
- phi1
- T0, T1, T2, T3, T4

Action States

- T1, T4
- T3
- T2

Trigger Source

M2_1

FD

D0, D1, S0

Ext_Trig, Int_Trig

Trig_SRC

VCC, GND

AND2B1

Asel

D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15

RS1, RS2, RS3, RS4, RS5, RS6, RS7, RS8, RS9, RS10, RS11, RS12, RS13, RS14, RS15, RS16

CB4CE
RadFET Sampling Rate Selector Block
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Frequency selector

~500 Hz

9 = div. by ~1k = 0.5 Hz

Serial select on opposite phase
Front Panel Selected

Front Panel Selected

RadFET Read Channel Selected

Serial Analog Output Channel Selected
Frequency selector

- FDC
- CB16CE
- BUF16

`~500 Hz`

- 8 = div. by ~1k = 1 sec

`8 = div. by ~1k = 1 sec`

[Viz_strobe]

makes RadFET read Strobe visible

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