Development of the CuEval FINESSE, a USB2.0 interfaced at-speed emulator for the new COPPER system

G. Varner, Y. Zheng, D. Shimokawa and B. Wei

University of Hawaii

Abstract

We are developing a high speed FINESSE mezzanine module for evaluating the newly designed high luminosity DAQ platform named COPPER, targeted for applications such as an upgraded Belle detector. Simulated sub-detector data is transferred from a Windows PC via a USB2.0 interface. In this way, continuous at-speed operation for the optimization channel density and data compression of sub-detectors and their electronics may be performed at the design stage. This module also serves to test the functionality and performance of the COPPER board.

1 Introduction

Upgrade of the KEKB collider toward $\mathcal{L} = 10^{35}\text{cm}^{-2}\text{s}^{-1}$ luminosity requires an upgrade of the Belle data acquisition (DAQ) system. To meet these requirements, as well as those for high luminosity experiments at the J-PARC facility currently under construction, a pipelined DAQ platform has been designed. This C0mmon Pipelined Platform for Electronics Readout (COPPER) [2] module contains four locations for standard interface mezzanine boards (FINESSE) [1], each of which digitizes front-end signals and pushes the data into FIFOs on the platform board upon receipt of a Global Decision Logic trigger. This DAQ platform accommodates a global data flow scheme which is same for different sub-detectors. In this way, all of the sub-detector specific front-end electronics are implemented on the plug-and-play FINESSE mezzanine cards, allowing great flexibility within a unified DAQ platform.
Before designing FINESSE cards for each Belle sub-detector, it is important to understand the FINESSE interface and gain experience with FINESSE card design. In addition, we also need software and hardware tools to check the functions and performance provided by the COPPER board. These factors lead us to develop a test FINESSE module, called CuEval (COPPER Evaluation), that can also help us gain experience for the next generation of Belle DAQ.

2 CuEval USB2.0 FINESSE Testing Card

2.1 Requirements and Solutions

To check the readout performance of the new DAQ platform, a FINESSE module, which is mandated to have a high continuous data flow connection between the data source and the pipelined buffers, is necessary. Figure 1 shows the design of such a testing module. It is equipped with a Cypress EZ-USB FX2 USB2.0 chip, which passes the data provided by the application software on a PC to the rest of the circuitry on the FINESSE module. There are two memory chips, each with a size of 256 kBytes implemented on the module. Thus, one memory chip can be read while writing to the other. These memory chips can function as an emulated synchronous buffer. To provide flexibility in the design, a Xilinx FPGA (Virtex xcv100e) is used to interconnect the USB interface with the memory chips. It reads the data in the FIFOs of the USB chip and passes them to the memory modules. Also on the CuEval there is one Xilinx CPLD chip to configure the xcv100e and connect the data in memory chips with the FINESSE interface.

2.2 USB Interface

Table 1 compares some of the more popular existing standards for transferring data at high speed. The USB2.0 interface can provide a transfer speeds of up to 480 Mbits/s. It is well supported by both the Windows and Linux operating systems. In addition, it is also designed as plug and play device without any demands for configuration on the user side. A cyclic redundancy check has already been implemented at the hardware level. Thus, we do not need to worry about the data transfer reliability. As a further incentive, the interface chip is inexpensive as well.

The Cypress EZ-USB FX2 chip is selected for the design. This is a USB2.0 chip with an 8051 compatible CPU integrated on it. This Cypress part is provided with a general purpose device driver under windows 2000/XP, which saved us quite a large amount of time by not having to develop a custom device driver.

For general hardware design purposes, there are four types of data transfers as shown in Table 2. We have chosen “bulk transfer” mode which provides fastest transfer speed [3].
Figure 1: A photograph of the USB2.0 FINESSE Testing Card (CuEval).

Table 1: A comparison of different standard data transfer interfaces.

<table>
<thead>
<tr>
<th>Interface</th>
<th>Format</th>
<th>Maximum Number of Devices/host</th>
<th>Speed (Max bits/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB2.0</td>
<td>Serial</td>
<td>255</td>
<td>480M</td>
</tr>
<tr>
<td>RS-232</td>
<td>Serial</td>
<td>2</td>
<td>20k ~ 115k</td>
</tr>
<tr>
<td>IEEE-1394 (FireWire)</td>
<td>Serial</td>
<td>64</td>
<td>400M</td>
</tr>
<tr>
<td>GPIB</td>
<td>Parallel</td>
<td>15</td>
<td>8M</td>
</tr>
<tr>
<td>Parallel Printer Port</td>
<td>Parallel</td>
<td>2 ~ 8</td>
<td>8M</td>
</tr>
</tbody>
</table>
Table 2: USB Transfer Types

<table>
<thead>
<tr>
<th>Data Transfer Type</th>
<th>Maximum data-transfer rate/endpoint (Bytes/sec)</th>
<th>Error Correction</th>
<th>Typical Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>16M</td>
<td>Yes</td>
<td>Configuration</td>
</tr>
<tr>
<td>Bulk</td>
<td>54M</td>
<td>Yes</td>
<td>Printer, Scanner, DAQ</td>
</tr>
<tr>
<td>Interrupt</td>
<td>25M</td>
<td>Yes</td>
<td>Mouse, Keyboard, Joystick</td>
</tr>
<tr>
<td>Isochronous</td>
<td>25M</td>
<td>No</td>
<td>Audio</td>
</tr>
</tbody>
</table>

3 Development Tools

We are using the Cypress reference design board CY4611 for understanding the hardware and software configuration. This board provides examples for designing the interface between USB and ATA100/COMPACTFLASH. The flexibility of the FX2 chip requires the firmware to handle the device configuration and initialization information. We use a Keil 8051 C and assembly compiler for compiling the USB firmware. Since the general purpose device driver provided by Cypress is supported under windows 2000/XP only, we use Microsoft Visual C++ for the development of applications such as detector simulation. We also use the Microsoft Driver Development Kit to compile the device driver source code [4]. Figure 2 shows the data flow between the application and the USB customized circuit.

4 Strategy for Bench Test

5 Status

6 Summary

A new FINESSE mezzanine module is designed and fabricated for testing the newly designed DAQ platform for Belle. To simulate the detector data with high transfer rate, we have utilized the USB2.0 interface for sending data to the DAQ platform from a PC. A Xilinx FPGA chip is used to realize the logic of communications between the simulation
Figure 2: An illustration of the USB data flow.
software on a PC and the memory buffers on FINESSE module. Another Xilinx CPLD chip is used to control the FPGA chip and exchange the data between memory buffers and DAQ platform through FINESSE interface.

References


