The primary functions of the firmware are to
- Control the reading of the pixel matrix by generating reset and clock signals for columns and rows
- Establish communication between pixel chip and ADC and FIFO
- Establish communication with DAQ

DESCRIPTION OF SIGNALS

TRIGGER

APT1_Clocks

All the functions of the firmware are initiated by TRIGGER – signal which is composed from incoming signal DIOC5 from the LabView – program. DIOC5 is run through two flip-flops and is set to clear i.e. to set output of first one to “0”. The output of the second one with duration of one clock pulse is labelled as TRIGGER.

TRIG_4  DISCARDED Formerly used for COL_CLK and ROW_CLK

The TRIGGER is led through a 4-bit shift register in order to delay it four clock pulses. The output Q3 of shift register is labelled TRIG_4.

PIXEL_RESET

APT1_Reset

The TRIGGER initiates the reset sequence which is performed by a 16-bit binary counter and a D flip-flop. Output of the flip-flop is set to “1” with TRIGGER. The output is used for feedback loop that maintains its state until the flip-flop is reset. This output is used to enable the counter clock. Counter is set to count four clock cycles. When the counter’s output has reached a value 0005 (output END_OF_RESET → “1”) the flip-flop is reset and the output is set to “0”. Next clock pulse sets PIXEL_RESET to “0”.

The duration of PIXEL_RESET can be set by selecting a suitable output of the counter to reset the flip-flop.
INTEGRATE

APT1_Integrate

After PIXEL_RESET is completed the integrate sequence is initiated. The setup for INTEGRATE is similar to RESET. The sequence starts with END_OF_RESET which is delivered to the input of a flip-flop. The INTEGRATE – signal stays high until END_OF_INTEGRATE - signal from counter sets the reset of the flip-flop. The clock input of the counter is enabled by DATAVALID which is derived from the DAV – signal from the LabView – program.

The duration of INTEGRATE is set by selecting an appropriate output of counter for the END_OF_INTEGRATE - signal.

READOUT

APT1_Readout

After integrate sequence is completed the READOUT is initiated by END_OF INTEGRATE. The duration of READOUT is set by a counter which provides the reset for flip-flop.

READOUT_DELAYED, END_OF_READOUT

APT1_Readout

READOUT is delayed for four clock cycles to form READOUT_DELAYED. This signal is split between an inverted input of an AND – gate and the flip-flop. The flip-flop delays READOUT_DELAYED for one clock cycle and END_OF_READOUT is generated by the output of the AND – gate.

REPEAT1, 3, 4

APT1_Readout

END_OF_READOUT is now split in the similar way as READOUT and led directly to non-inverted input of the AND – gate. The output of AND - gate is set to “1” since state of the inverting input is “0”. END_OF_READOUT is also used for the CE for the counter which after three clock cycles provides a “1” to the inverting input of the AND – gate and setting gate’s output to “0”.

Output of the AND – gate is labelled as REPEAT1 and the shift register delays this signal by two clock cycles and three clock cycles to generate REPEAT3 and REPEAT4 respectively.
COL_CLK  
APT1_MatrixControl

There are two conditions for COL_CLK to be generated: READOUT and DATAVALID, or REPEAT3. If either of case is present then the output in the OR – gate exists and this output is labelled COL. After being inverted and buffered, COL signal is transformed to COL_CLK.

COL_128  
APT1_MatrixControl

COL is also used as a strobe to the counter that counts and controls the number of COL_CLK pulses generated and generates COL_128 signal.

The outputs of the counter are set to “0” by TRIGGER which is connected to counter’s CLR – input through an OR – gate with COL_128. The counters CE is set constantly to “1” by Vcc. When counter has received 128 COL pulses, COL_128 (C7 of output bus) is set to “1”. COL_128 sets the outputs of the counter to “0” on the next clock cycle. This signal is also used to generate ROW_CLK and COL_RESET pulses.

ROW_CLK  
APT1_MatrixControl

The first ROW_CLK is made from the REPEAT3 signal. The subsequent ROW_CLK pulses are determined by COL_128 signal described above.

COL_RESET  
APT1_MatrixControl

The first COL_RESET occurs with the TRIGGER. The subsequent COL_RESET pulses are set by REPEAT1 or COL_128.

ROW_RESET  
APT1_MatrixControl

The first ROW_RESET is initiated by the TRIGGER. The subsequent ROW_RESET pulses are set by REPEAT1.
**WCK**

Conditions for enabling the WCK are: The DATAVALID and the READOUT_DELAYED or DATAVALID and WCK_ENABLE have to be present.

As default the WCK is set for 128 ROW_CLK and 128 COL_CLK pulses. The Pixel chip can also be divided to four segments and user can determine which of the segments is to be read. This is accomplished by setting one of inputs DIOC0…3 to “1”. These inputs are used as inputs for the first four inputs of a 10-to-4-line encoder. The outputs determine which inputs of two 2-to-1 multiplexers connected to outputs of the ROW and the COL counters are used.

These counters are used for providing state “1” as output during ROW:s and COL:s 64…128. By combining these outputs as such or inverted WCK_DISABLE is set for blanking the WCK - signal. The WCK - signal passes a latch controlled by WCK_DISABLE - signal only at the ROW:s/COL:s of desired segment.

The selection between default and segment reading is made with a multiplexer controlled by the DIOC0…3 inputs via an XOR gate. The XOR - gate is used to ensure that only one segment is designated. If however more than one controls are set to “1” the output of the WCK - signal is set to default.

The shift register in the WCK output is used to set proper delay between COL_CLK and WCK.

**ADC_CLK**

The requirements for the clock cycle of ADC clock are 374 ns minimum and 602 ns maximum. Since the clock frequency of the firmware chip is 40 MHz, the ADC clock is made by dividing the clock frequency to 2.5 MHz, which makes the ADC clock cycle of 400 ns. This is done by running the clock through a 8-bit counter and using bit 4 output as source of ADC_CLK signal.

**ST_CAL**

The requirement for the length of ST_CAL signal is four ADC clock cycles minimum. The DIOC4 signal from the LabView – program is labelled in firmware as INIT. The incoming pulse is driven through a flip-flop and is used to enable clock signal of a counter which provides a CLR to flip-flop after three clock cycles CE was set to “1”. The counter uses the ADC clock signal as clock input. The output of flip-flop is used as ST_CAL for ADC.
**NOT_READY**  
APT1_ADC_FIFO

CAL-END from ADC is labelled as END_CAL in firmware. This signal or signal described above is used as NOT_READY for LabView – program.

**RS**  
APT1_ADC_FIFO

The signal described in ST_CAL or TRIGGER - signal is used as inverted to form RS – signal to FIFO.

**RCKL**  
APT1_DAQ_comm

The END_OF_READOUT is use to form the SEND – signal running it through two flip-flops. The first one is clocked with a PCLK - signal derived from the CLK input by dividing frequency of CLK by two. The state of output of the flip-flop is sustained by feedback through OR gate. The output of the second stage, labelled SEND and ACK1 from LabView – program provide the CE for the counter that determines the duration of the SEND – signal. The RCKL - signal is formed from SEND and ACK1 and PCKL.

**REQ1**  
APT1_Top

After being inverted and buffered SEND signal is labelled REQ1.
OPERATIONAL DESCRIPTION

All the functions of the firmware are initiated by the TRIGGER – signal build from DIOC5 input from the LabView – program. The primary functions derived from the TRIGGER are:

- initiation of the PIXEL_RESET
- to provide the initial reset for the column clock and row clock for the pixel chip
- to set the outputs of the counter for the column clock pulses to “0”.
- to provide the RS – signal for resetting FIFO.
- to provide TRIG_OUT – signal for…
- to initiate WCK_ENABLE signal.

The PIXEL_RESET is used to clear the pixel matrix in order to prepare the pixel chip to be charged during the integrate period. When the PIXEL_RESET is initiated the column and row clocks are reset, i.e. both pointers are set to first column and row respectively.

From the DIOC4 – input the firmware gets signal which after being buffered is labeled INIT. This signal is used for providing ST_CAL for ADC. This signal launches self calibration sequence in ADC. During calibration CAL_END – output from ADC is set to “0” indicating that calibration is in process. This state is delivered via the firmware to the LabView – program to inform that ADC is in “not-ready” condition. After the calibration is completed the CAL_END gets state “1”, which indicates that the ADC is back to normal conversion mode.

The same signal which is used as such as the ST_CAL is used to deliver the “not ready” signal to the LabView – program, and after being inverted as the initial reset for FIFO.

After the integrate period is completed the reading of the pixel chip is initiated, i.e. the analog data from pixel chip is transferred to the ADC. The transfer is scheduled by the DATAVALID signal which is generated from the DAV – signal originated from the ADC. The clock signal for the ADC is derived form the clock signal of the firmware chip. The original clock frequency of 40 MHz is reduced to 2.5 MHz for the ADC.

The firmware generates clock pulses for shifting the column and row pointers. The pixel matrix is read column by column in 128 pixel rows controlled by COL_CLK – signal. When a counter for column clock reaches value 128, indicating the last column in the row, the COL_RESET and ROW_CLK pulses are generated to sift the pointers to the first column of the next row. This sequence continues until the pointer reaches the last column of the last row. As a default all the pixels are read, however pixel chip can also be divided to four 64 by 64 pixel segments and each of these segments can be read individually. This is done by selecting one of the four inputs DIOC1…3 to “1”.
The converted data from the ADC is transferred to the FIFO. The OE, output enable input of ADC, is constantly connected to Vcc in firmware in order to ensure continuous transfer to FIFO. The firmware controls the transfer by delivering a WCKL – signal to the FIFO. The data is transferred with every rising edge of WCKL. If however the FIFO is full and not able to receive data, the firmware gets a FF signal form the FIFO and all the functions related to reading and transfer data are disabled.

The DAQ asserts the ACK_1 signal to indicate it is ready to perform a transfer. After being inverted and buffered the SEND – signal, described earlier, is labeled REQ1. While both of these signals are present a transfer occurs between the test board and the DAQ on the rising edge of the PCKL signal.

In the firmware there are ten output pins assigned to signal monitoring. In the current version of firmware these signals are:

<table>
<thead>
<tr>
<th>MON #</th>
<th>Connector pin</th>
<th>Signal name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>7</td>
<td>COL_RESET</td>
</tr>
<tr>
<td>2</td>
<td>8</td>
<td>ROW_RESET</td>
</tr>
<tr>
<td>3</td>
<td>9</td>
<td>COL_CLK</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
<td>ROW_CLK</td>
</tr>
<tr>
<td>5</td>
<td>11</td>
<td>WCK</td>
</tr>
<tr>
<td>6</td>
<td>12</td>
<td>ST_CAL</td>
</tr>
<tr>
<td>7</td>
<td>13</td>
<td>REQ1</td>
</tr>
<tr>
<td>8</td>
<td>14</td>
<td>TRIGGER</td>
</tr>
<tr>
<td>9</td>
<td>15</td>
<td>RCKL</td>
</tr>
<tr>
<td>10</td>
<td>16</td>
<td>CLOCK</td>
</tr>
</tbody>
</table>

The outputs for signal monitoring are defined in the top level sheet of the firmware design and they can be assigned to any signal that is needed to be monitored. If however some signal in the sublevel sheets needs to be monitored, it has to be defined as an output in the sublevel sheet and the top level symbol of modified sublevel sheet has to be updated. Furthermore, the firmware design has to be implemented and the firmware on the CPLD has to be updated.