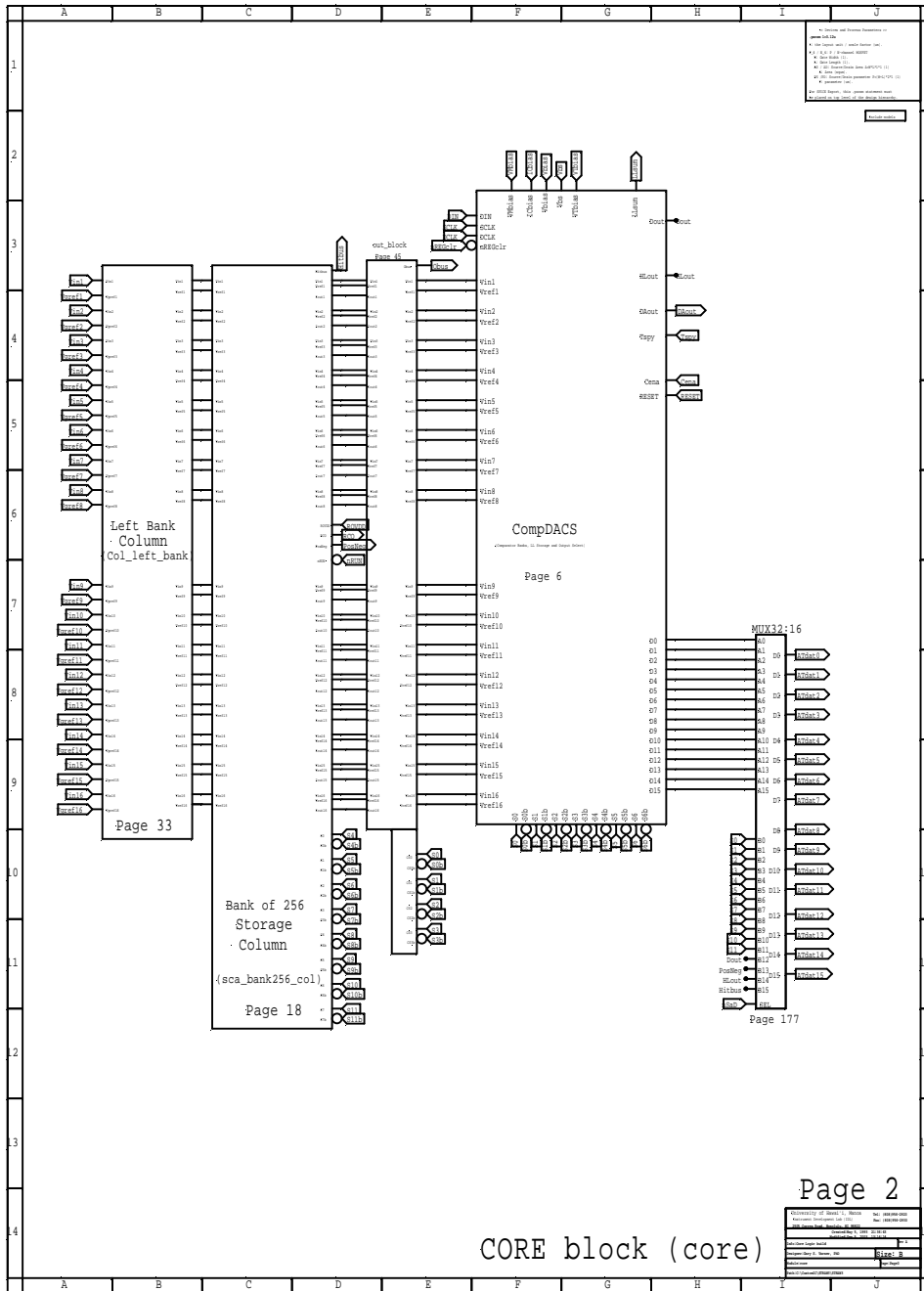


PadRing
Page 8

STRAW3

top
(top level sheet)
Page 1

STRAW3 Page 1



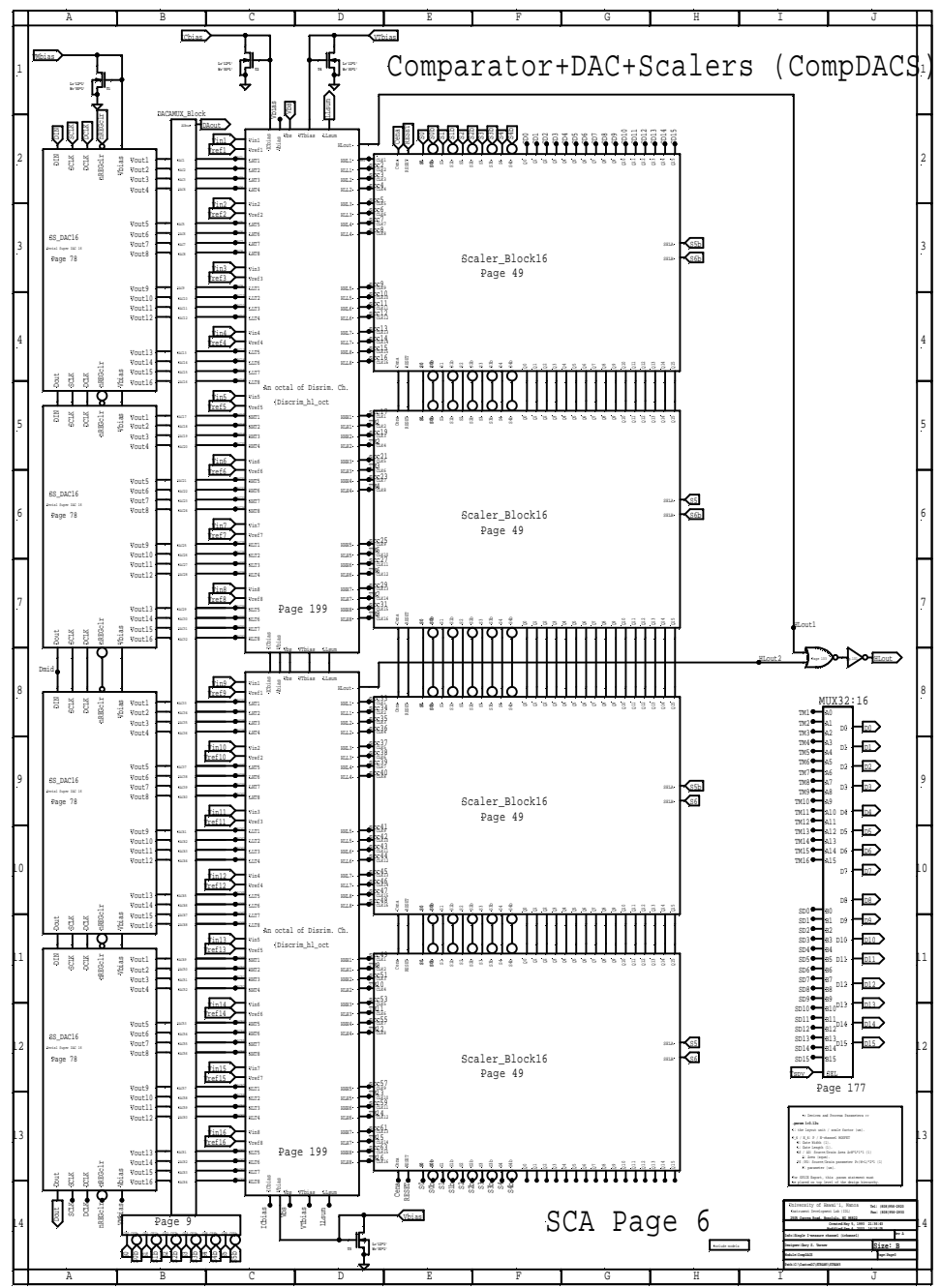
1. Data Bus and Control Buses
 2. Data Bus
 3. Control Bus
 4. Clock
 5. Reset
 6. Data Input
 7. Data Output
 8. Control Input
 9. Control Output
 10. Data Input/Output
 11. Control Input/Output

Page 2

CORE block (core)

Project Name	Project No.	Rev.
Project Path	Project Date	Project Status
Project Lead	Project Manager	Project Sponsor
Project Team	Project Budget	Project Risk
Project Start	Project End	Project Phase
Project Version	Project Release	Project Approval

Comparator+DAC+Scalers (CompDACS)

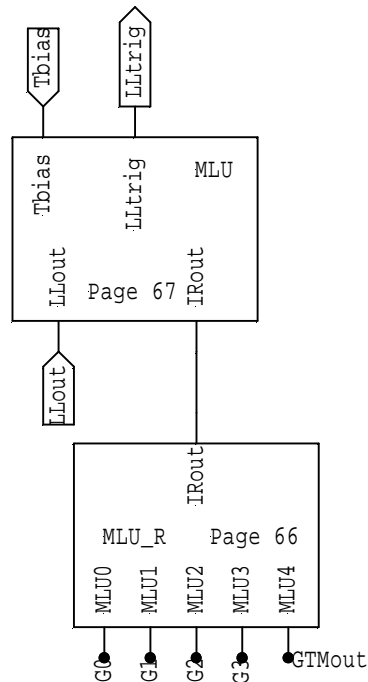


SCA Page 6

Legend:
 SR_DAC16: DAC16M04
 Scaler_Block16: Scaler16
 MUX32:16: MUX32:16
 DAC16M04: DAC16M04
 Scaler16: Scaler16
 MUX32:16: MUX32:16

Component	Page
SR_DAC16	78
Scaler_Block16	49
MUX32:16	177
DAC16M04	16
Scaler16	16
MUX32:16	16

Majority Logic Unit (MLU) Block

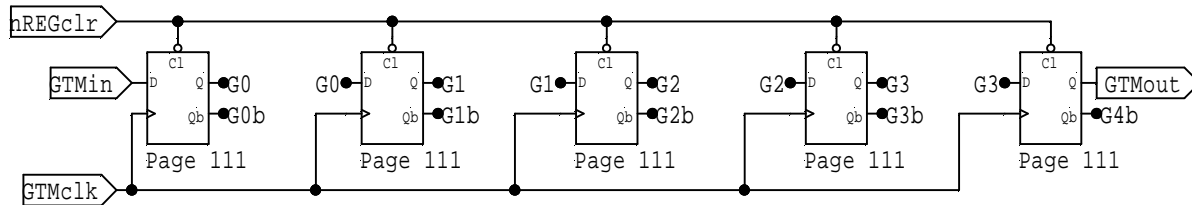


```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (1).
L: Gate Length (1).
AS / AD: Source/Drain Area A=W*L*1*1 (1)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W*L)*2*1 (1)
P: parameter (um).

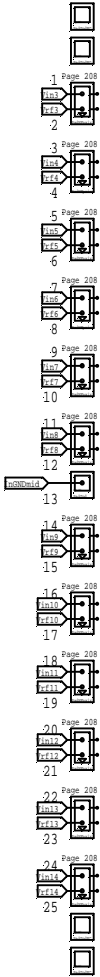
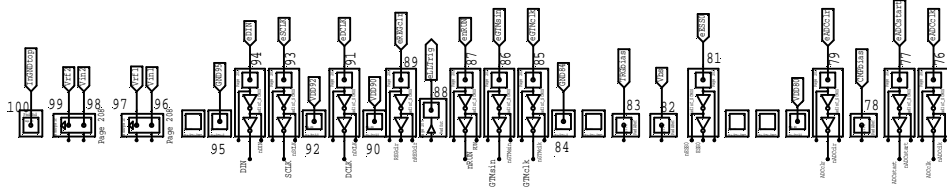
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

Include models



STRAW3 Page 7

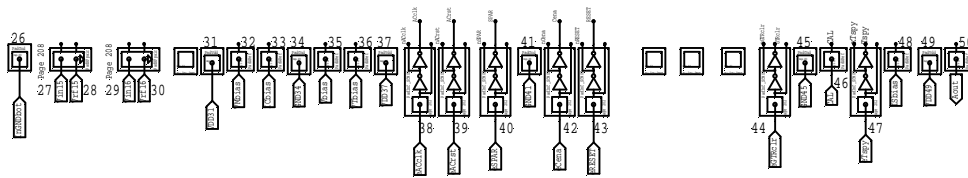
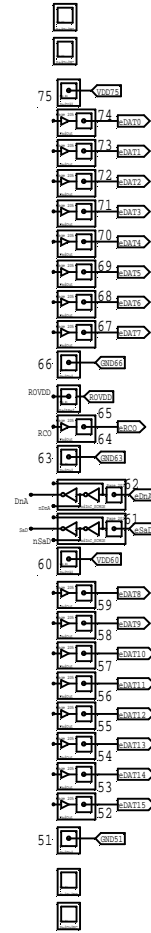
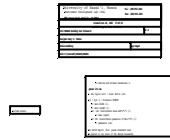
University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43	Size: 5x7		
Modified: Sep 4, 2003 11:20:25	Rev A		
Info: MLU Trigger			
Designer: Gary S. Varner, PhD			
Module: MLU_block		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			



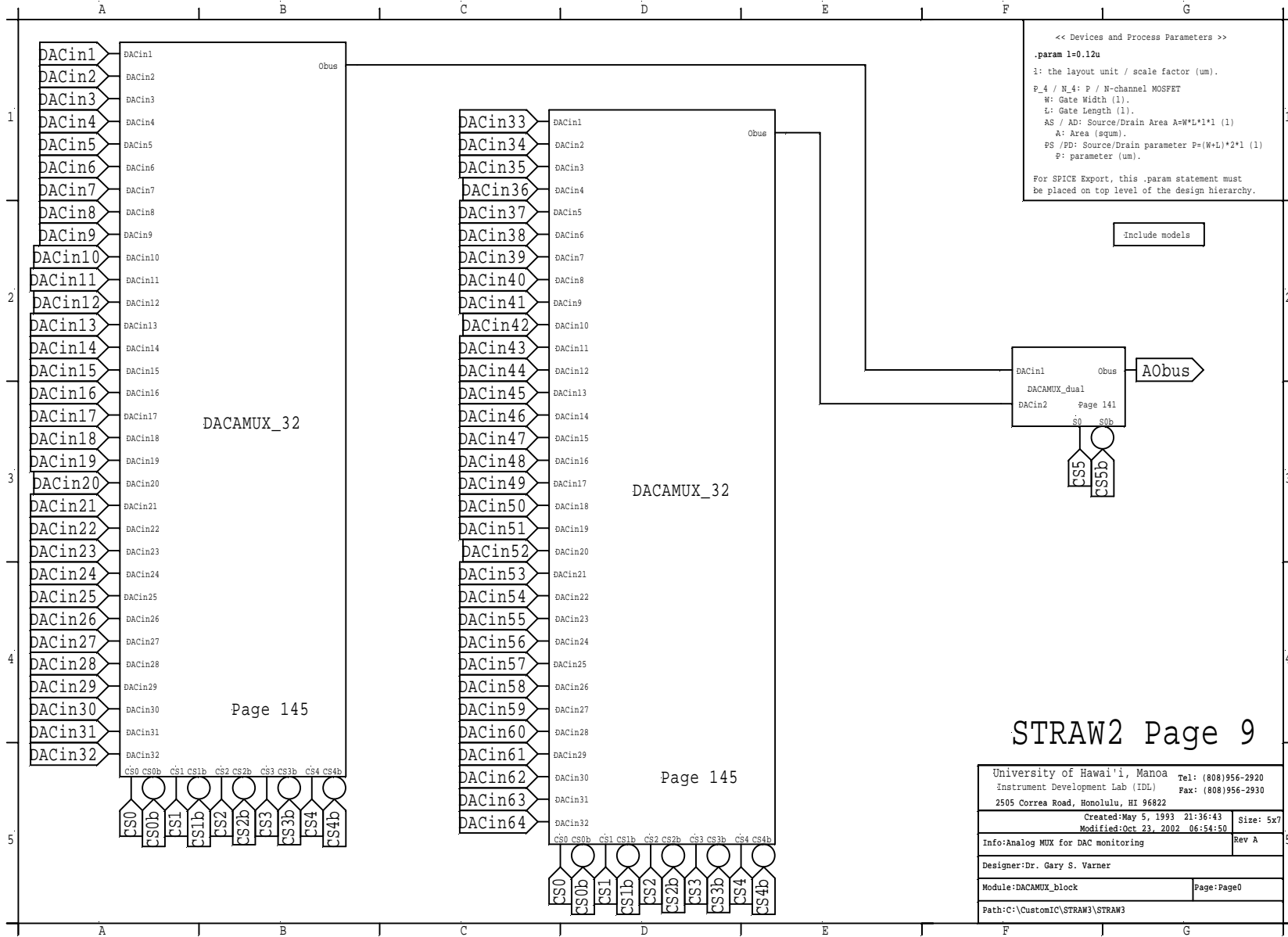
STRAW2 PadRing

(Pad Ring definition)

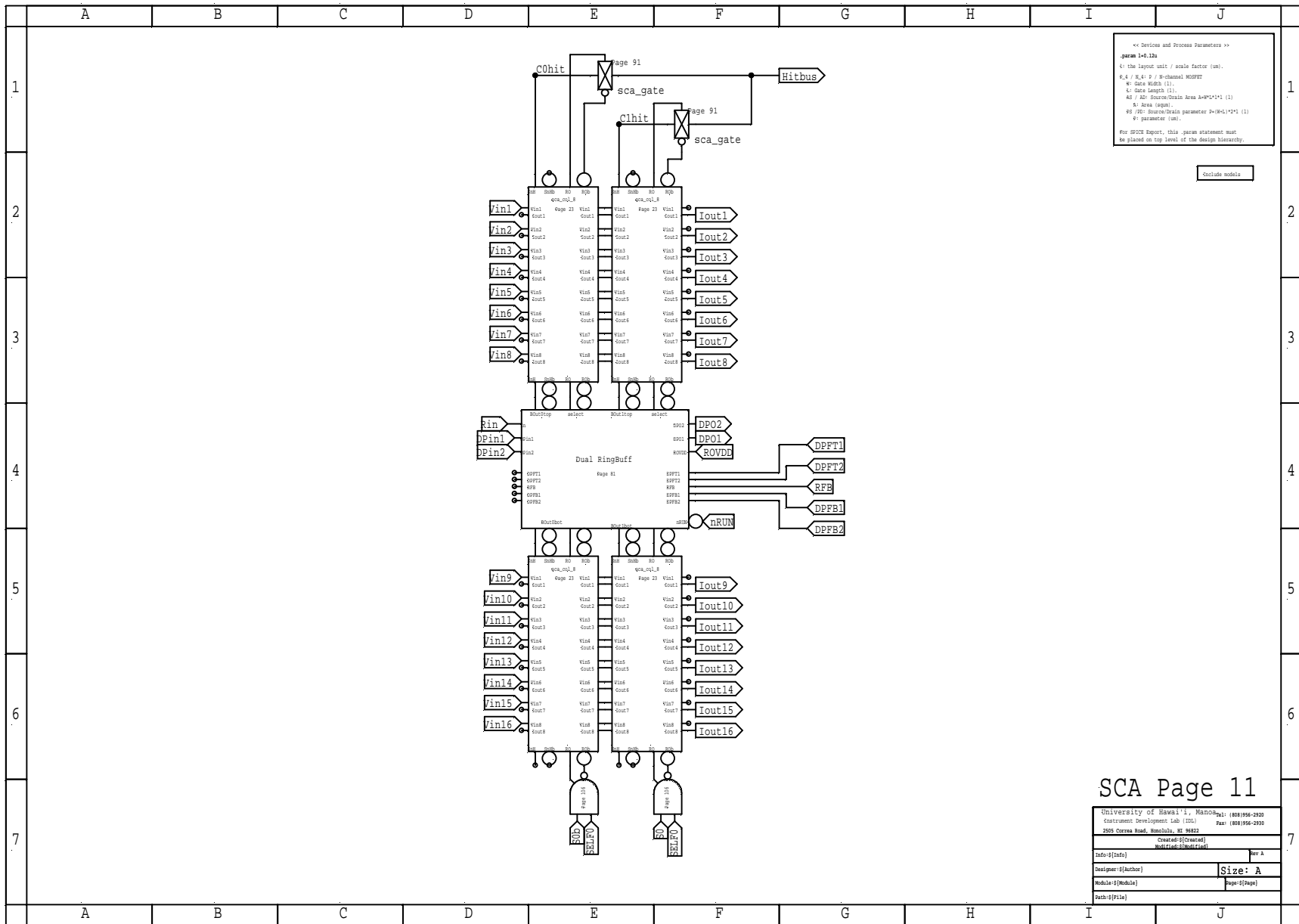
Page 8



DAC Analog Mux Block [64-Ch.] (DACAMUX_Block)



SCA Dual Column (sca_dual_col)



```

<< Devices and Process Parameters >>
.param 1=0.125
!< the layout unit / scale factor (um).
!< Gate Width (1).
!< Gate Length (1).
!< Ad / Ad' Source/Drain Area 3=PM1*1*1 (1)
!< Area (squm).
!< Ad / Ad' Source/Drain parameter 3=(W1)*L1 (1)
!< Parameter List.
    
```

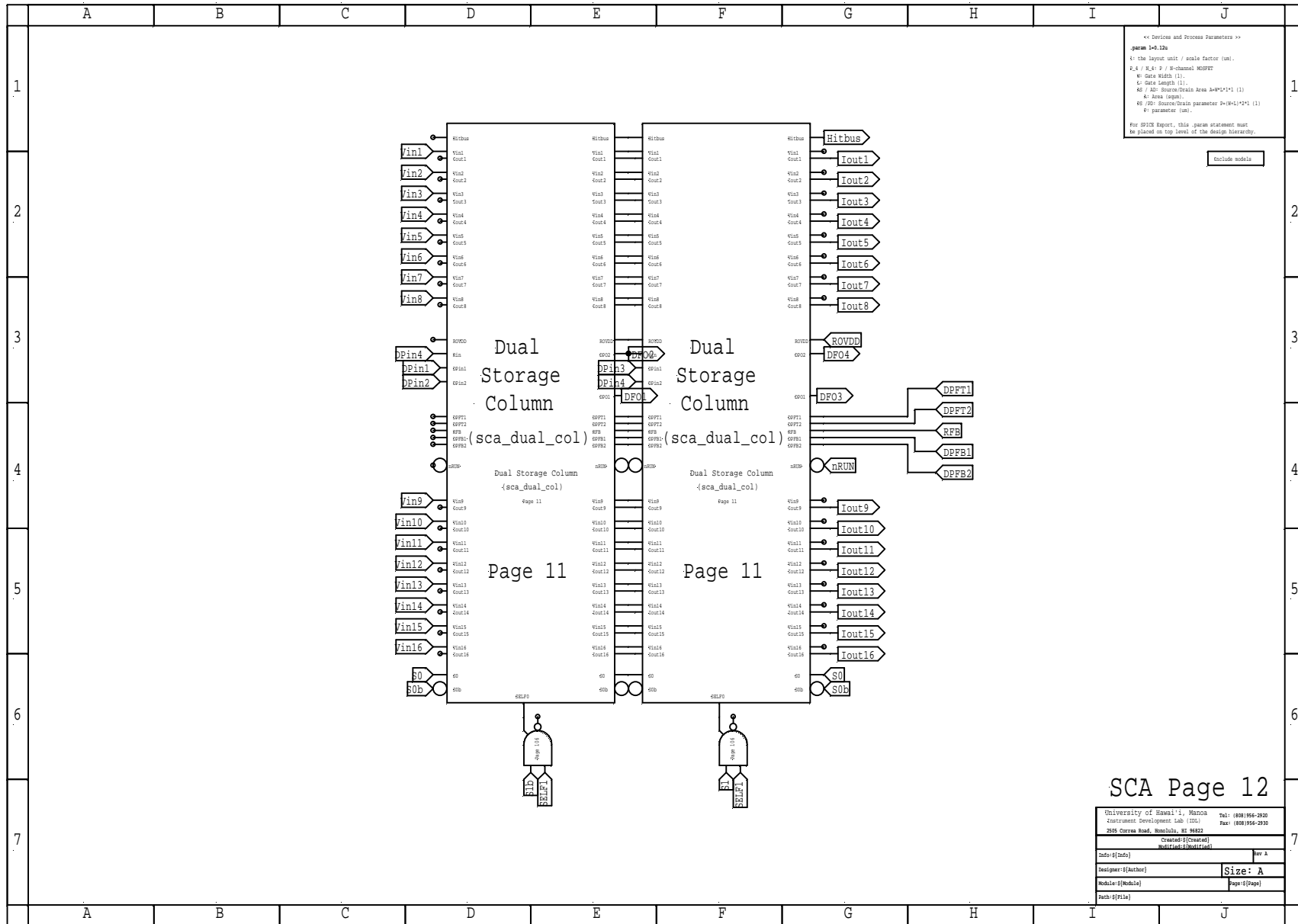
For SPICE Report, this param statement must be placed on top level of the design hierarchy.

Include models

SCA Page 11

University of Hawaii, Manoa		Tel: (808)956-2920	
Continuum Development Lab (CDL)		Fax: (808)956-2930	
2055 Correa Road, Honolulu, HI 96822			
Created: [Created]		Rev: A	
Info: [Info]		Module: [Module]	
Designer: [Author]		Size: A	
Date: [Date]		Page: [Page]	
Path: [Path]			

SCA Quad Column (sca_quad_col)



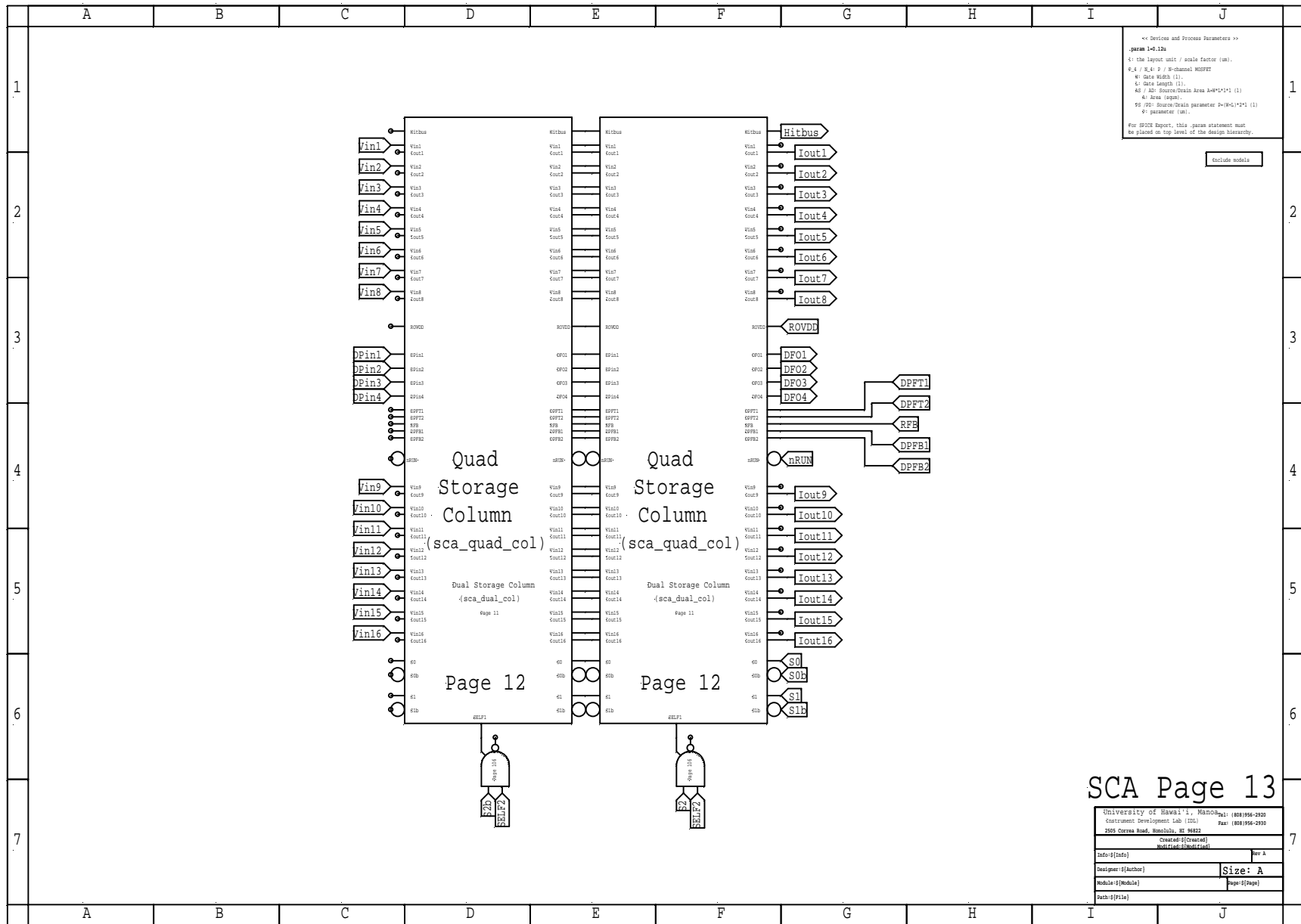
<< Devices and Process Parameters >>
 .param 1=0.125
 1: the layout unit / scale factor (um).
 2,4: #_A_# 2 / #_B-channel WIDTH
 #_B: Data Width (1).
 4: Data Length (1).
 44: #_A#: Storage/Train Area 3=4*#_A_#*1 (1)
 #_A: Area (squm).
 45: #_B#: Storage/Train parameter 2=(#_A_#)*#_B_#*1 (1)
 #_B: parameter (um).
 For SVCS Report, this .param statement must be placed on top level of the design hierarchy.

Include models

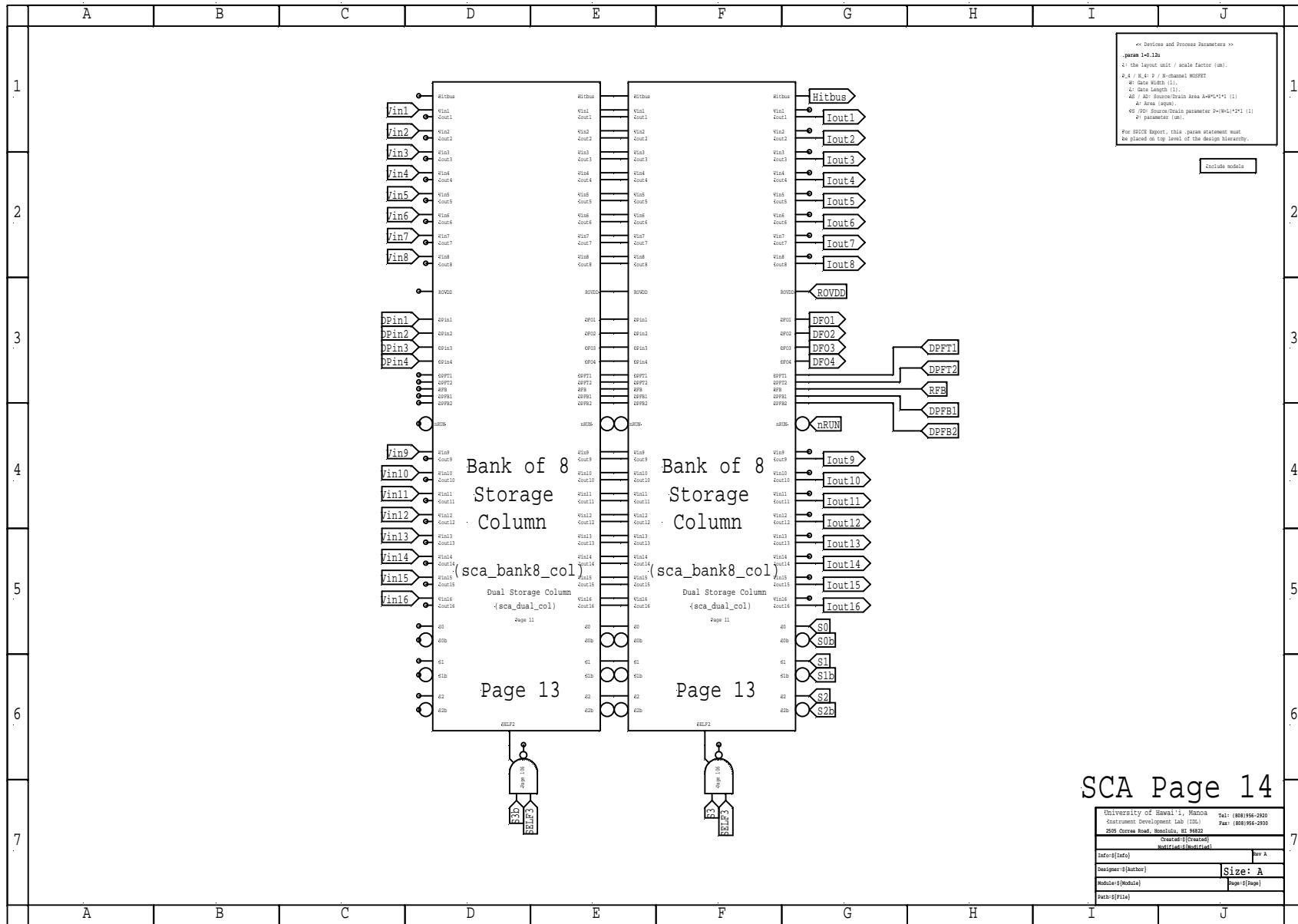
SCA Page 12

University of Hawaii '1, Manoa		Tel: (808) 956-2920	
Instrument Development Lab (IDL)		Fax: (808) 956-2930	
2525 Correa Road, Honolulu, HI 96822			
Created: 5/1/2004		Rev: A	
Info: 1 (Info)			
Designer: J (Author)	Size: A		
Module: F (Module)	Page: 2 (Page)		
Part: 1 (Part)			

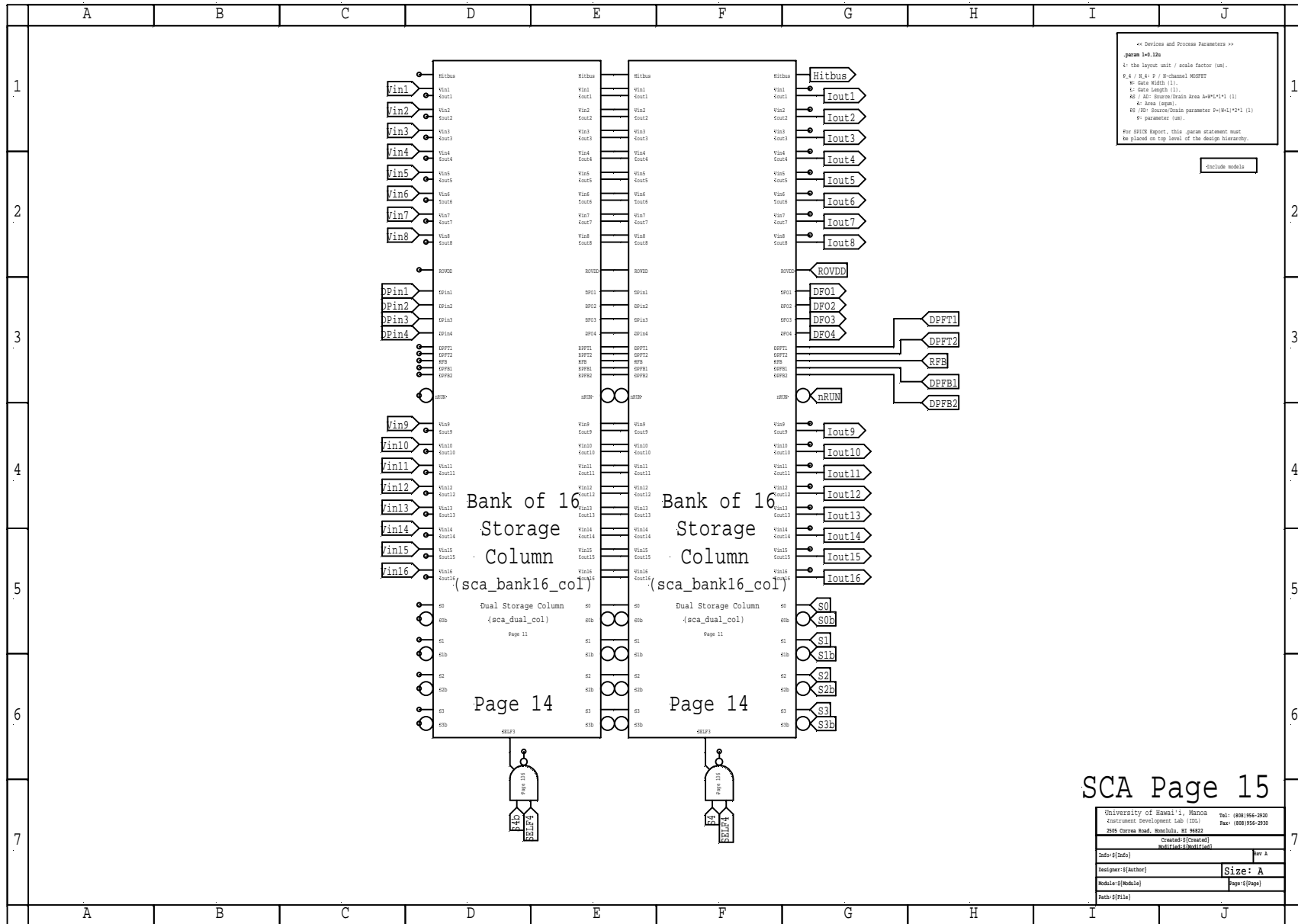
SCA Bank of 8 Column (sca_bank8_col)



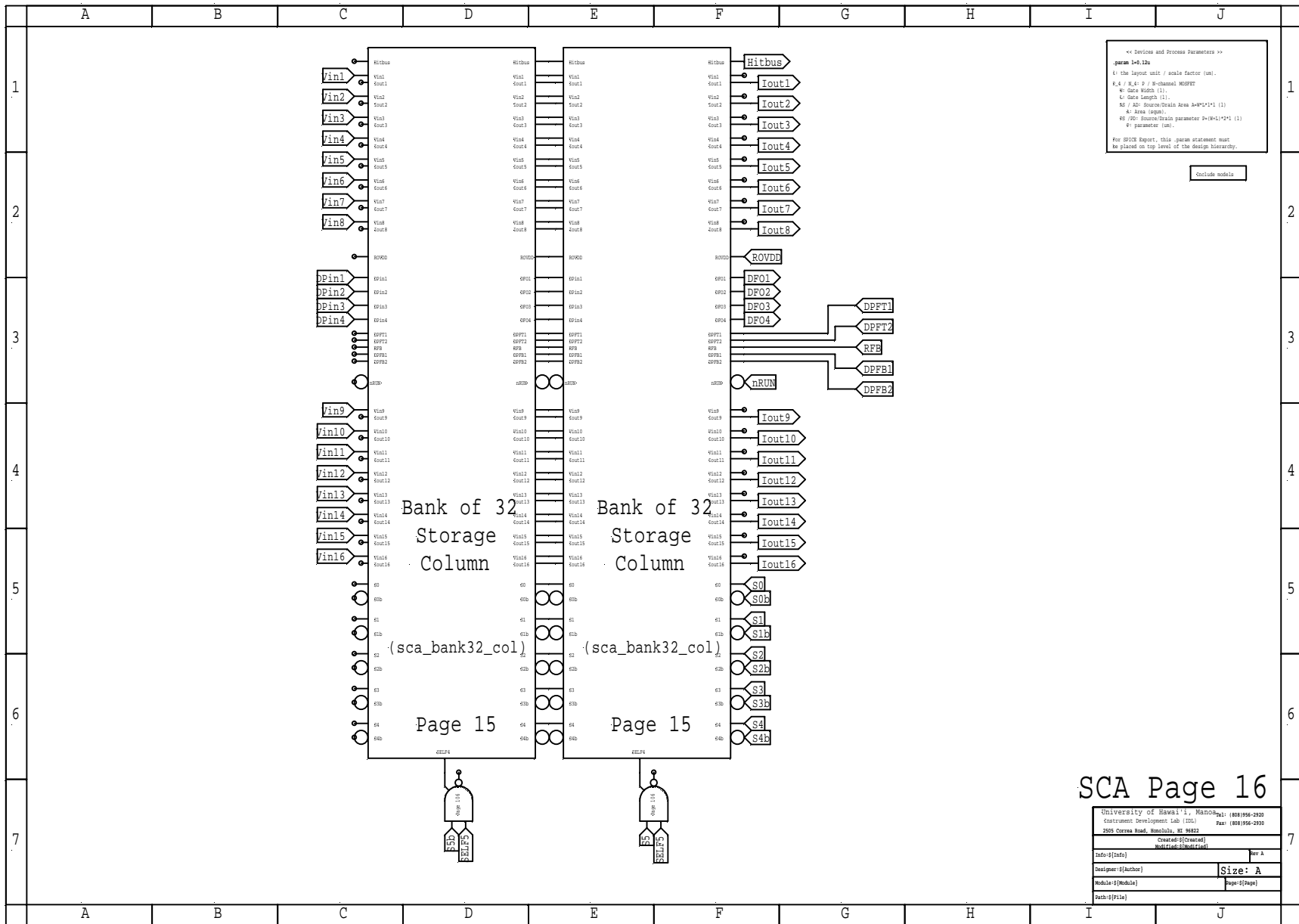
SCA Bank of 16 Column (sca_bank16_col)



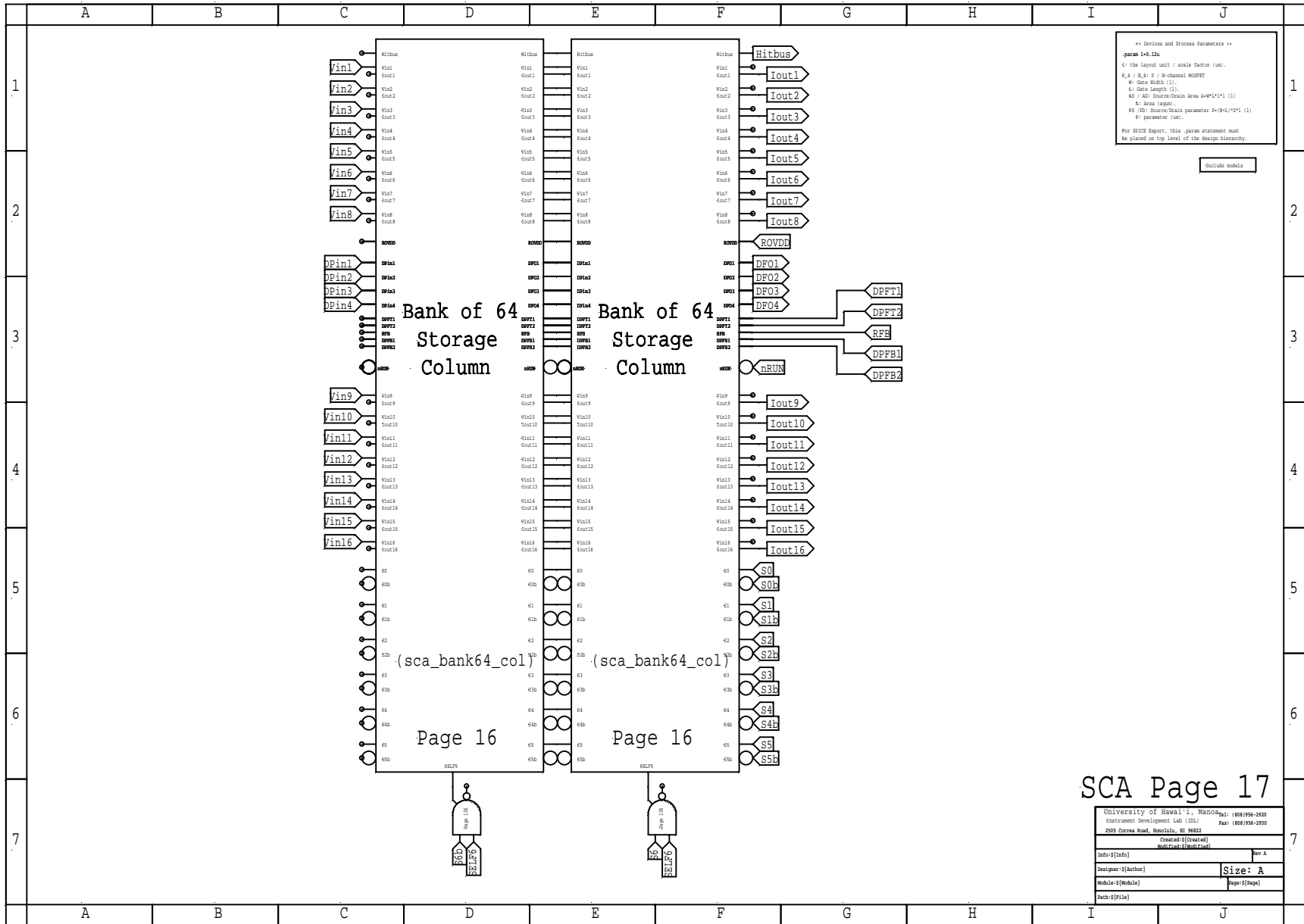
SCA Bank of 32 Column (sca_bank32_col)



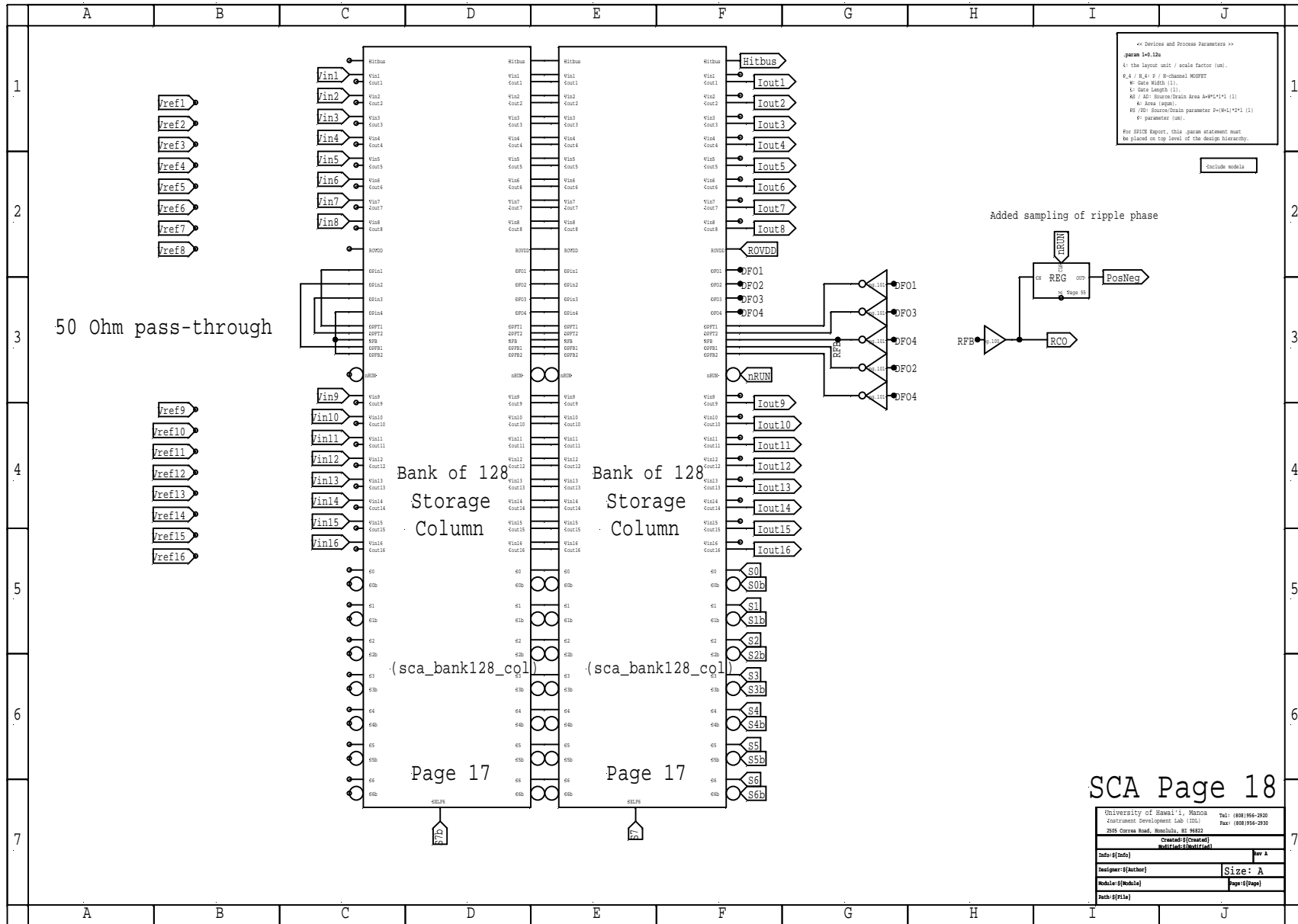
SCA Bank of 64 Column (sca_bank64_col)



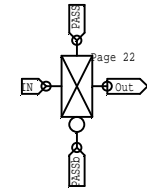
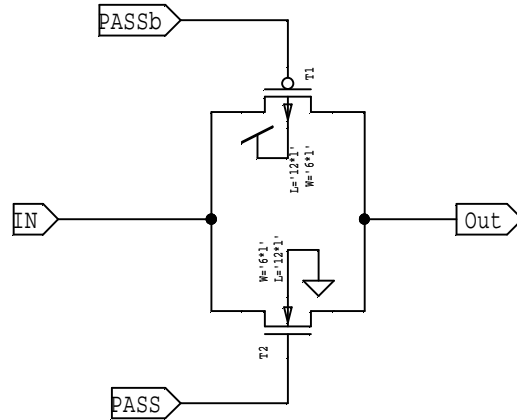
SCA Bank of 128 Column (sca_bank128_col)



SCA Bank of 256 Column (sca_bank256_col)



Big Pass Transistor (big_passt)



[NETTRAN OUTPUT=<# SCMOS_NOR2 %[A] %[B] %]{Out}]

```
<< Devices and Process Parameters >>
.param l=0.12u
i: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).
```

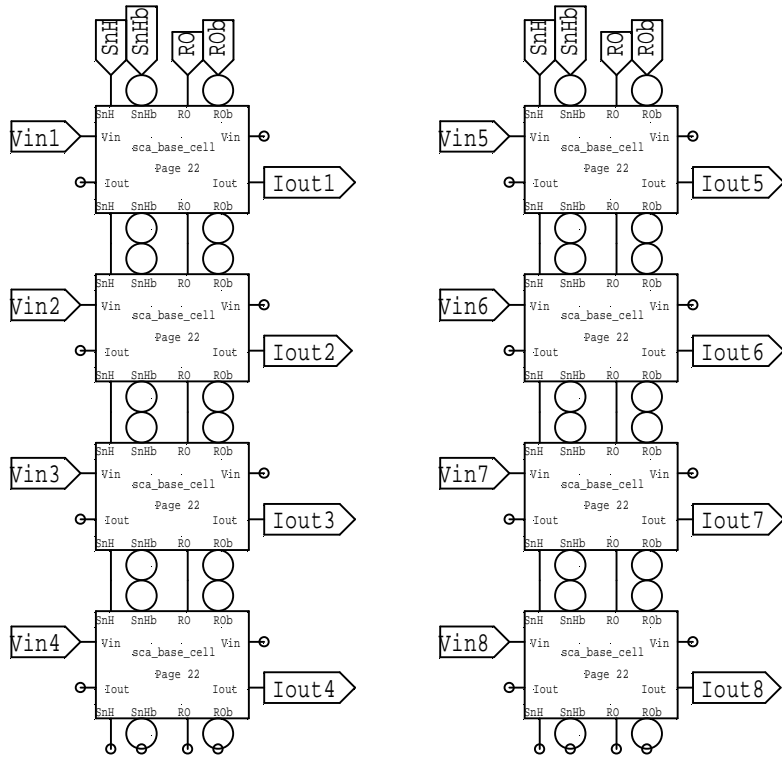
For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

Include models

Page 22

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993	21:36:43	Size: 5x7	
Modified: Oct 23, 2002	08:27:57	Rev A	
Info: Big Pass Transistor for mirror select			
Designer: Gary S. Varner			
Module: big_passt		Page: Page0	
Path: C:\CustomTC\STRAW2\straw2_23oct02			

SCA Half_column of 8 (sca_col_8)



```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*l (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*l (l)
P: parameter (um).

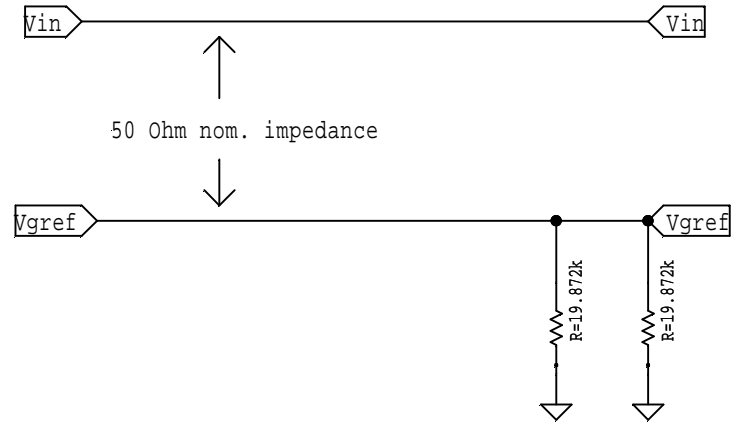
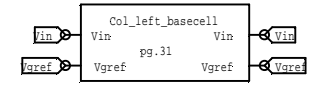
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

SCA Page 23

University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created: \${Created}	Size: 5x7
Modified: \${Modified}	Rev A
Info: \${Info}	
Designer: \${Author}	
Module: \${Module}	Page: \${Page}
Path: \${File}	

Include models

Column Left Basecell (Col_left_basecell)



n.c. pulldown/shutdown and input protect

Include models

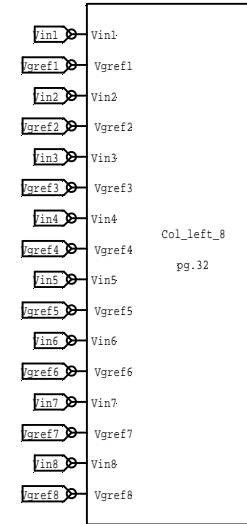
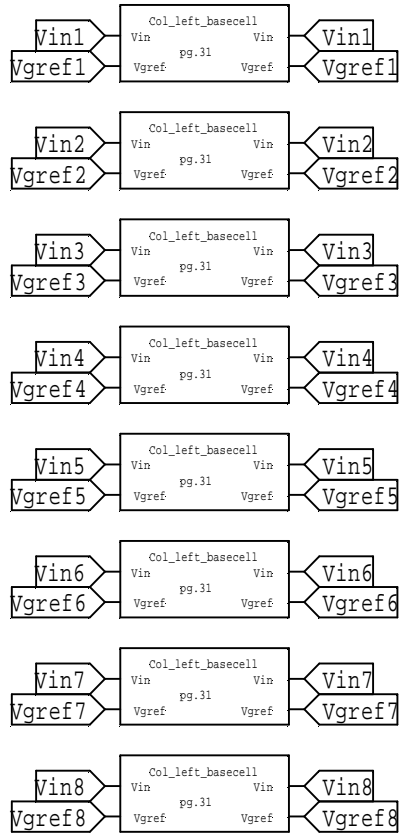
```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:41		Size: 5x7	
Modified: Sep 24, 2002 13:26:02		Rev A	
Info: Input cell left col			
Designer: Dr. Gary S. Varner			
Module: Col_left_basecell		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

Bank of 8 Col Left cells (Col_left_8)



Pass-through Trigger signals are No Connect

```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

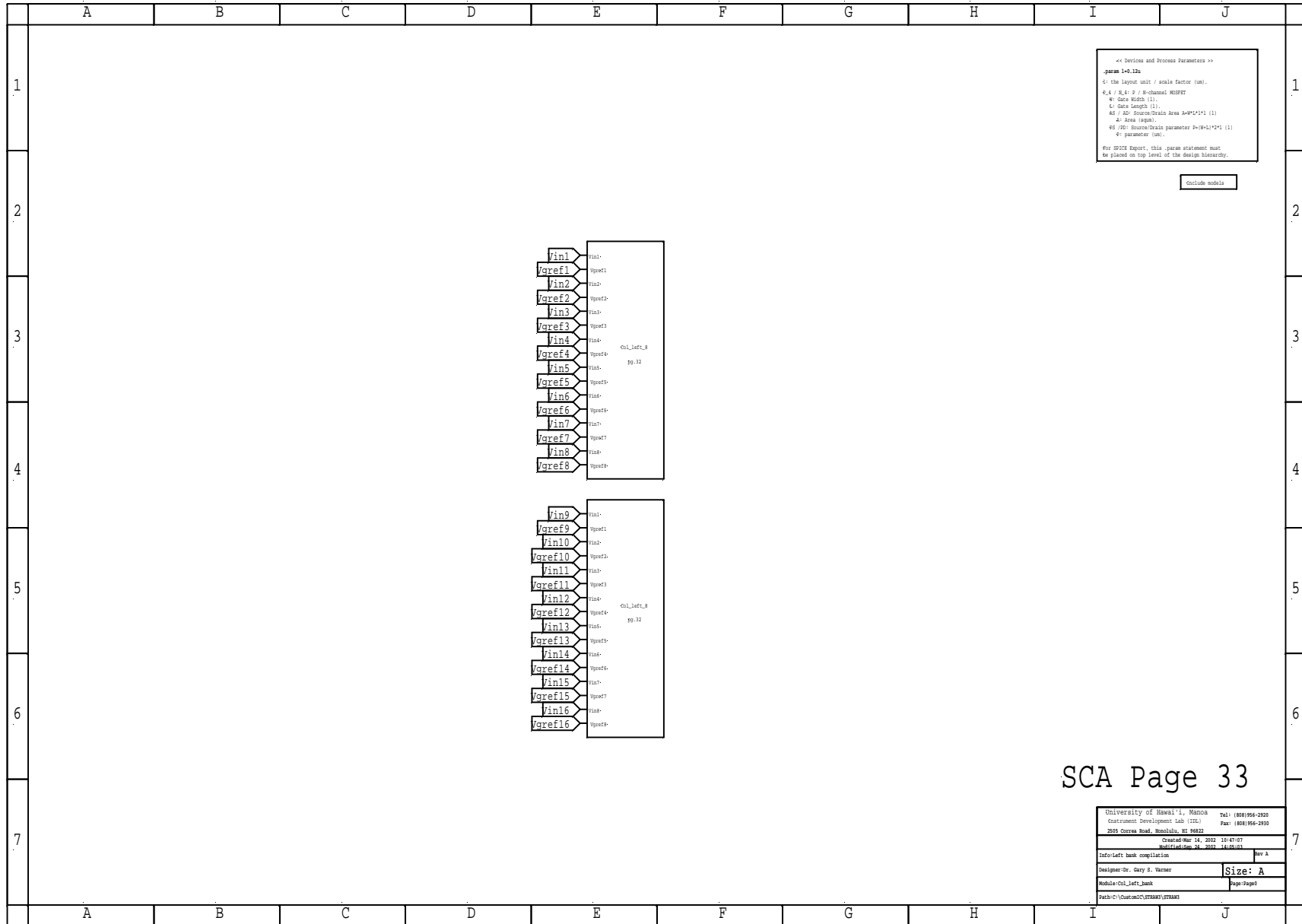
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

Include models

SCA Page 32

University of Hawai'i, Manoa		tel: (808)956-2920
Instrument Development Lab (IDL)		Fax: (808)956-2930
2505 Correa Road, Honolulu, HI 96822		
Created: May 5, 1993 21:36:41	Size: 5x7	
Modified: Oct 23, 2002 05:28:06	Rev A	
Info: Left input cells		
Designer: Dr. Gary S. Varner		
Module: Col_left_8	Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3		

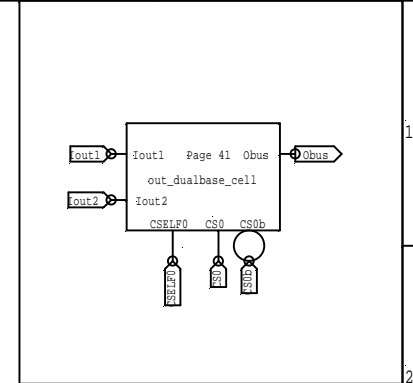
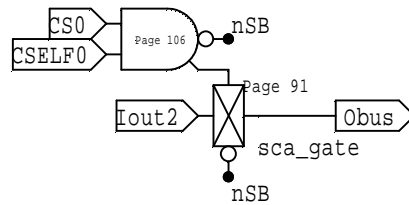
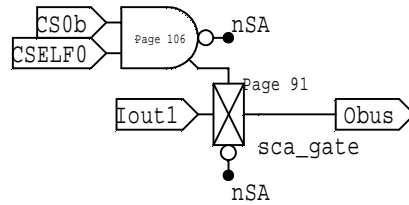
Left Bank (Col_left_bank)



SCA Page 33

UNIVERSITY of Hawaii, MANOA		Tel: (808)956-2929	
Government Development Lab (121)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created Mar 14, 2012 10:47:07			
Modified Sep 24, 2012 14:26:51			
Info: Left bank compilation		Rev A	
Designer: Dr. Gary S. Warner		Size: A	
Module: Col_left_bank		Page: 3/40	
Path: C:\Users\gswarner\Documents\SPICE			

Output Dual Base Cell (out_dualbase_cell)



<< Devices and Process Parameters >>

```
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).
```

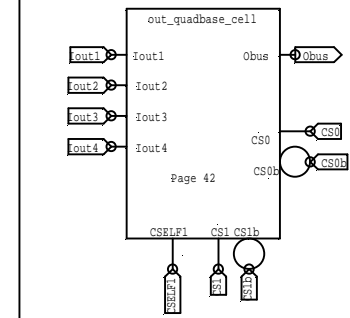
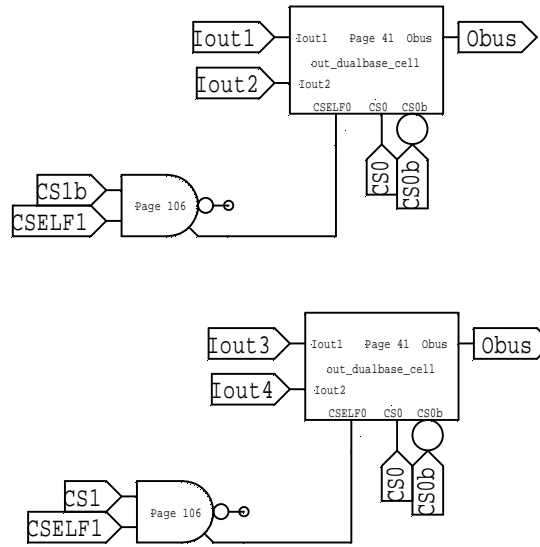
For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

include models

SCA Page 41

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43		Size: 5x7	
Modified: Oct 14, 2002 08:57:20		Rev A	
Info: A/M 12-bit Bus select			
Designer: Dr. Gary S. Varner			
Module: out_dualbase_cell		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

Output Quad Base Cell (out_quadbase_cell)



SCA Page 42

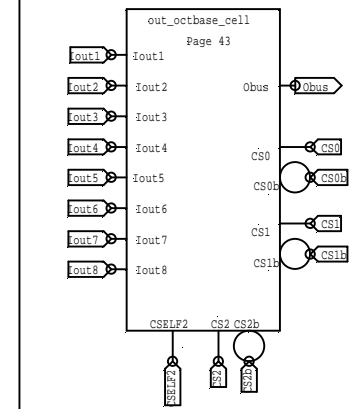
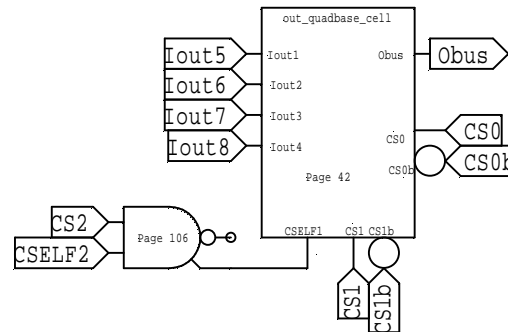
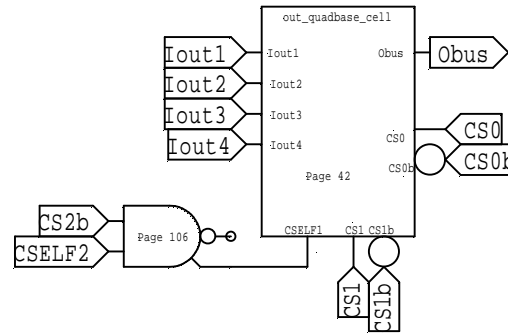
```
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
```

include models

University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created: May 5, 1993 21:36:43	Size: 5x7
Modified: Sep 23, 2002 16:05:45	Rev A
Info: A/M 12-bit Bus select	
Designer: Dr. Gary S. Varner	
Module: out_quadbase_cell	Page: Page0
Path: C:\CustomIC\STRAW3\STRAW3	

Output Octal Base Cell (out_octbase_cell)



<< Devices and Process Parameters >>

```
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).
```

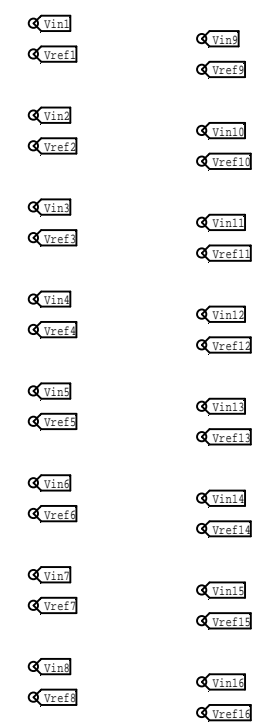
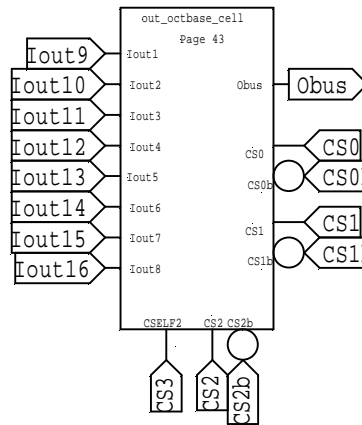
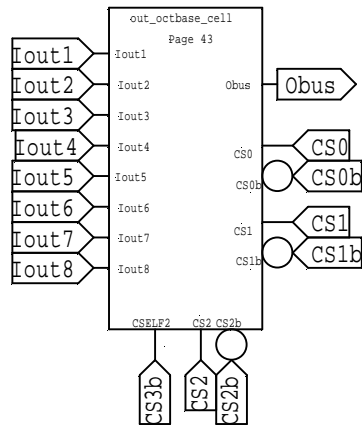
For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

include models

SCA Page 43

University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created: May 5, 1993 21:36:43	Size: 5x7
Modified: Sep 23, 2002 16:05:06	Rev A
Info: A/M 12-bit Bus select	
Designer: Dr. Gary S. Varner	
Module: out_octbase_cell	Page: Page0
Path: C:\CustomIC\STRAW3\STRAW3	

Output Block w/Select (out_block)



Pass through signals

<< Devices and Process Parameters >>

```
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).
```

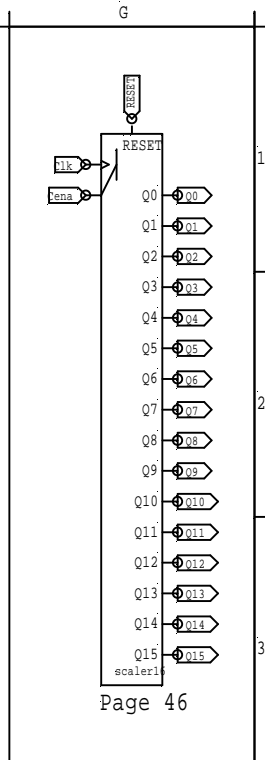
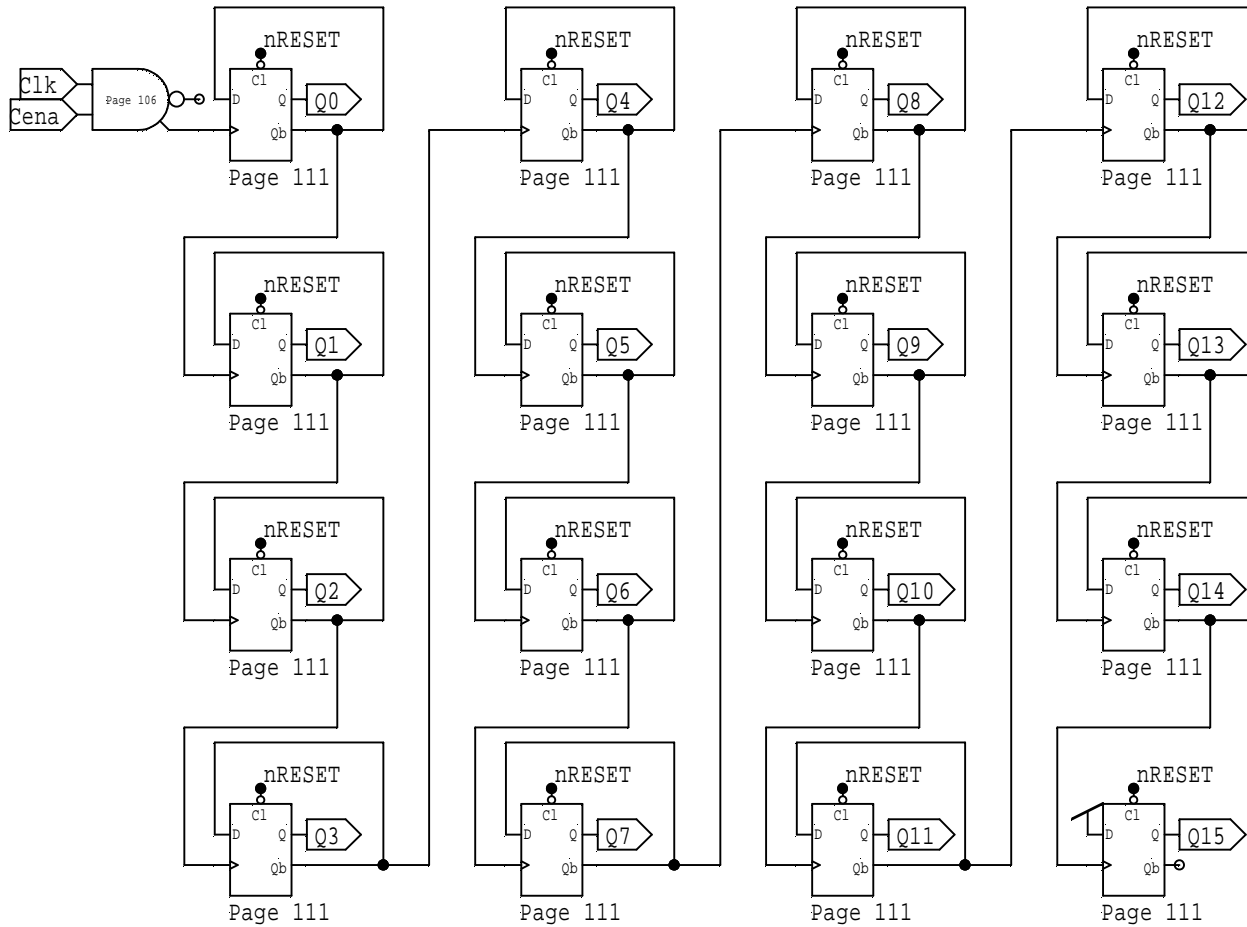
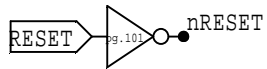
For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

include models

SCA Page 45

University of Hawai'i, Manoa		tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43		Size: 5x7	
Modified: Sep 1, 2003 10:20:51		Rev A	
Info: A/M 12-bit Bus select			Rev A
Designer: Dr. Gary S. Varner			
Module: out_block		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

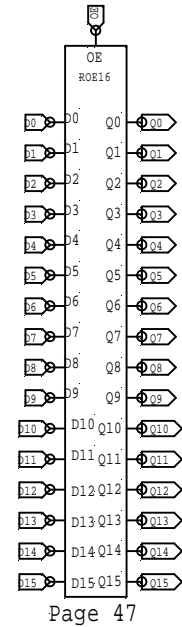
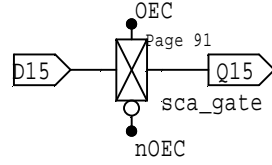
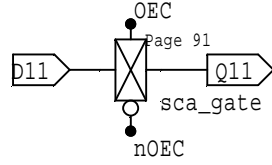
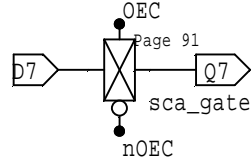
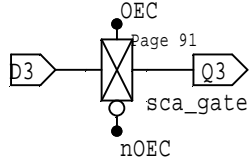
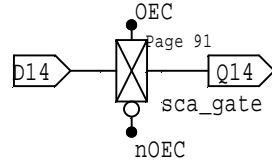
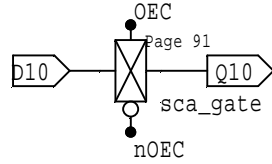
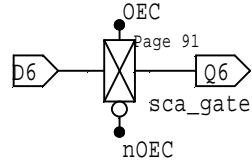
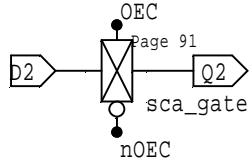
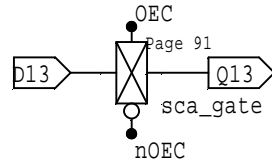
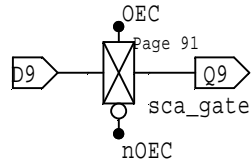
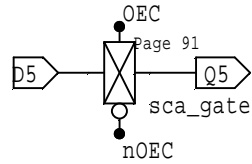
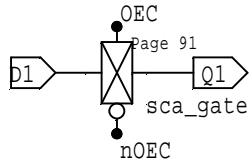
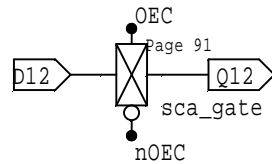
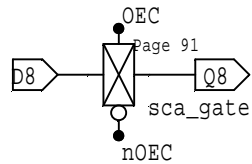
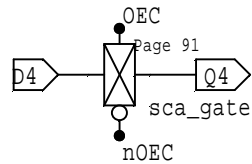
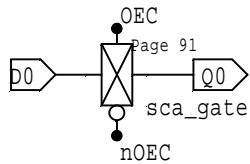
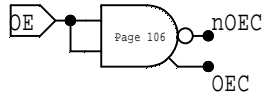
16-bit scaler [15+overflow bit] (scaler16)



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University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created:\$(Created)	Size: 5x7
Modified:\$(Modified)	Rev A
Info:\$(Info)	
Designer:\$(Author)	
Module:\$(Module)	Page:\$(Page)
Path:\$(File)	

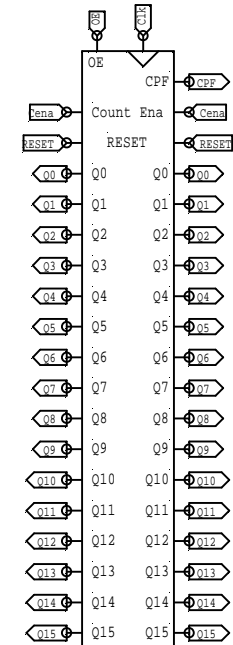
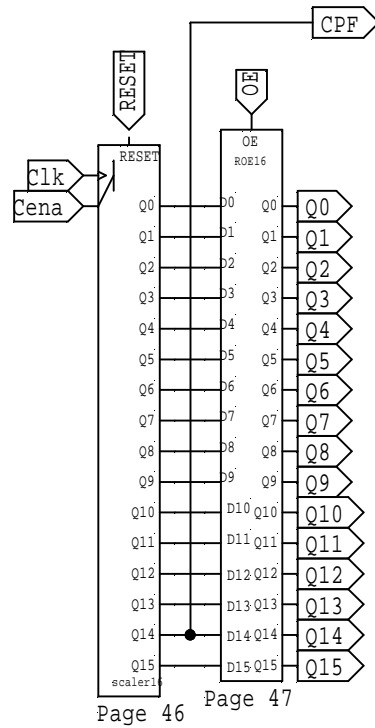
Register Output Enable [16-bit reg] (ROE16)



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University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created:\$(Created)	Size: 5x7
Modified:\$(Modified)	Rev A
Info:\$(Info)	
Designer:\$(Author)	
Module:\$(Module)	Page:\$(Page)
Path:\$(File)	

16-bit Scaler+Output Enable (Scaler_Block)

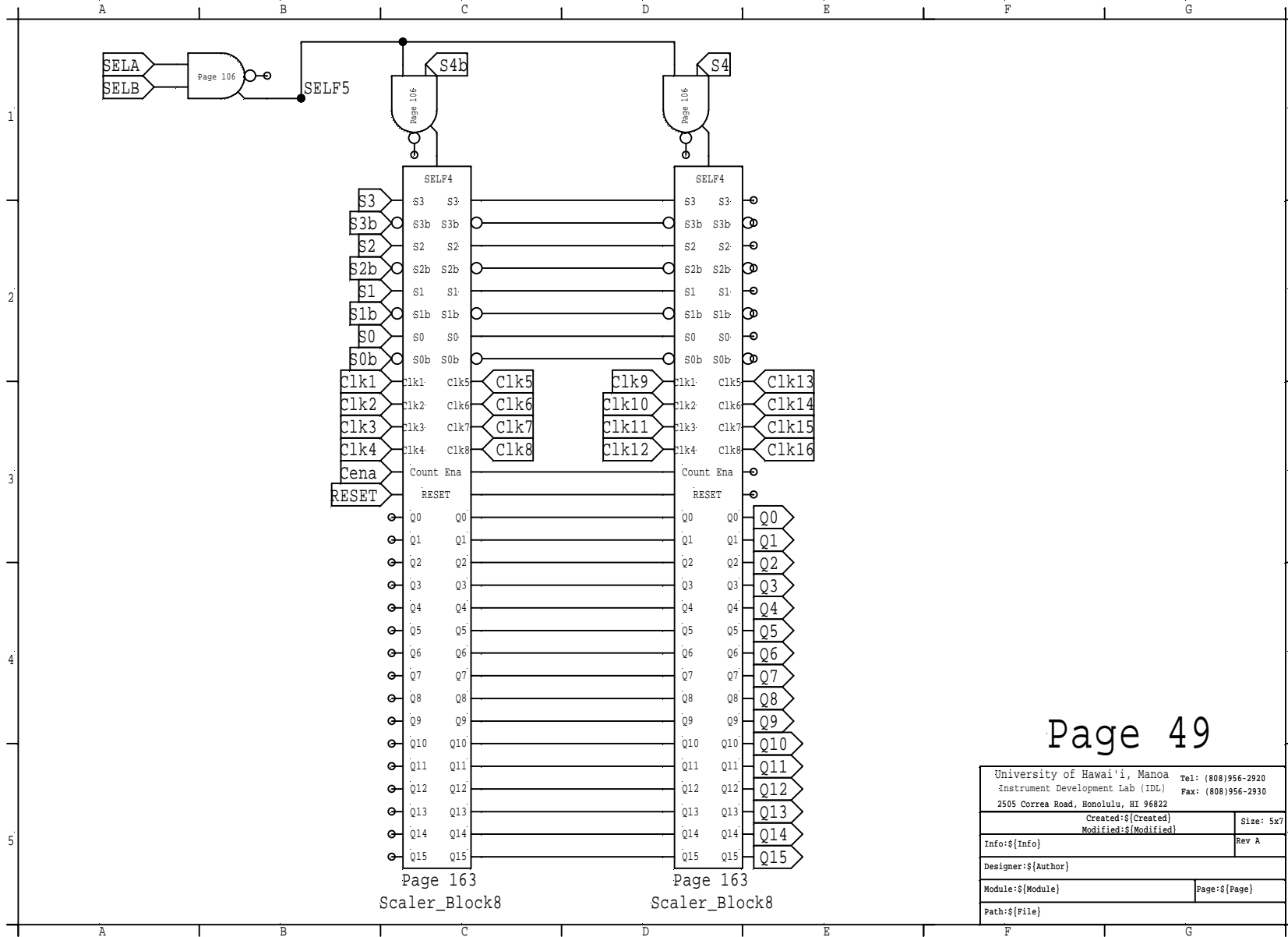


Page 48
Scaler_Block

Page 48

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: \${Created}		Size: 5x7	
Modified: \${Modified}		Rev A	
Info: \${Info}			
Designer: \${Author}			
Module: \${Module}		Page: \${Page}	
Path: \${File}			

Block of 16 Scalers (Scaler_Block16)



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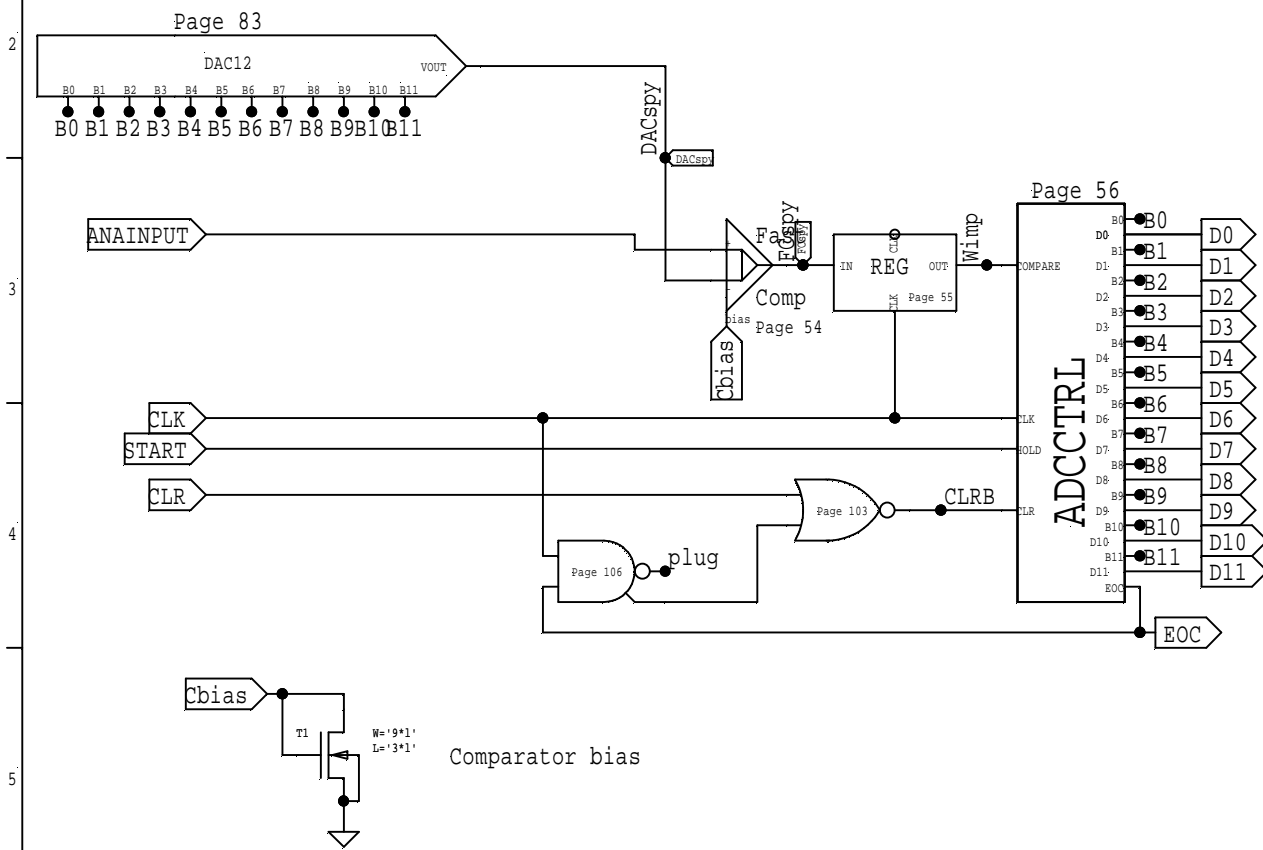
University of Hawai'i, Manoa		Tel: (808)956-2920
Instrument Development Lab (IDL)		Fax: (808)956-2930
2505 Correa Road, Honolulu, HI 96822		
Created: \${Created}		Size: 5x7
Modified: \${Modified}		Rev A
Info: \${Info}		
Designer: \${Author}		
Module: \${Module}		Page: \${Page}
Path: \${File}		

ADC12

```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*l*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```



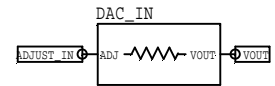
Include models

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University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: Nov 3, 1999 09:33:45	Size: 5x7		
Modified: Sep 6, 2003 11:12:23	Rev A		
Info: 12-bit Successive Approximation ADC			
Designer: Gary S. Varner			
Module: ADC12		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

A B C D E F G

1

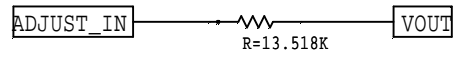


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(DAC_IN)

2

3



4

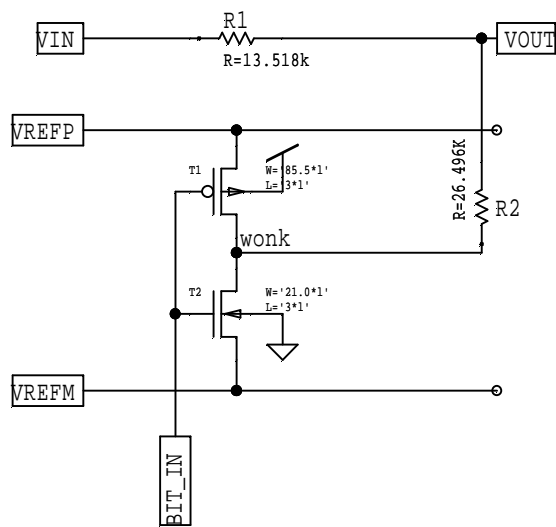
Page 52

5

University of Hawai'i, Manoa		tel: (808)956-2920
Instrument Development Lab (IDL)		Fax: (808)956-2930
2505 Correa Road, Honolulu, HI 96822		
Created: Aug 25, 1995 10:21:16	Size: 5x7	
Modified: Nov 1, 2002 05:55:47	Rev A	
Info: DAC trim		
Designer: Gary S. Varner		
Module: DAC_IN		Page: Page0
Path: C:\CustomIC\STRAW3\STRAW3		

A B C D E F G

DAC_BIT

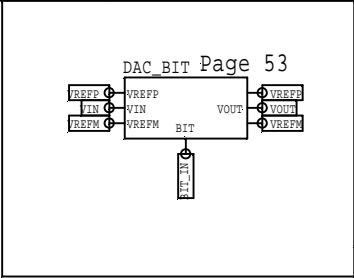


Include models

```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```



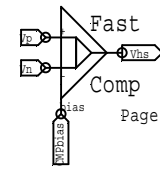
University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created: Aug 25, 1995 10:33:23	Size: 5x7
Modified: Sep 2, 2003 18:49:50	Rev A
Info: R-2R DAC bit	
Designer: Gary S. Varner	
Module: DAC_BIT	Page: Page0
Path: C:\CustomIC\STRAW3\STRAW3	

Two-stage Fast Comparator (Comparator2)

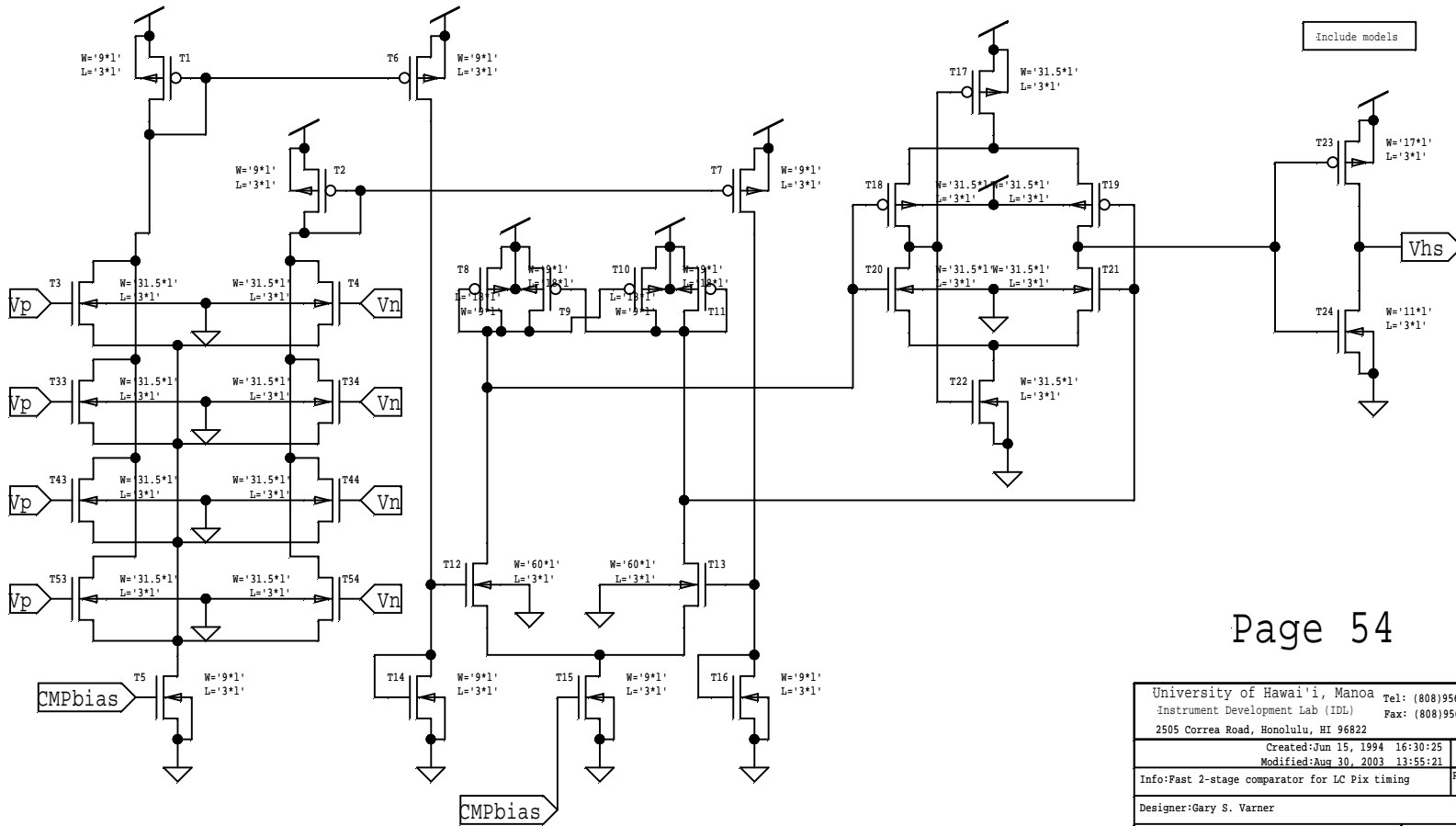
```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```



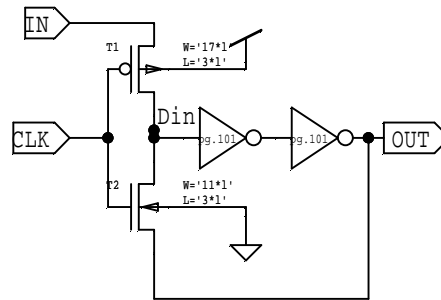
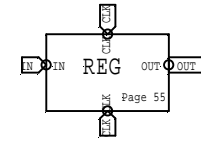
Page 54



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University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: Jun 15, 1994 16:30:25	Size: 5x7		
Modified: Aug 30, 2003 13:55:21	Rev A		
Info: Fast 2-stage comparator for LC Pix timing			
Designer: Gary S. Varner			
Module: Comparator2		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

REG



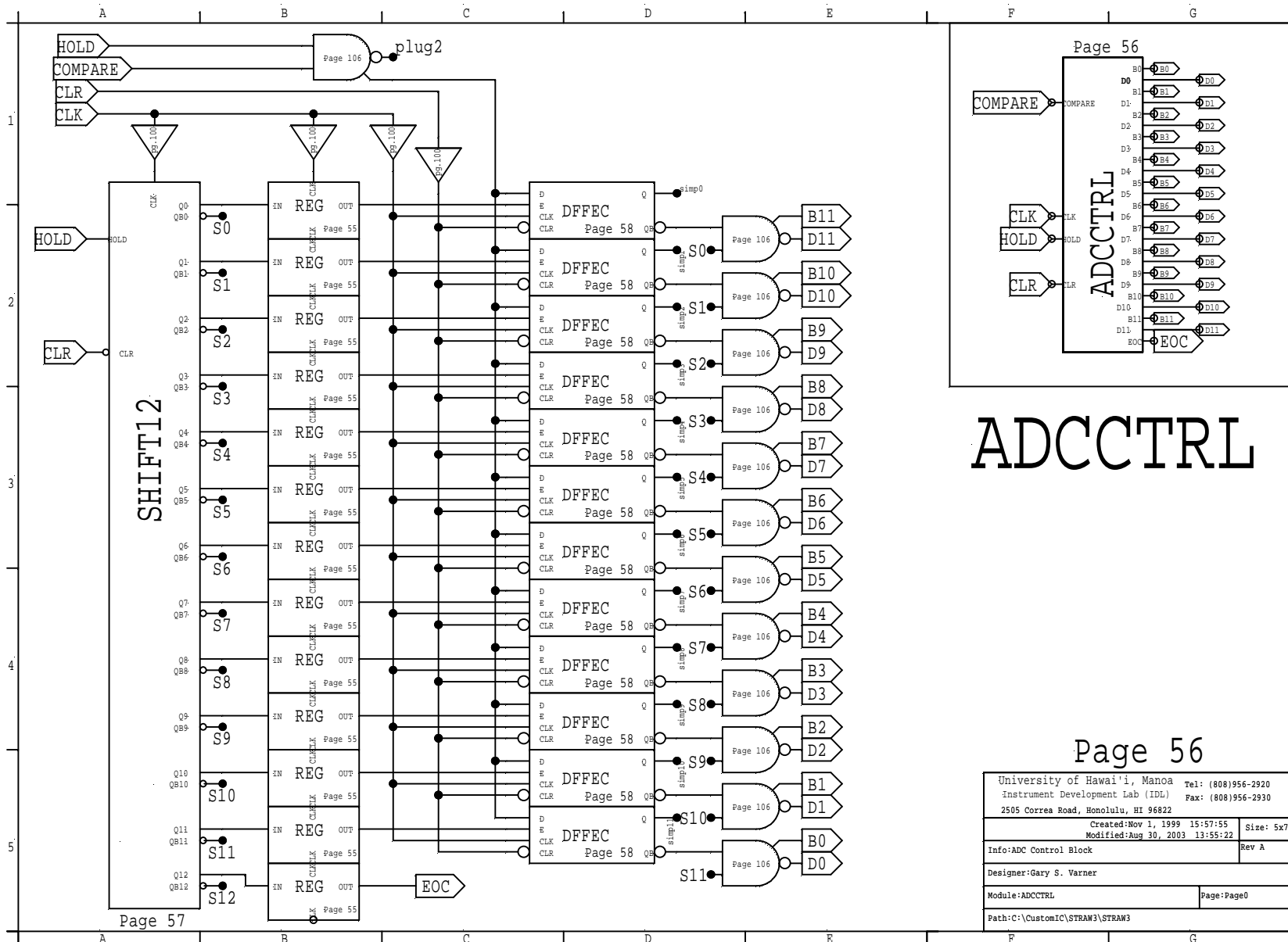
Include models

```
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l)
L: Gate Length (l)
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
```

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University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created:\${Created}		Size: 5x7	
Modified:\${Modified}		Rev A	
Info:\${Info}			
Designer:\${Author}			
Module:\${Module}		Page:\${Page}	
Path:\${File}			

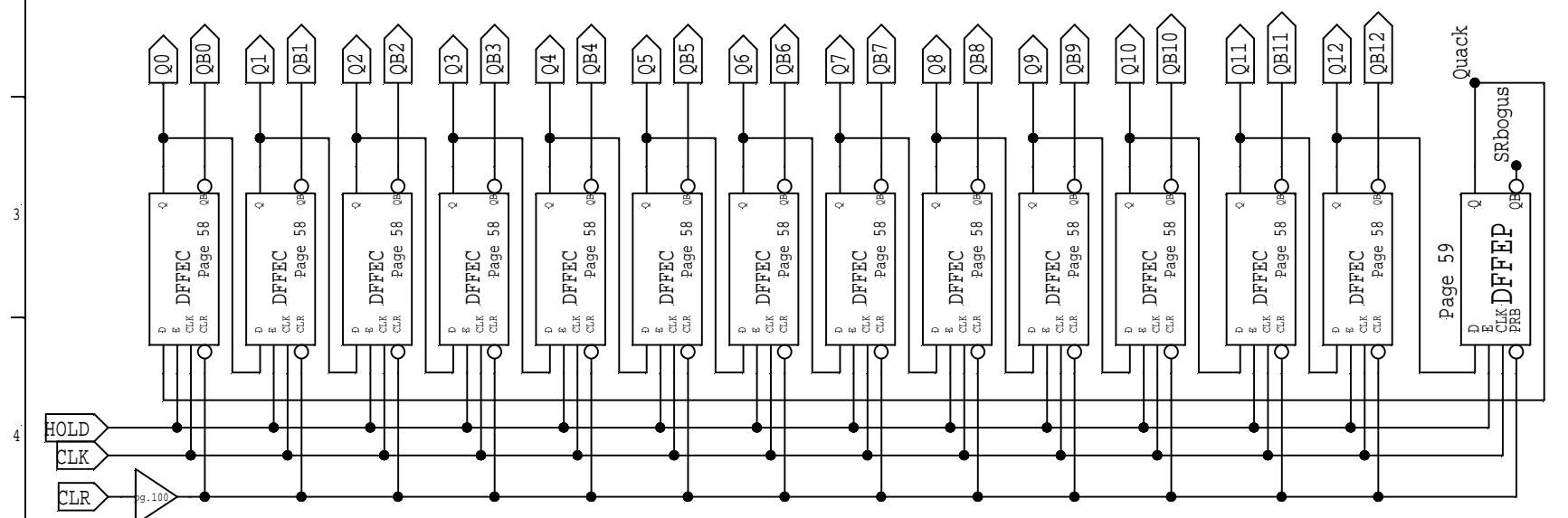
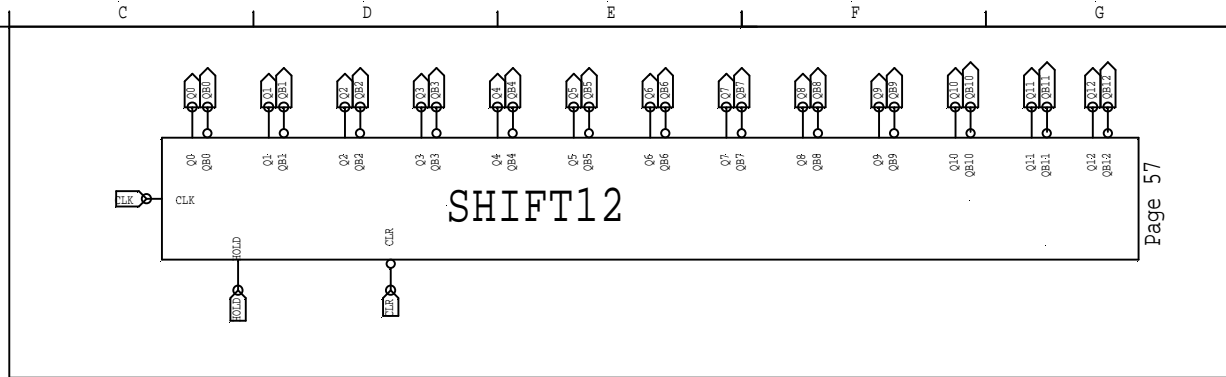


ADCCTRL

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University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822		Created: Nov 1, 1999 15:57:55	
		Modified: Aug 30, 2003 13:55:22	
Info: ADC Control Block		Size: 5x7	
Designer: Gary S. Varner		Rev A	
Module: ADCCTRL		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

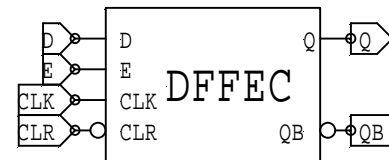
SHIFT12



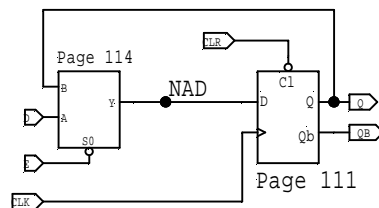
Page 57

University of Hawai'i, Manoa Instrument Development Lab (IDL) 2505 Correa Road, Honolulu, HI 96822		Tel: (808)956-2920 Fax: (808)956-2930	
Created:\$(Created)	Modified:\$(Modified)	Size: 5x7	
Info:\$(Info)		Rev A	
Designer:\$(Author)			
Module:\$(Module)		Page:\$(Page)	
Path:\$(File)			

DFFEC



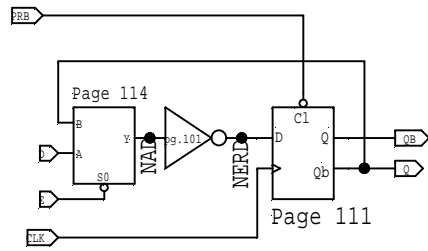
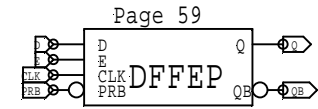
Page 58



Page 58

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: Nov 1, 1999 14:50:00		Size: 5x7	
Modified: Aug 30, 2003 13:55:22		Rev A	
Info: DFF w/Ena & Clear			Rev A
Designer: Gary S. Varner			
Module: DFFEC		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

DFFEP

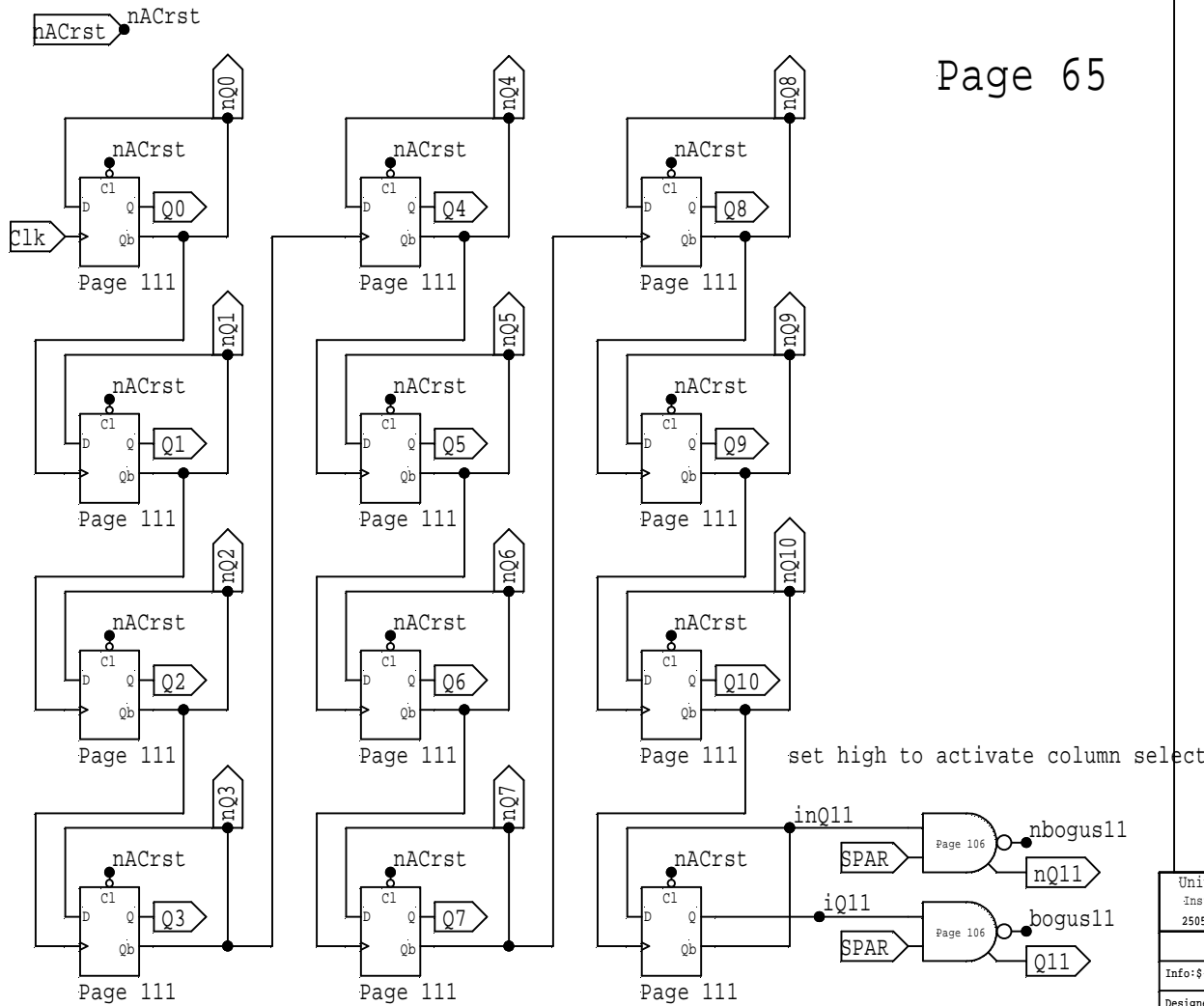


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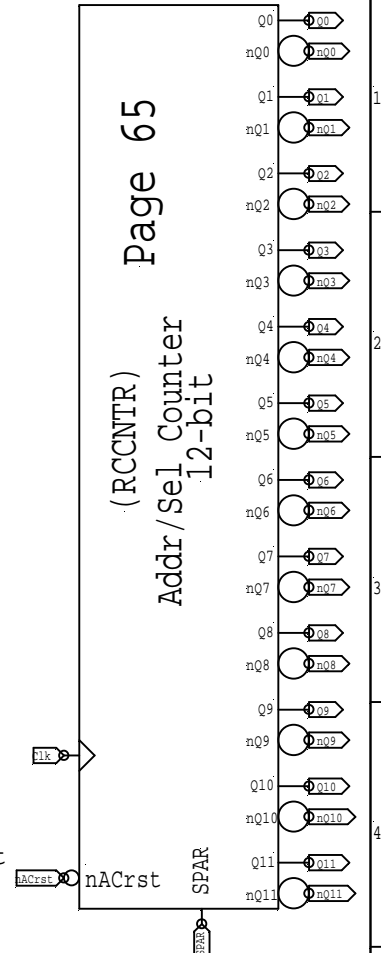
University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: Nov 1, 1999 15:07:45		Size: 5x7	
Modified: Aug 30, 2003 13:55:22		Rev A	
Info: presetable D Flip-flop			Rev A
Designer: Gary S. Varner			
Module: DFFEP		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

12-bit Ripple Counter (RCCNTR)

Page 65

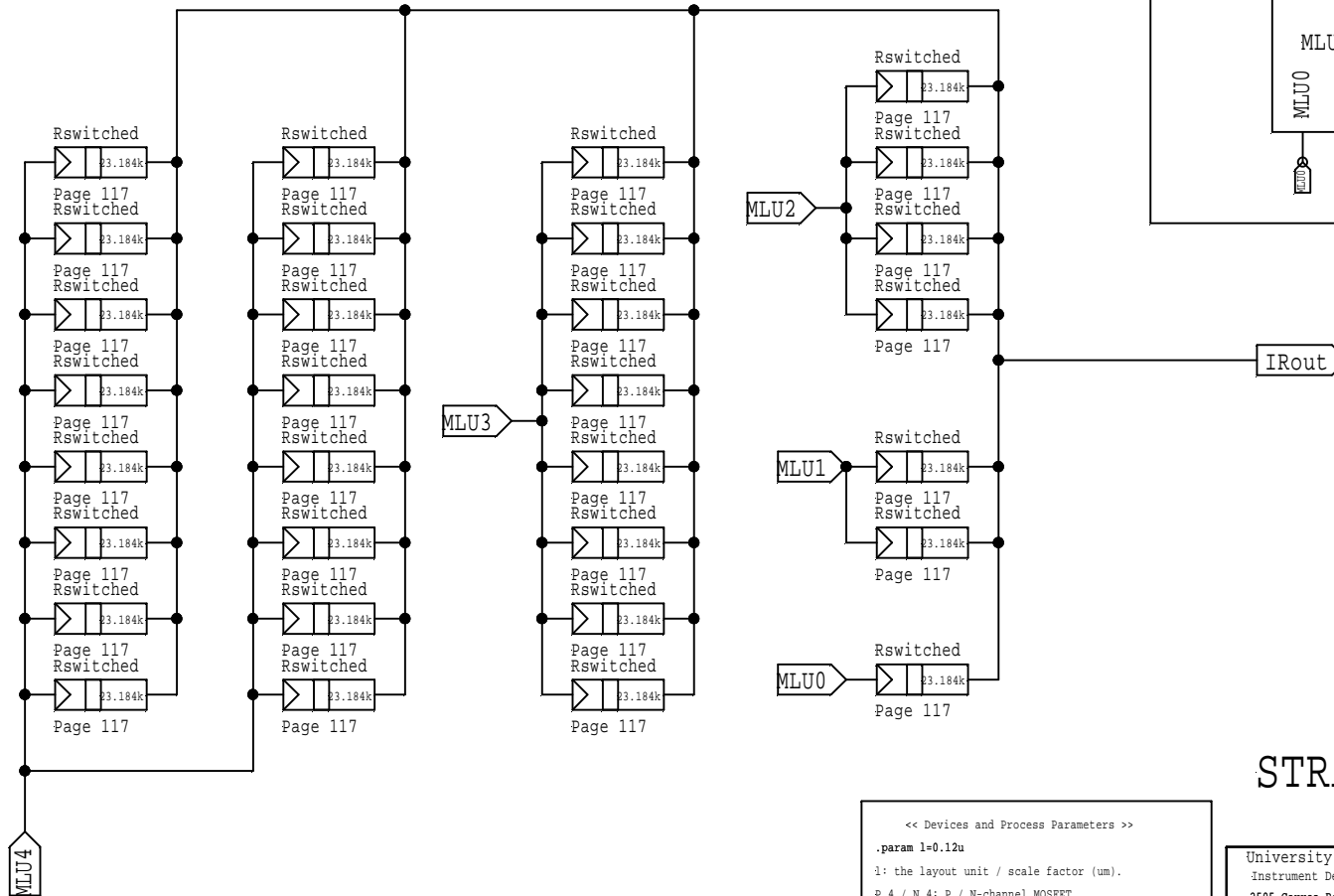


Page 65
(RCCNTR)
Addr/Sel Counter
12-bit



University of Hawai'i, Manoa tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created: \${Created}	Size: 5x7
Modified: \${Modified}	Rev A
Info: \${Info}	
Designer: \${Author}	
Module: \${Module}	Page: \${Page}
Path: \${File}	

MLU Select Level (MLU_R)



STRAW3 Page 66

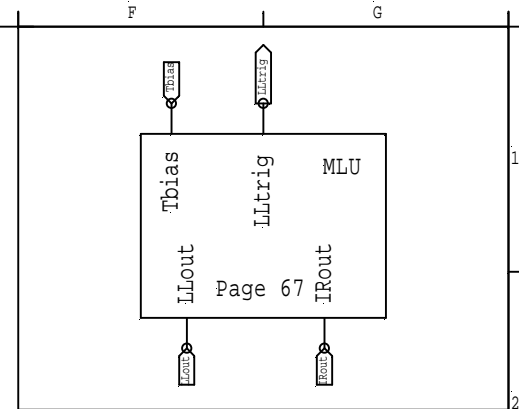
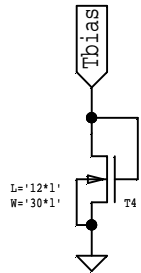
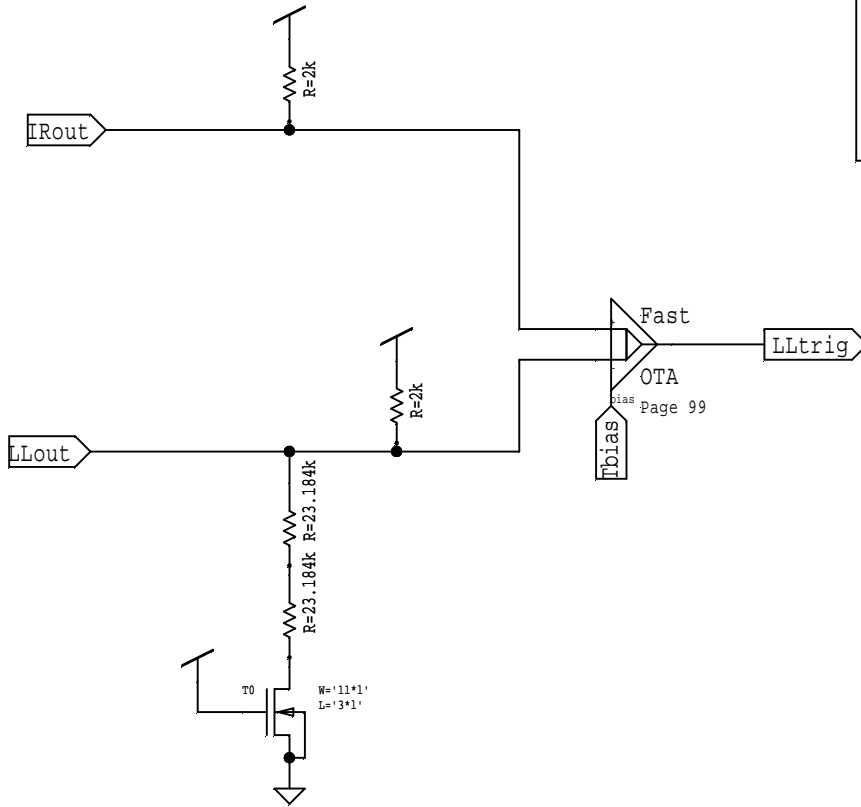
```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (1).
L: Gate Length (1).
AS / AD: Source/Drain Area A=W*L*1 (1)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (1)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created: May 5, 1993 21:36:43	Size: 5x7
Modified: Oct 23, 2002 08:06:33	Rev A
Info: MLU Trigger Reference	
Designer: Gary S. Varner, PhD	
Module: MLU_R	Page: Page0
Path: C:\CustomIC\STRAW3\STRAW3	

Majority Logic Unit (MLU)



```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
FS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

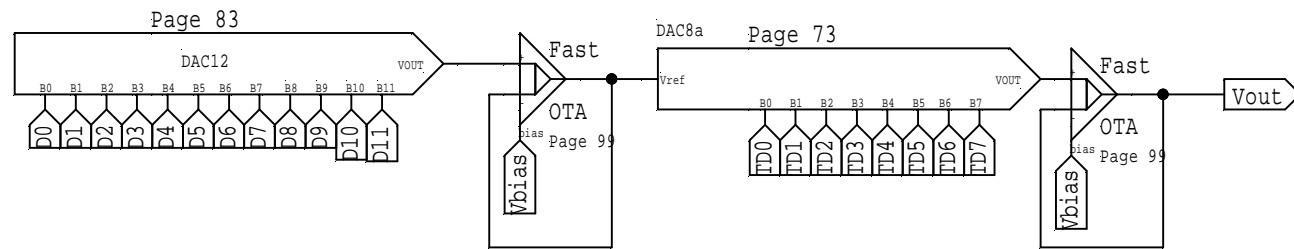
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

STRAW3 Page 67

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43		Size: 5x7	
Modified: Sep 4, 2003 11:21:53		Rev A	
Info: MLU Trigger			
Designer: Gary S. Varner, PhD			
Module: MLU		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

Include models

20 bit composite DAC (superDAC)



Include models

<< Devices and Process Parameters >>

```
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).
```

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

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University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: \${Created}		Size: 5x7	
Modified: \${Modified}		Rev A	
Info: \${Info}			
Designer: \${Author}			
Module: \${Module}		Page: \${Page}	
Path: \${File}			

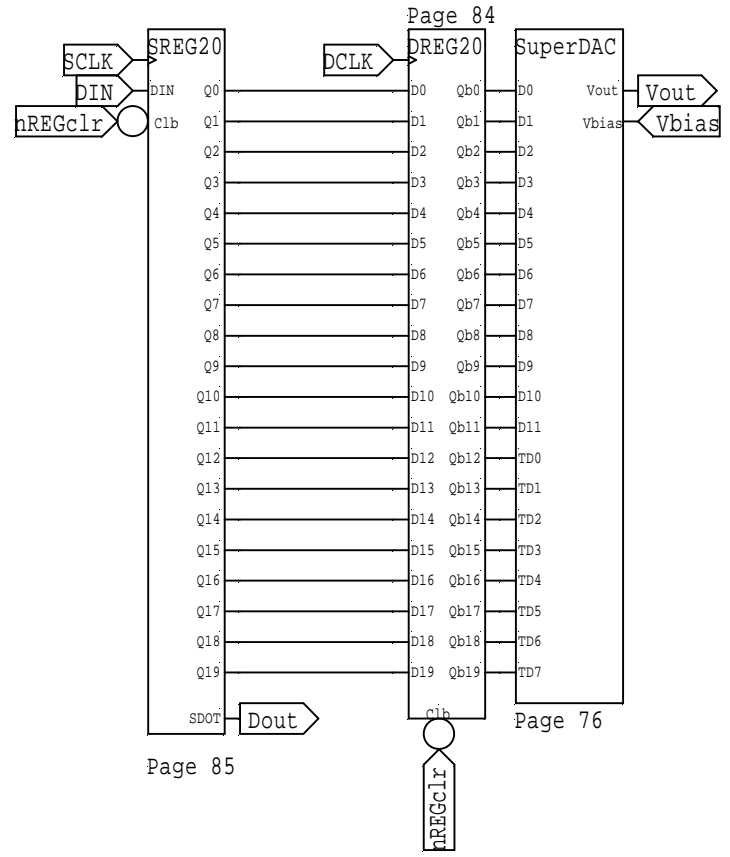
Serial-load SuperDAC [20-bit] (SS_DAC)

```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

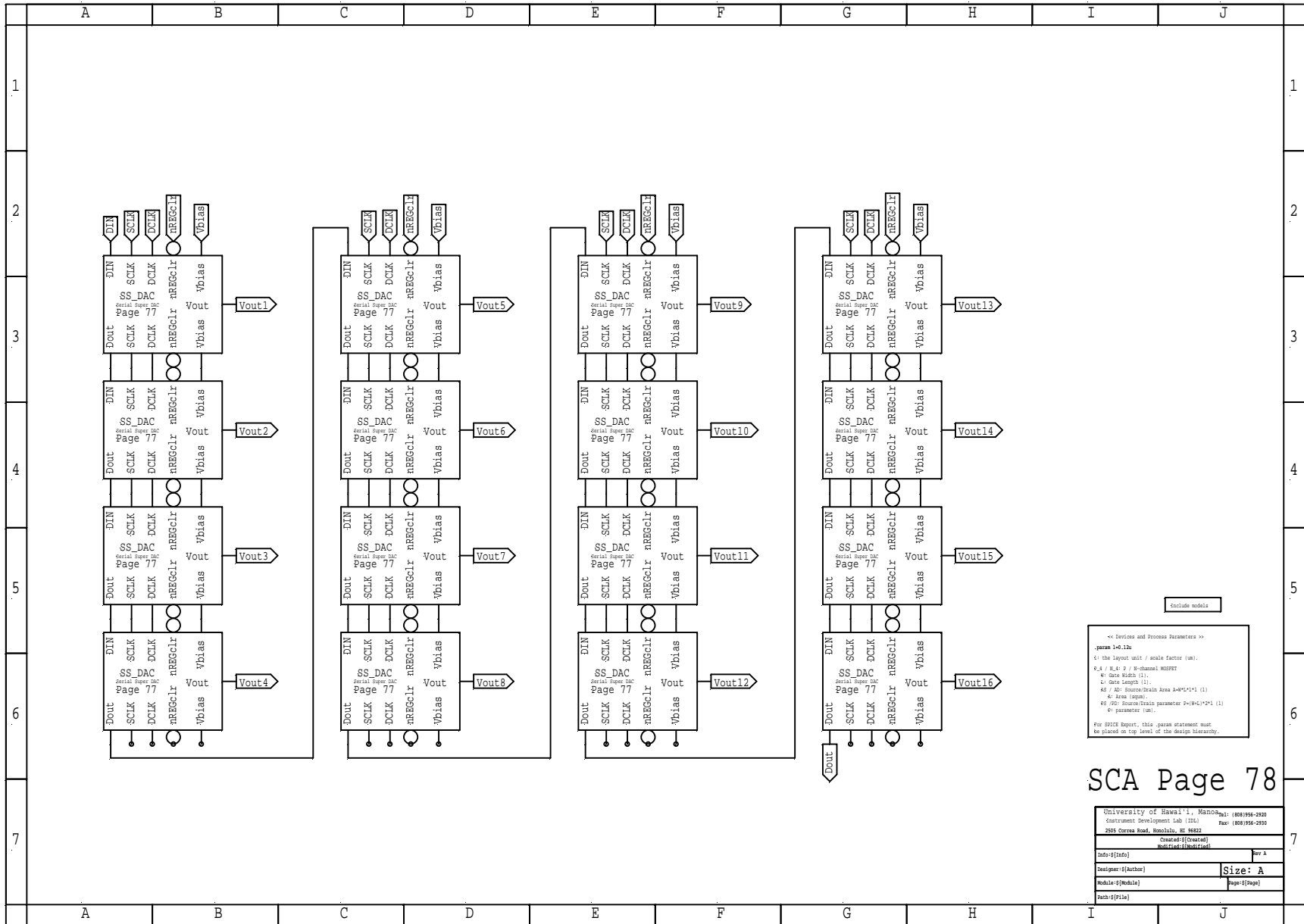
Include models



SCA Page 77

University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created: \${Created}	Size: 5x7
Modified: \${Modified}	Rev A
Info: \${Info}	
Designer: \${Author}	
Module: \${Module}	Page: \${Page}
Path: \${File}	

16 Ch. Serial SuperDAC [20-bit] (SS_DAC16)



```

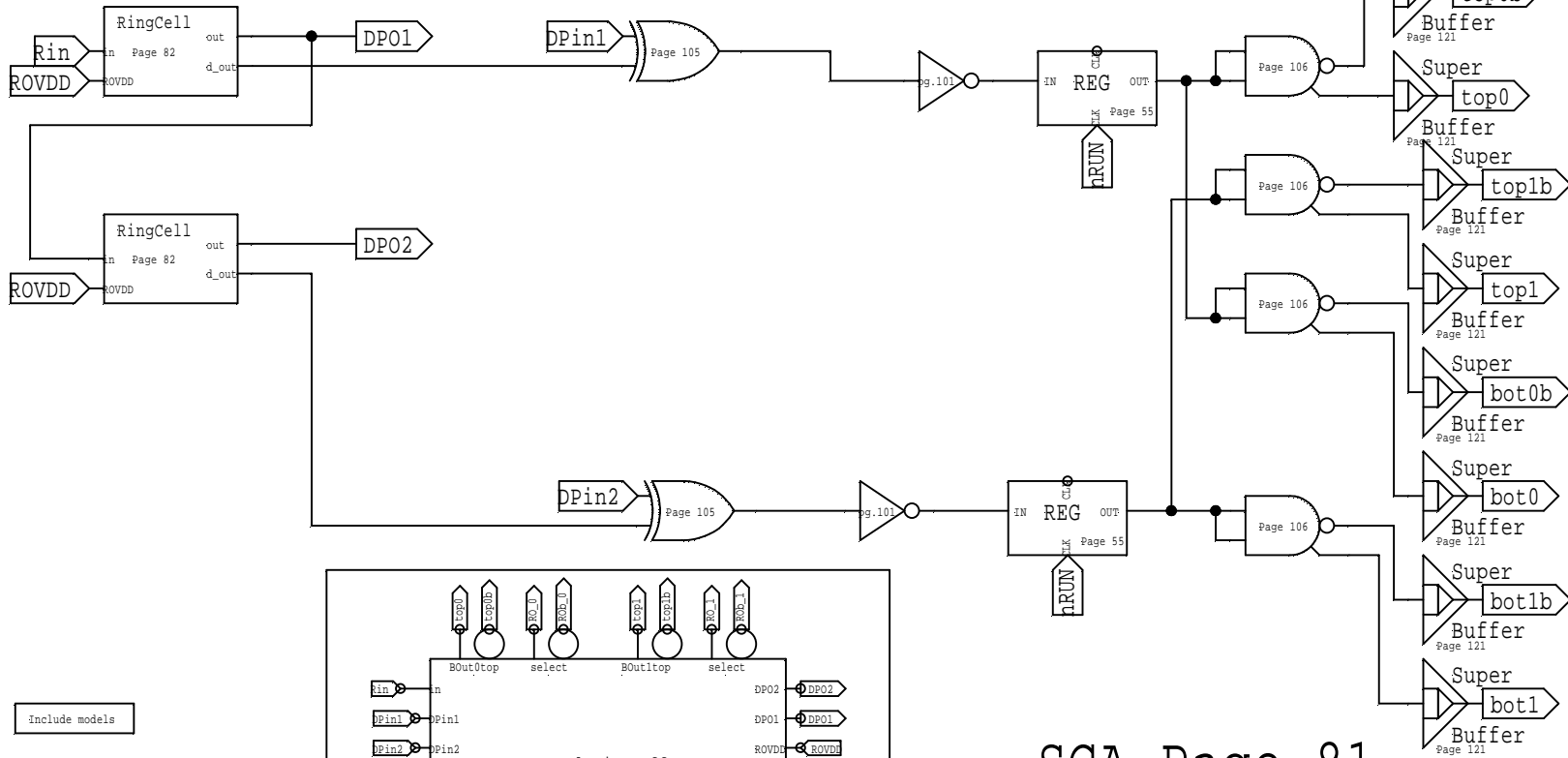
<< Device and Process Parameters >>
.param L4=120
<: the layout unit / scale factor (um).
0.4 / M: 0 / N: channel width
4: Data Width (1);
2: Data Length (1);
48 / 30: Source/Drain Area A=M*L*(1 / 1)
4: Area (squm);
90 / 90: Source/Drain parameter P=(M*L)*M*(1 / 1)
* parameter (um).

For SPICE Report, this .param statement must
be placed on top level of the design hierarchy.
    
```

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University of Hawaii, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2926	
2055 Correa Road, Honolulu, HI 96822			
Created: [Created]	Size: A		
Info: [Info]	Page: [Page]		
Designer: [Author]	Page: [Page]		
Module: [Module]	Page: [Page]		
Sub: [File]			

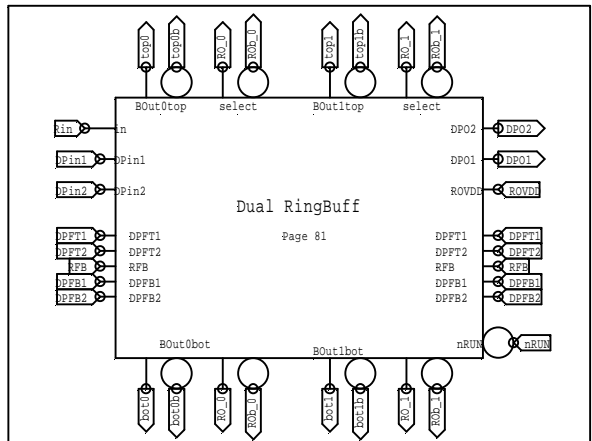
dual_ring_buffer



Include models

```
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).
```

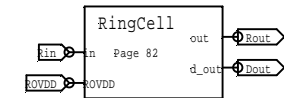
For SPICE Export, this .param statement must be placed on top level of the design hierarchy.



SCA Page 81

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: Jun 15, 1994 16:30:25	Size: 5x7		
Modified: May 20, 2002 15:05:25	Rev A		
Info: Dual Ring oscillator/fanout			
Designer: Dr. Gary S. Varner			
Module: dual_ring_buff		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

ring_cell



Include models

<< Devices and Process Parameters >>

```
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).
```

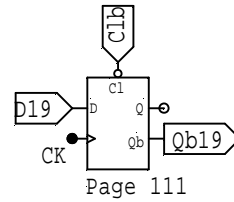
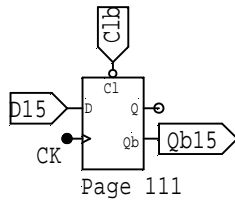
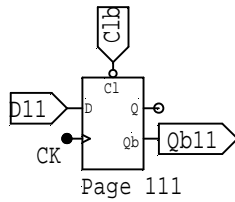
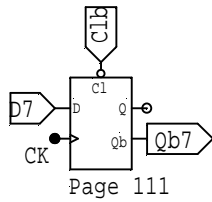
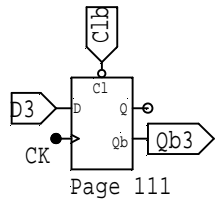
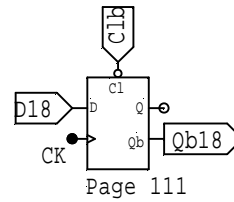
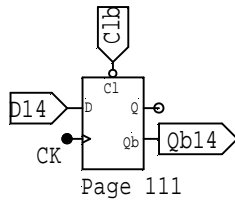
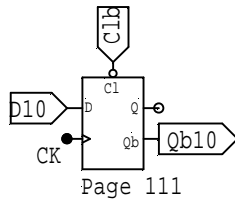
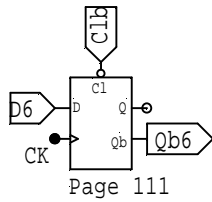
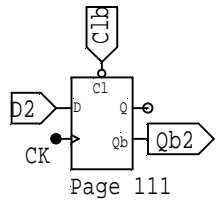
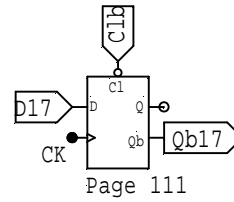
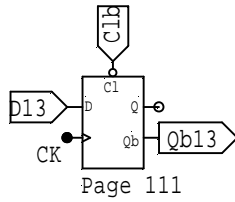
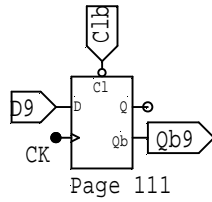
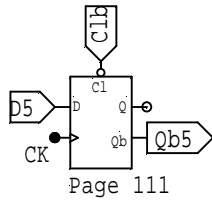
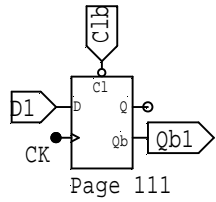
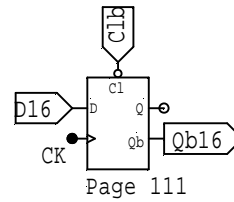
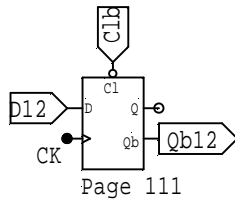
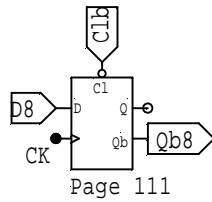
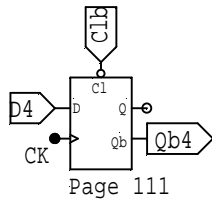
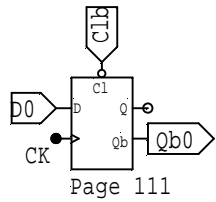
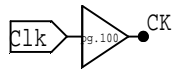
For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

SCA Page 82

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: \${Created}		Size: 5x7	
Modified: \${Modified}		Rev A	
Info: \${Info}			
Designer: \${Author}			
Module: \${Module}		Page: \${Page}	
Path: \${File}			

20-bit Data Register (DREG20)

special superDAC version (w/inv. outputs)

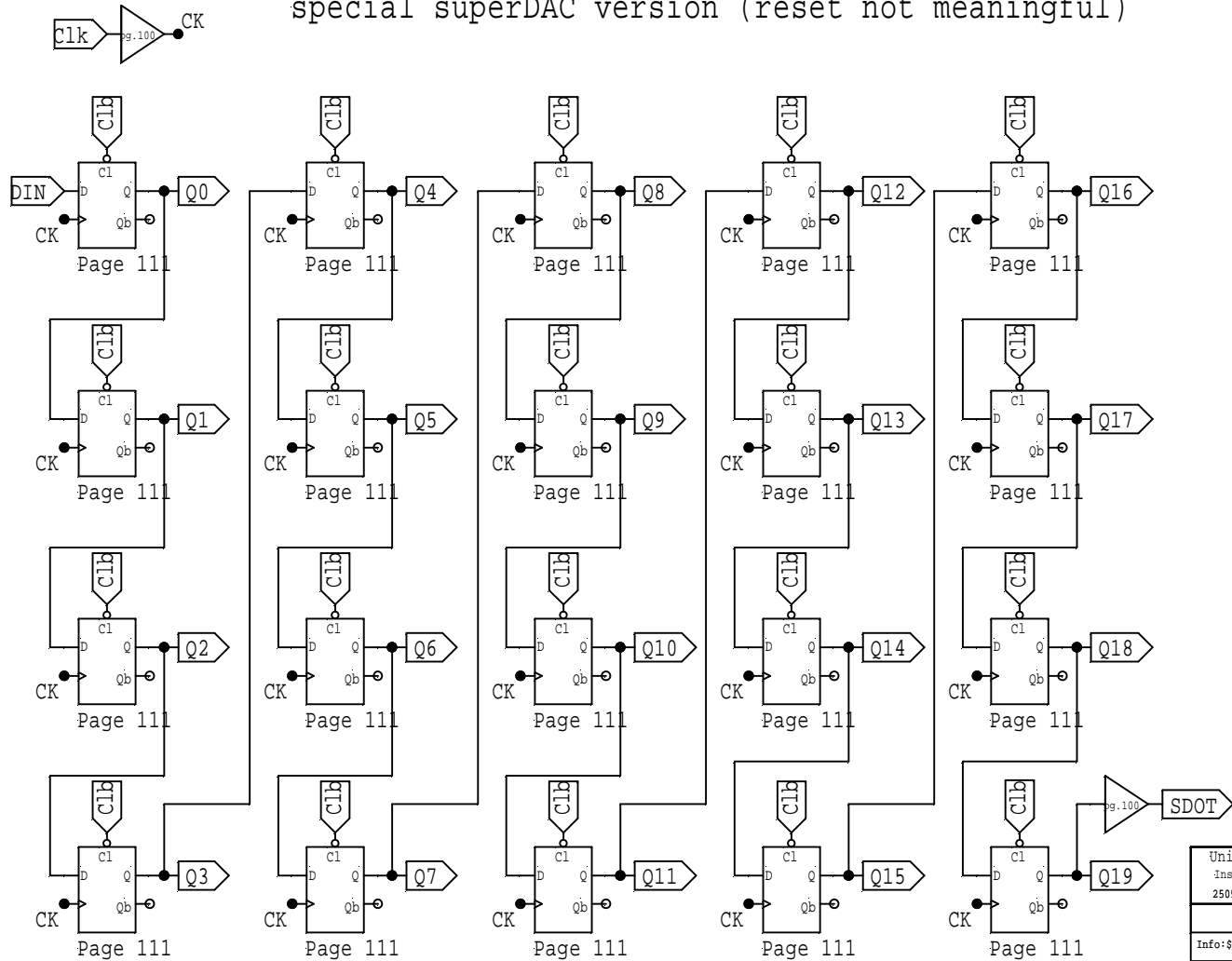


Page 84

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:41	Size: 5x7	Modified: Sep 1, 2003 14:55:16	
Info: D Flip-flop registers			Rev A
Designer: Dr. Gary S. Varner			
Module: DREG20		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

20-bit Shift Register (SREG20)

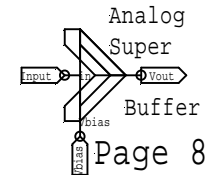
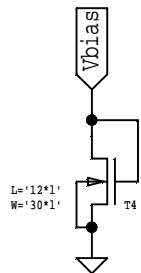
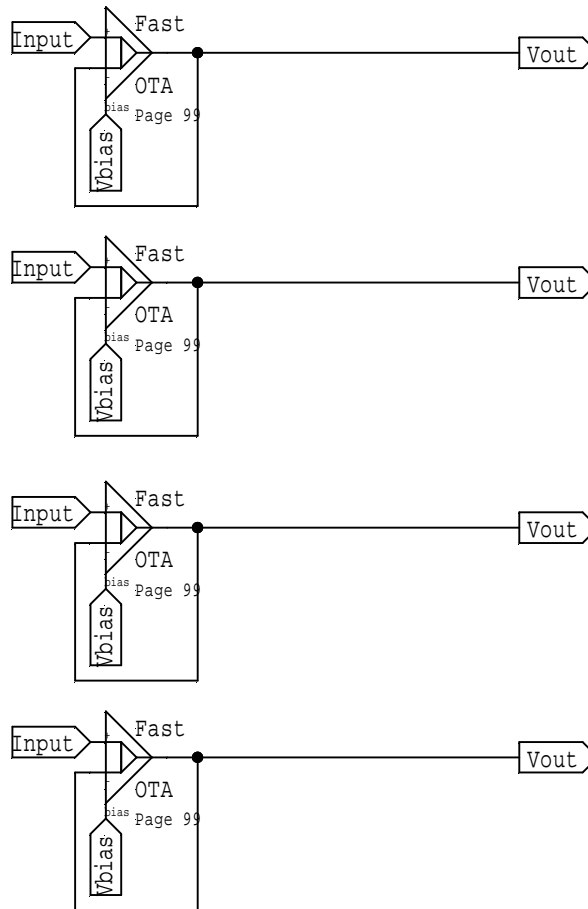
special superDAC version (reset not meaningful)



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University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: \${Created}		Size: 5x7	
Modified: \${Modified}		Rev A	
Info: \${Info}			
Designer: \${Author}			
Module: \${Module}		Page: \${Page}	
Path: \${File}			

Analog Output Super Buffer (ao_superbuff)



Page 88

```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*l*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*l (l)
P: parameter (um).

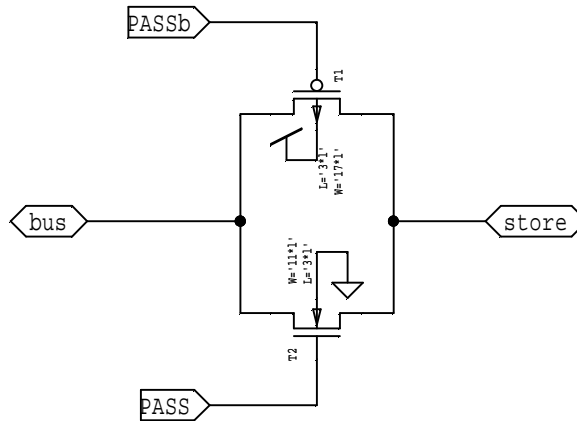
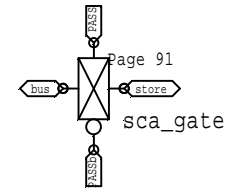
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

Include models

Page 88

University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created: Jun 15, 1994 16:30:25	Size: 5x7
Modified: Sep 4, 2003 11:24:40	Rev A
Info: Analog Output Buffer (ao_buff)	
Designer: Gary S. Varner	
Module: ao_superbuff	Page: Page0
Path: C:\CustomIC\STRAW3\STRAW3	

SCA Pass Transistor (sca_gate)



Include models

```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (1).
L: Gate Length (1).
AS / AD: Source/Drain Area A=W*L*1*1 (1)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (1)
P: parameter (um).

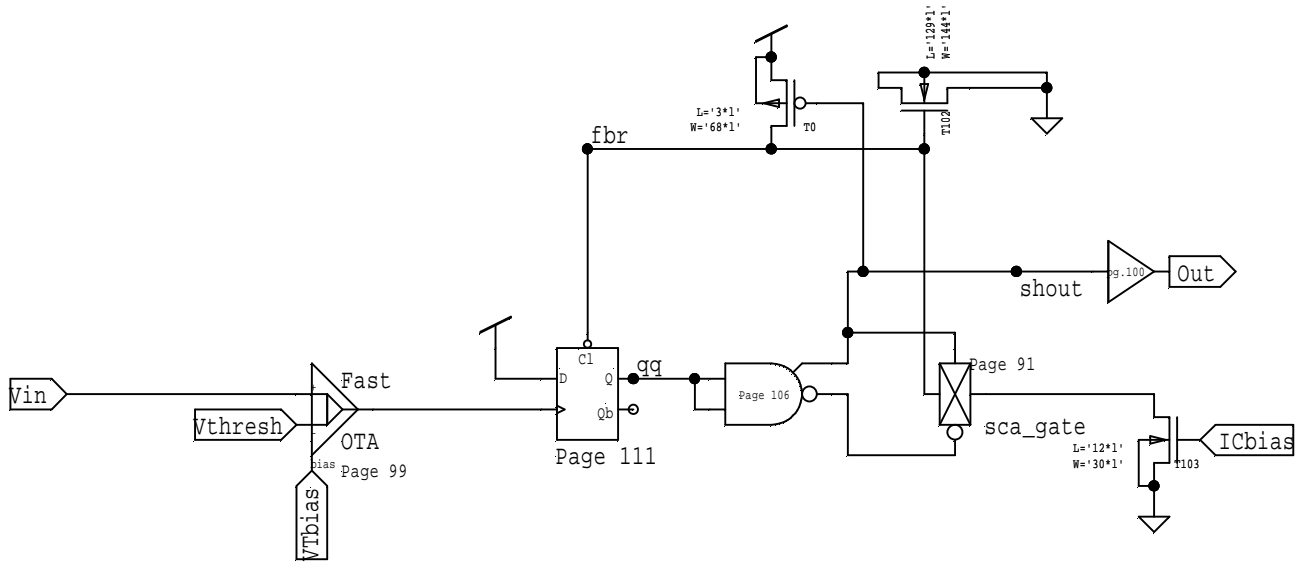
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

SCA Page 91

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created:\$(Created)		Size: 5x7	
Modified:\$(Modified)		Rev A	
Info:\$(Info)			
Designer:\$(Author)			
Module:\$(Module)		Page:\$(Page)	
Path:\$(File)			

Adj. Width Discriminator (discrim_adj)

17.3 x 20.8um ~ 1.58pF (4.8fF/um^2 but 1.58pF extracted)

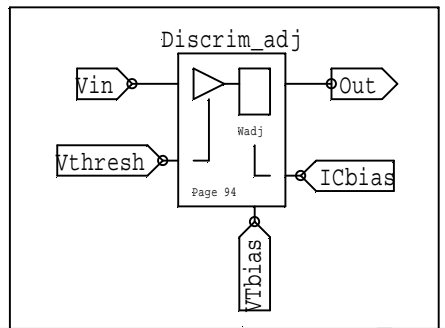


Include models

options

```
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

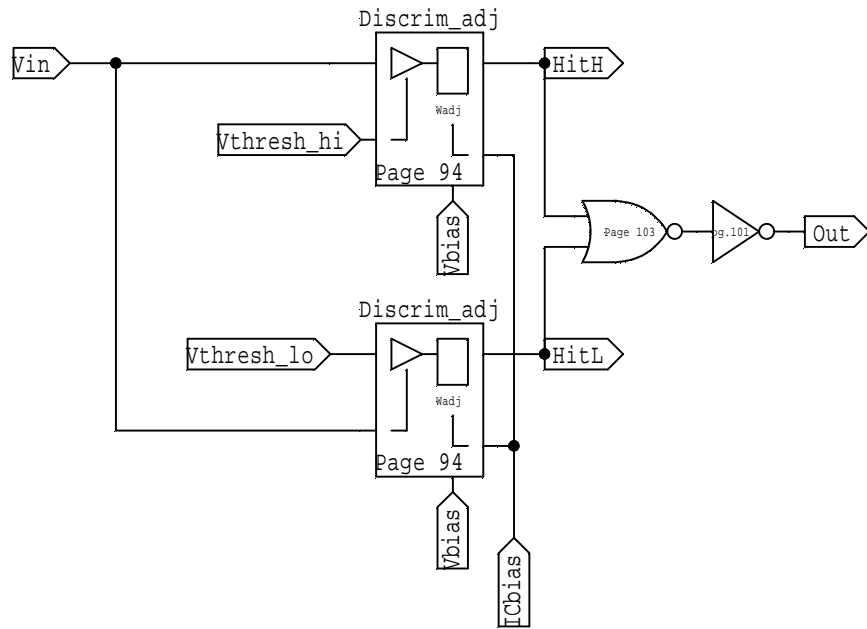
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
```



STRAW3 Page 94

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: Nov 3, 1999 09:33:45	Size: 5x7		
Modified: Oct 23, 2002 07:02:38	Rev A		
Info: 32-chan SCA/Trigger chip			
Designer: Dr. Gary S. Varner			
Module: discrim_adj		Page: Page 0	
Path: C:\CustomIC\STRAW3\STRAW3			

upper and lower disrim pair (discrim_pair)



```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l)
L: Gate Length (l)
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

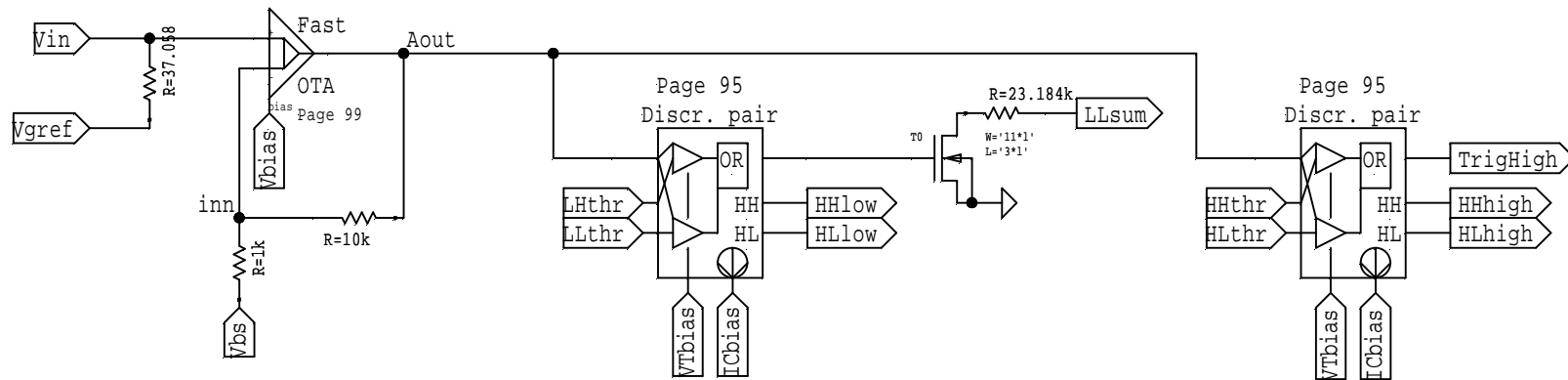
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

include models

STRAW3 Page 95

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: Nov 3, 1999 09:33:45		Size: 5x7	
Modified: Oct 23, 2002 07:00:59		Rev A	
Info: Simulation for trigger on Bi-polar pulses			
Designer: Dr. Gary S. Varner			
Module: discrim_pair		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

disrim high-low block (discrim_hl)



```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l)
L: Gate Length (l)
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm)
PS /PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

include models

STRAW3 Page 96

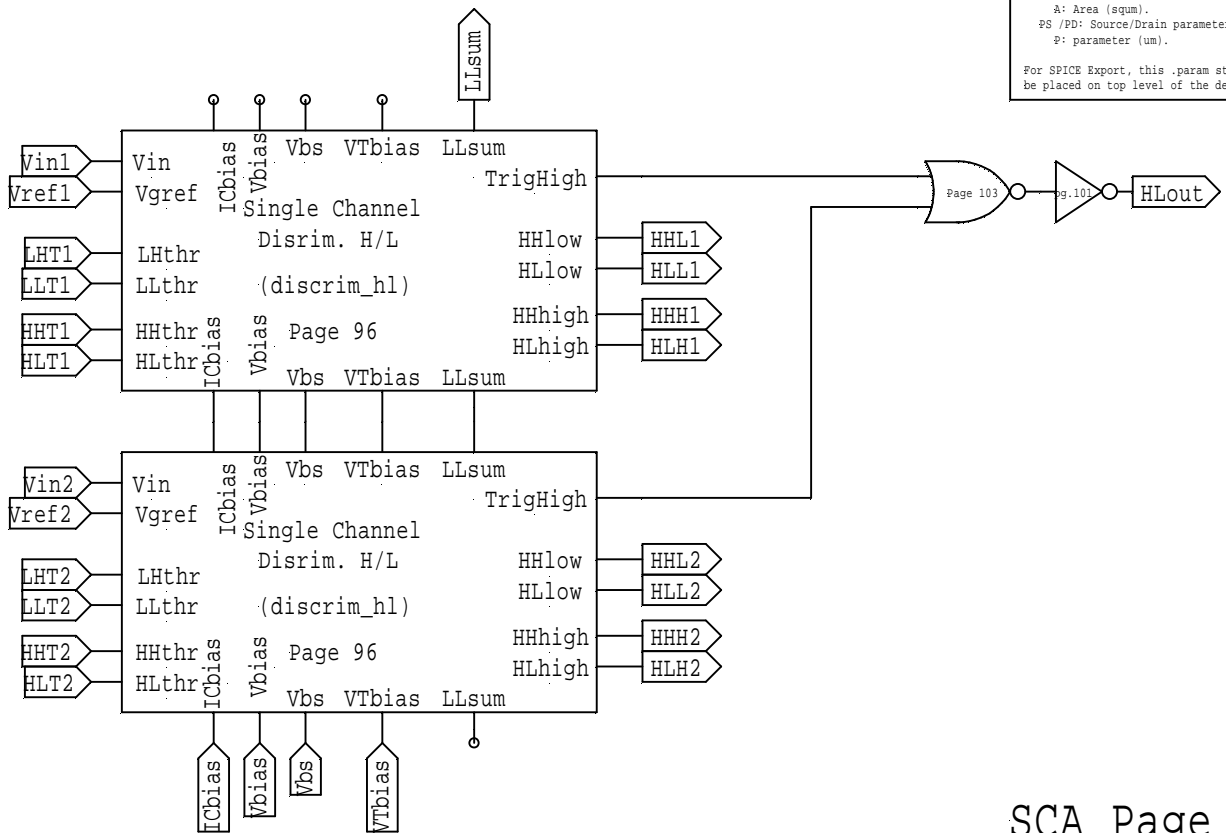
University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: Nov 3, 1999 09:33:45		Size: 5x7	
Modified: Sep 4, 2003 10:52:04		Rev A	
Info: High & Low bi-level Discrim. block			
Designer: Gary S. Varner, PhD			
Module: discrim_hl		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

Pair of Comp Pairs (PairCompPair)

```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```



Include models

SCA Page 97

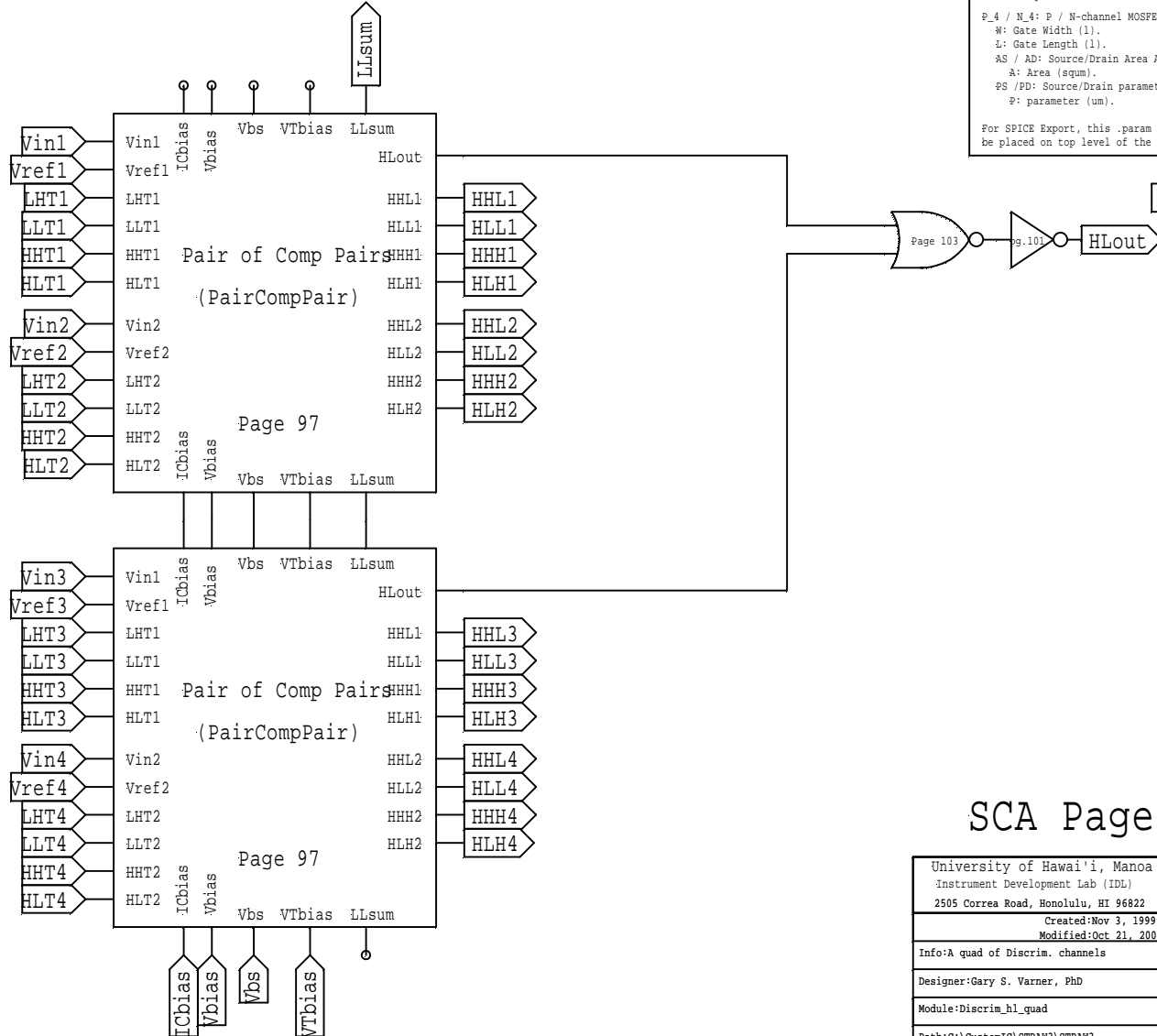
University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: \${Created}	Modified: \${Modified}	Size: 5x7	
Info: \${Info}			Rev A
Designer: \${Author}			
Module: \${Module}		Page: \${Page}	
Path: \${File}			

Set of 4 Discrim blocks (Discrim_hl_quad)

```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

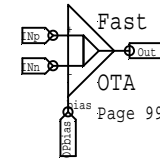


include models

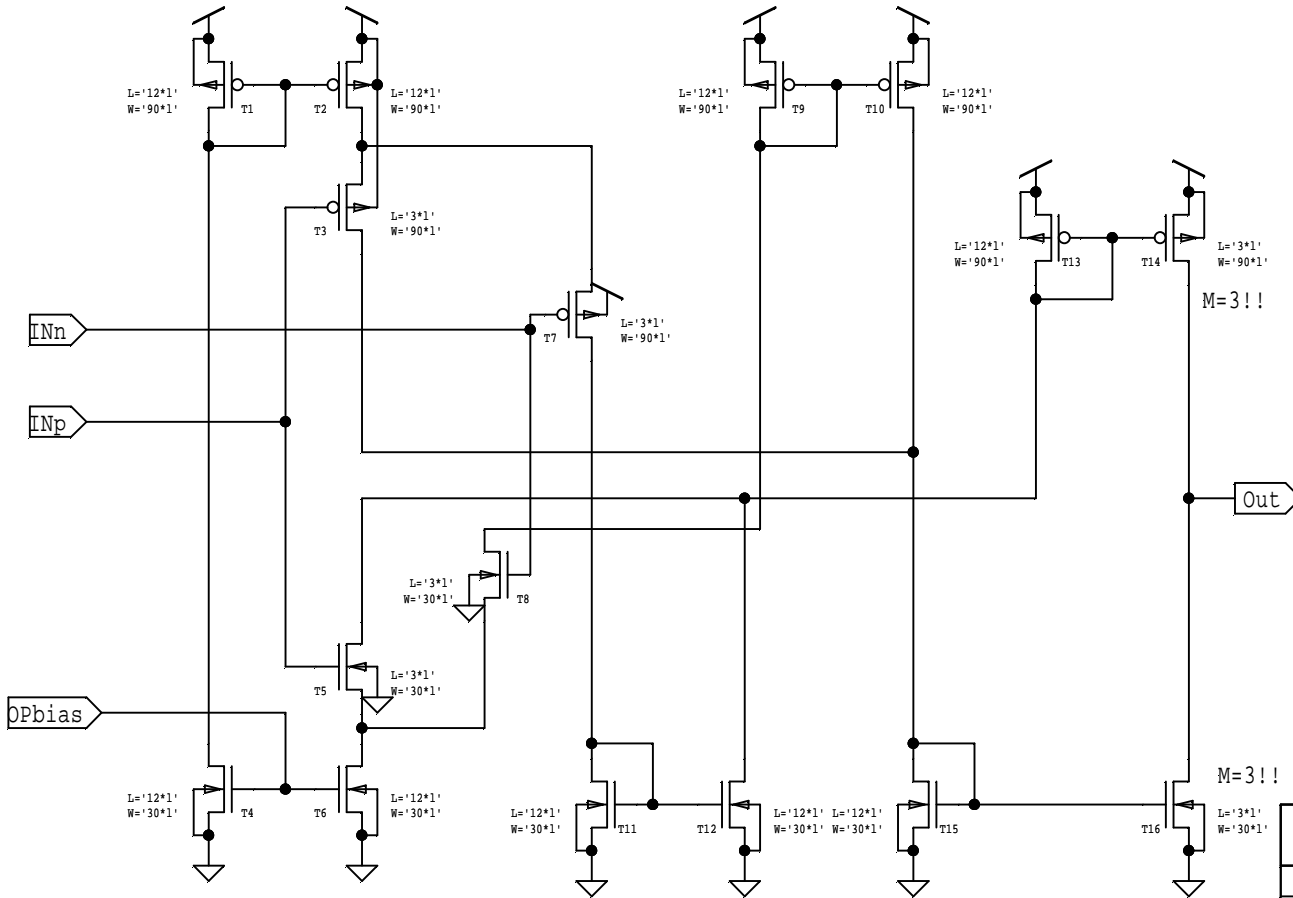
SCA Page 98

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: Nov 3, 1999 09:33:45		Size: 5x7	
Modified: Oct 21, 2002 19:24:24		Rev A	
Info: A quad of Discrim. channels			
Designer: Gary S. Varner, PhD			
Module: Discrim_hl_quad		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

OTA for Fast performance (OTA)



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<< Devices and Process Parameters >>

```
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
```

Include models

Page 99

University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created: May 5, 1993 21:36:43	Size: 5x7
Modified: Oct 23, 2002 06:43:53	Rev A
Info: Fast Operational Transimp Amp	
Designer: Gary S. Varner	
Module: OTA	Page: Page0
Path: C:\CustomIC\STRAW3\STRAW3	

A B C D E F G

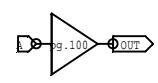
1

2

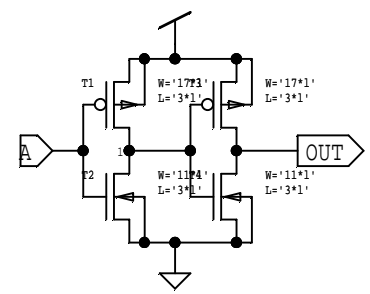
3

4

5



Buf1



Include models

```

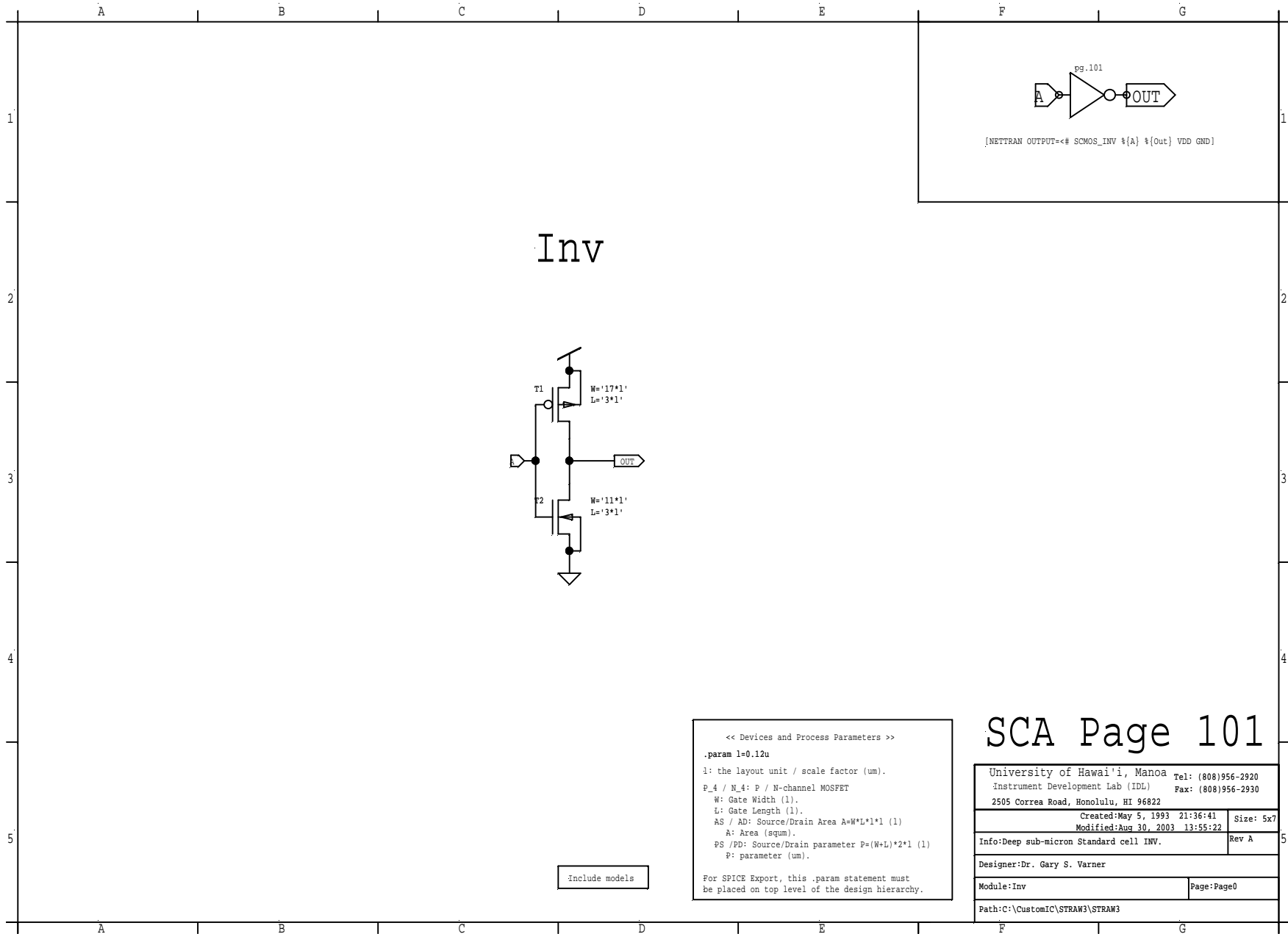
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

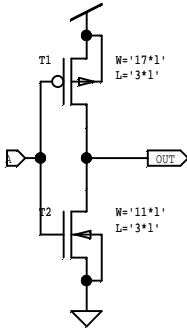
SCA Page 100

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:41		Size: 5x7	
Modified: Aug 30, 2003 13:55:22		Rev A	
Info: Std. min. Digital buffer			
Designer: Dr. Gary S. Varner			
Module: Buf1		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

A B C D E F G



Inv



Include models

```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

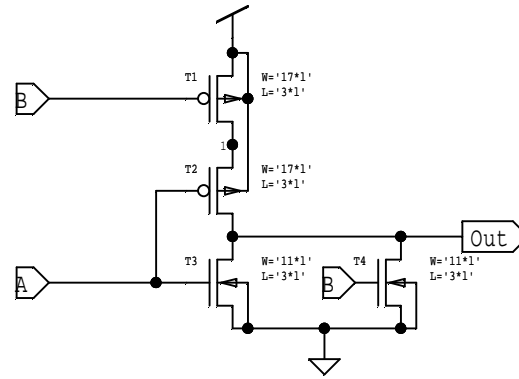
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.

```

SCA Page 101

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:41		Size: 5x7	
Modified: Aug 30, 2003 13:55:22		Rev A	
Info: Deep sub-micron Standard cell INV.			
Designer: Dr. Gary S. Varner			
Module: Inv		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

NOR2



Include models

```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```



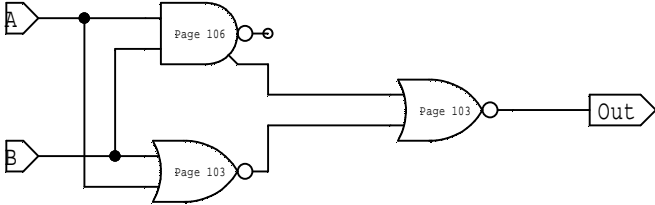
[NETTRAN OUTPUT=<<# SCMOS_NOR2 #[A] #[B] #[Out]]

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43		Size: 5x7	
Modified: Aug 30, 2003 13:55:22		Rev A	
Info: Deep sub-micron Standard Cell NOR2			
Designer: Dr. Gary S. Varner			
Module: NOR2		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

XOR2



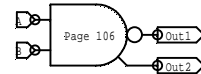
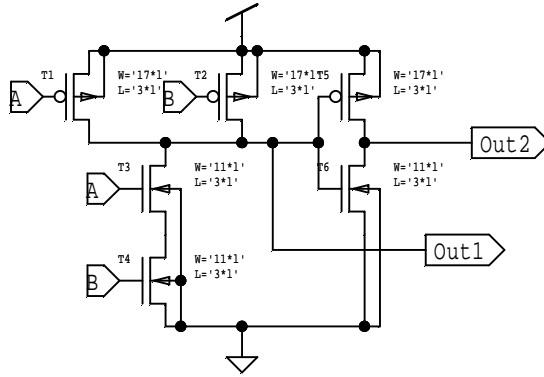
```
[NETTRAN OUTPUT=<# SCMOS_XOR2 %[a] %[b] %Out]]
```



Page 105

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: \${Created}		Size: 5x7	
Modified: \${Modified}		Rev A	
Info: \${Info}			
Designer: \${Author}			
Module: \${Module}		Page: \${Page}	
Path: \${File}			

NAND2C



[NETTRAN OUTPUT-<# SCMOS_NAND2C %[A] %[B] %[Out1] %[Out2]]

```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

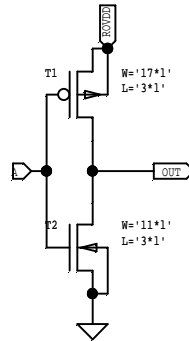
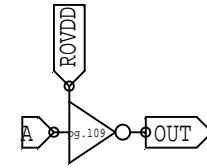
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

Page 106

Include models

University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created: May 5, 1993 21:36:43	Size: 5x7
Modified: Sep 3, 2003 11:56:05	Rev A
Info: Deep sub-micron Standard cell NAND2C	
Designer: Dr. Gary S. Varner	
Module: NAND2C	Page: Page0
Path: C:\CustomIC\STRAW3\STRAW3	

Ring Oscillator Inverter (ring_osc_inv)



Include models

<< Devices and Process Parameters >>

```
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).
```

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

SCA Page 109

University of Hawai'i, Manoa Tel: (808)956-2920
 Instrument Development Lab (IDL) Fax: (808)956-2930
 2505 Correa Road, Honolulu, HI 96822

Created: \${Created}		Size: 5x7
Modified: \${Modified}		Rev A
Info: \${Info}		
Designer: \${Author}		
Module: \${Module}		Page: \${Page}
Path: \${File}		

A B C D E F G

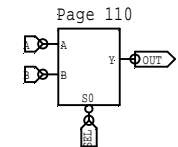
1

2

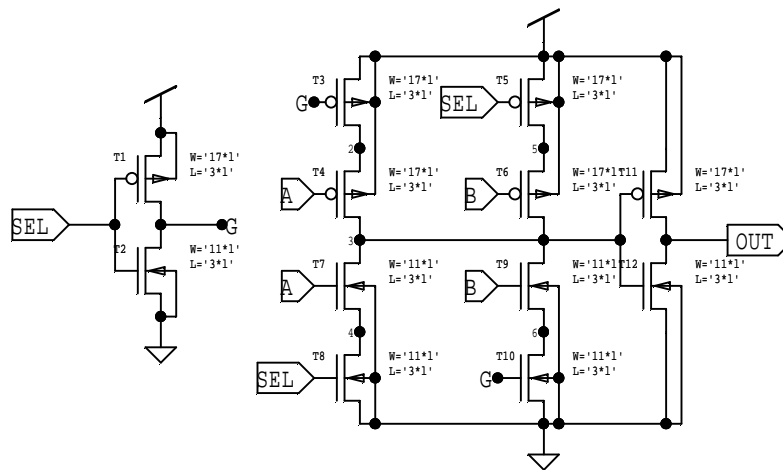
3

4

5



Mux2



Include models

```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

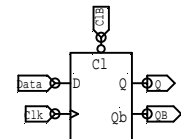
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

Page 110

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43		Size: 5x7	
Modified: Oct 23, 2002 07:22:29		Rev A	
Info: 2-input MUX			
Designer: Gary S. Varner			
Module: Mux2		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

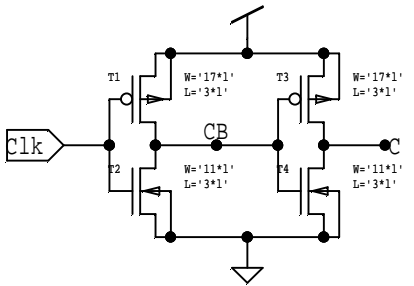
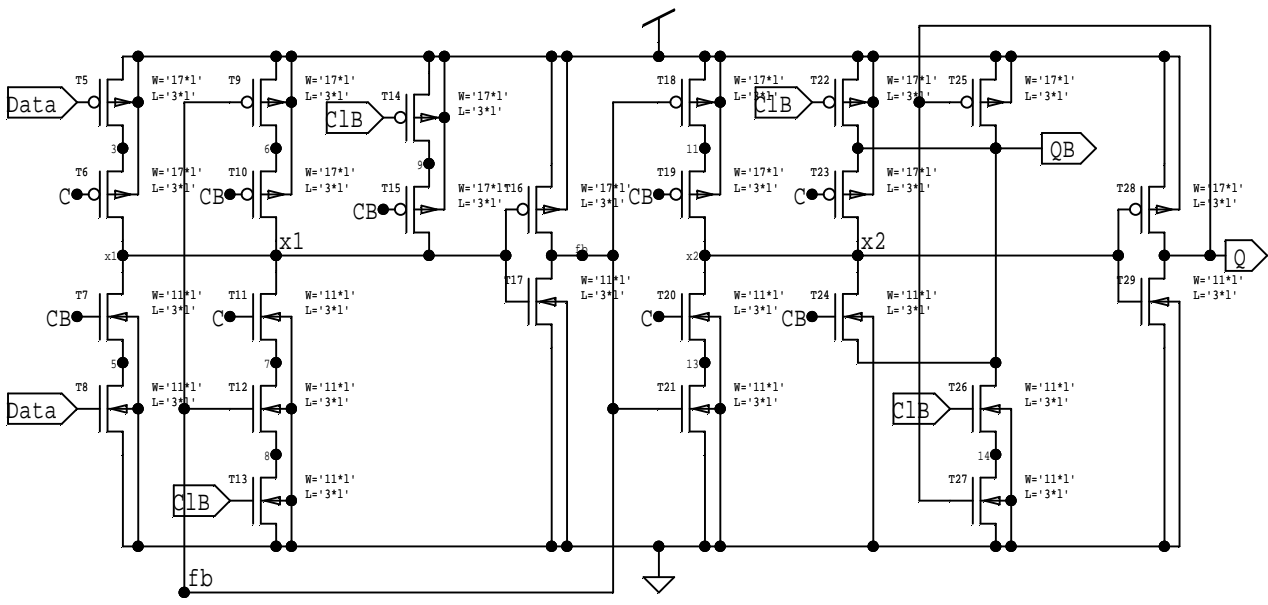
A B C D E F G

DFFC



Page 111

Include models



```

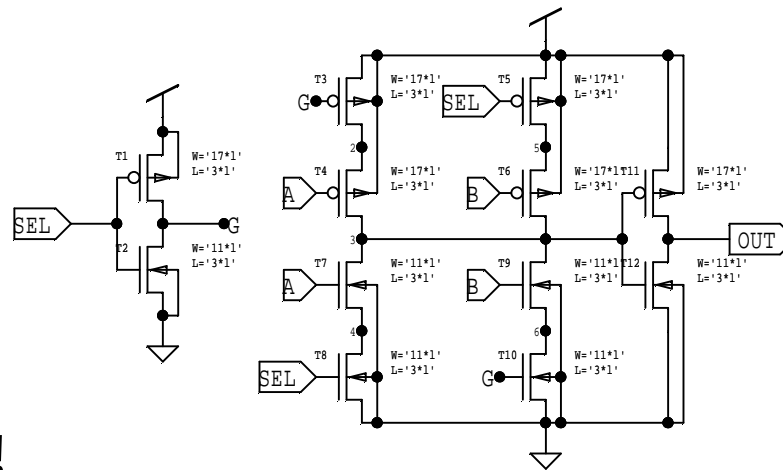
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

Page 111

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:41		Size: 5x7	
Modified: Aug 30, 2003 15:33:40		Rev A	
Info: D Flip-Flop with Clear			
Designer: Dr. Gary S. Varner			
Module: DFFC		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

Mux2ADC



N.B.!!

opposite definition for ADC!!

Include models

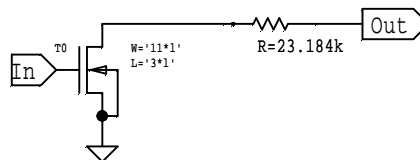
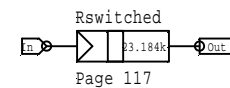
```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43		Size: 5x7	
Modified: Sep 4, 2003 11:56:08		Rev A	
Info: 2-input MUX			
Designer: Gary S. Varner			
Module: Mux2ADC		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

Switched R (Rsw)



Include models

```

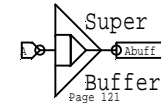
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (1).
L: Gate Length (1).
AS / AD: Source/Drain Area A=W*L*1*1 (1)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (1)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

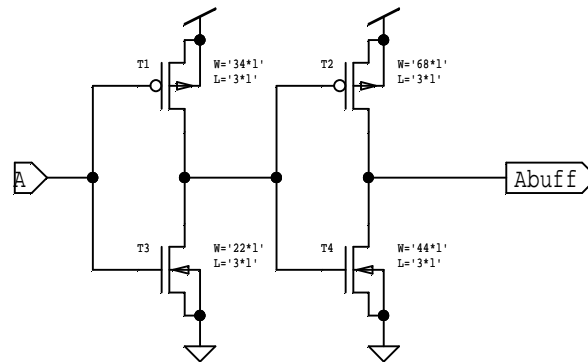
STRAW3 Page 117

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created:\$(Created)		Size: 5x7	
Modified:\$(Modified)		Rev A	
Info:\$(Info)			
Designer:\$(Author)			
Module:\$(Module)		Page:\$(Page)	
Path:\$(File)			

Super Buffer (super_buff)



[NETTRAN OUTPUT=<# SCMOS_DFF %[Data] %[Clk] %[Q] %[QB]]



SCA Page 121

<< Devices and Process Parameters >>

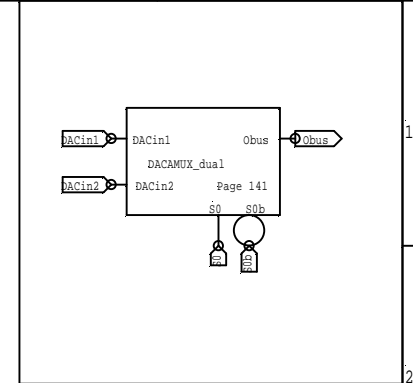
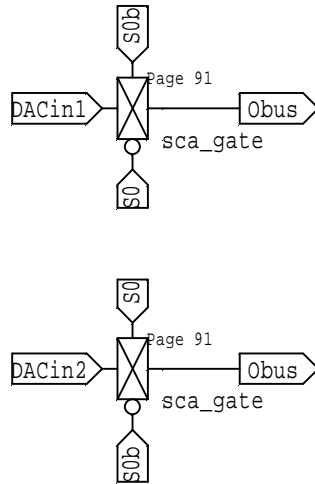
```
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).
```

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

include models

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created:\${Created}		Size: 5x7	
Modified:\${Modified}		Rev A	
Info:\${Info}			
Designer:\${Author}			
Module:\${Module}		Page:\${Page}	
Path:\${File}			

DAC Analog MUX 2-Ch. (DACAMUX_dual)



```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*l (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W*L)*2*l (l)
P: parameter (um).

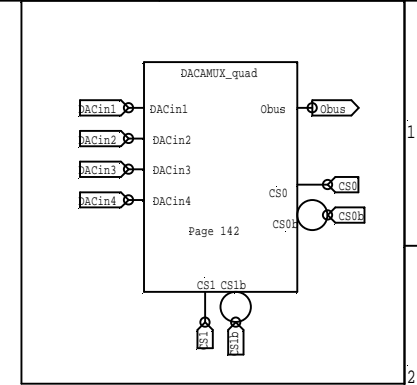
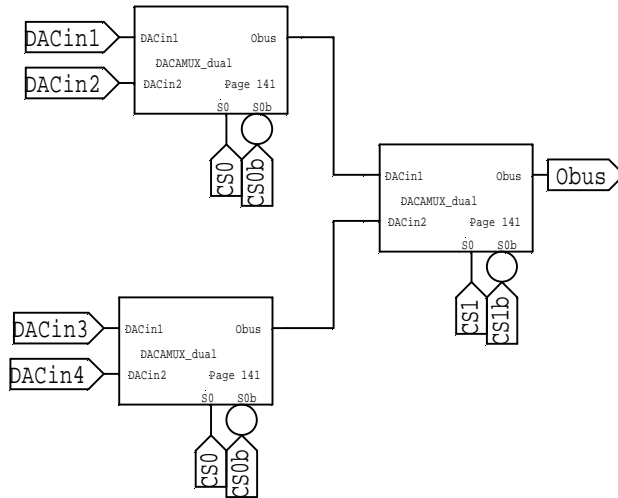
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

include models

SCA Page 141

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43		Size: 5x7	
Modified: Oct 23, 2002 06:53:23		Rev A	
Info: dual Analog MUX			
Designer: Dr. Gary S. Varner			
Module: DACAMUX_dual		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

DAC Analog Mux 4-Ch. (DACAMUX_quad)



```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

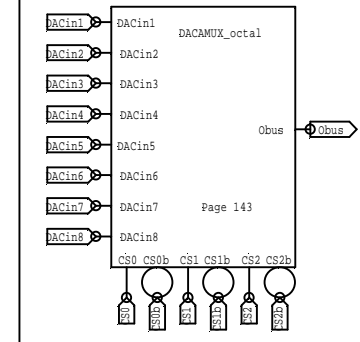
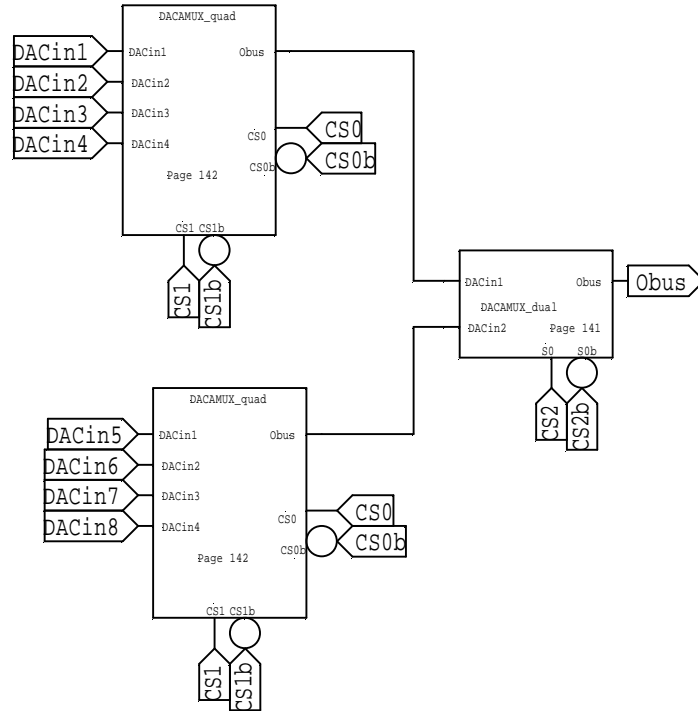
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

include models

SCA Page 142

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43		Size: 5x7	
Modified: Oct 23, 2002 06:52:31		Rev A	
Info: Analog MUX element			Rev A
Designer: Dr. Gary S. Varner			
Module: DACAMUX_quad		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

DAC Analog Mux 8-Ch. (DACAMUX_octal)



SCA Page 143

<< Devices and Process Parameters >>

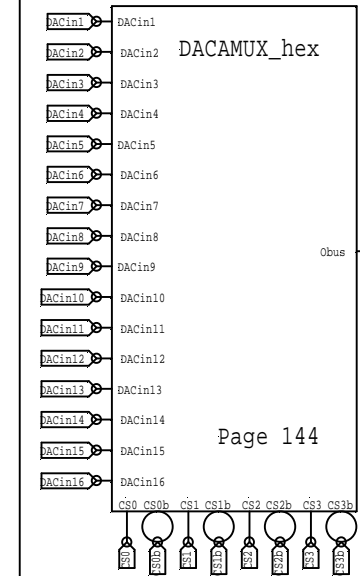
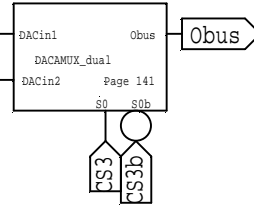
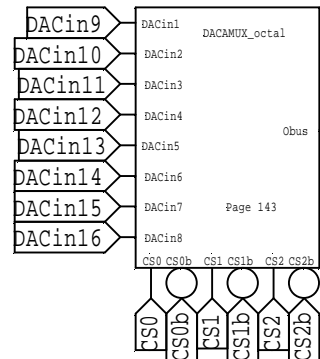
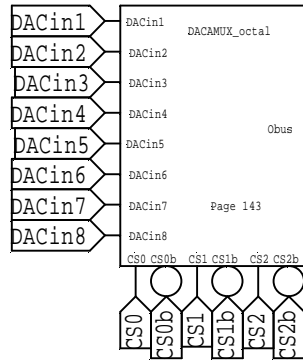
```
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).
```

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

include models

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43		Size: 5x7	
Modified: Oct 15, 2002 07:37:33		Rev A	
Info: A/M 12-bit Bus select			Rev A
Designer: Dr. Gary S. Varner			
Module: DACAMUX_octal		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

DAC Analog Mux 16-Ch. (DACAMUX_octal)



```
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
```

include models

SCA Page 144

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43	Size: 5x7		
Modified: Oct 15, 2002 07:37:33	Rev A		
Info: A/M 12-bit Bus select			
Designer: Dr. Gary S. Varner			
Module: DACAMUX_hex		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

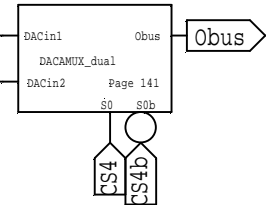
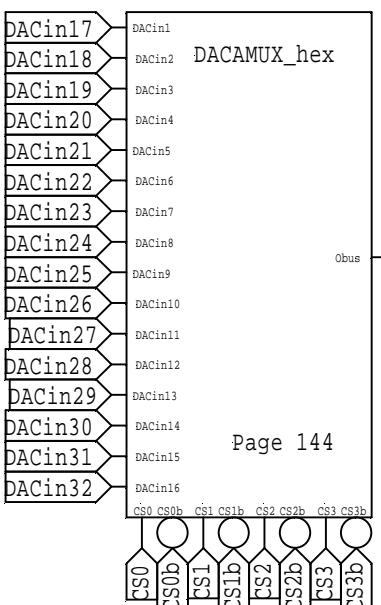
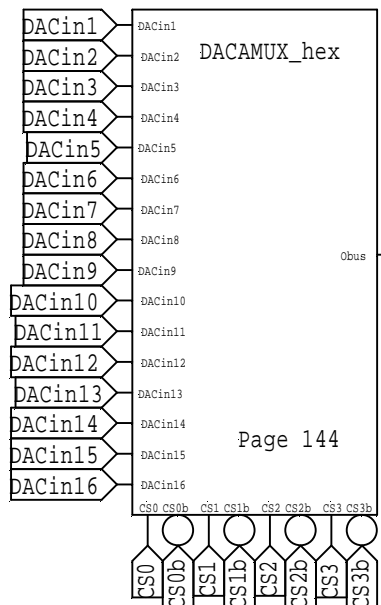
DAC Analog Mux 32-Ch. (DACAMUX_32)

```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

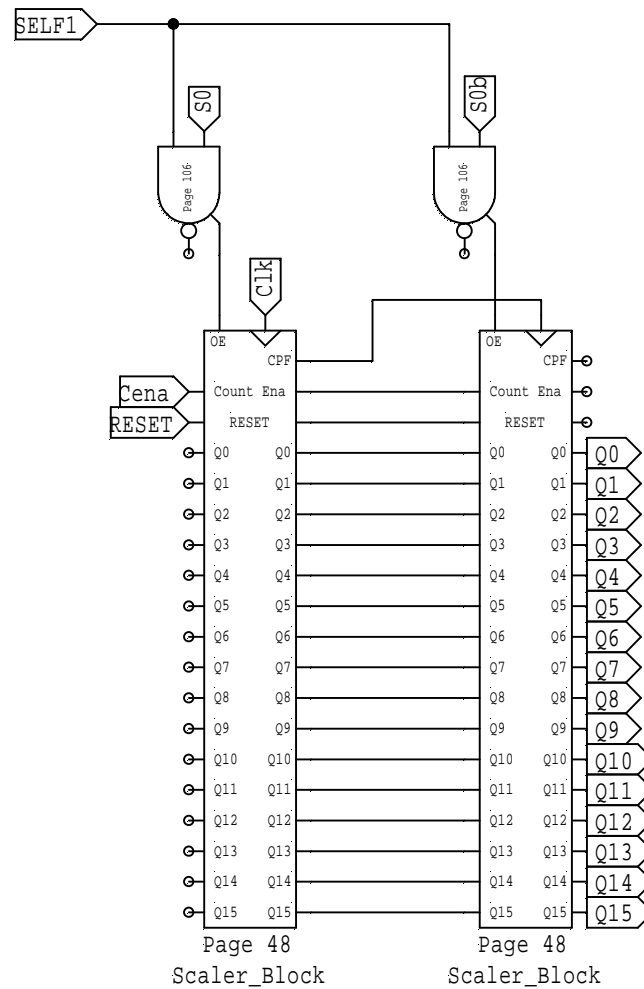
Include models



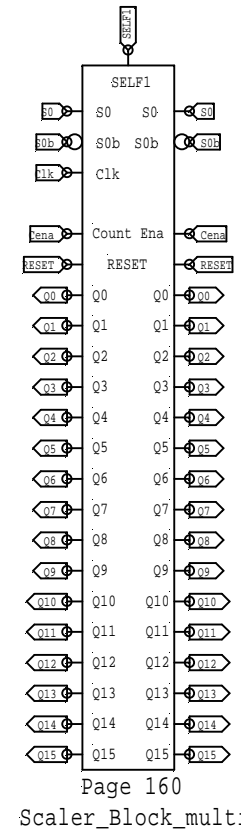
SCA Page 145

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43		Size: 5x7	
Modified: Oct 15, 2002 06:58:29		Rev A	
Info: A/M 12-bit Bus select			
Designer: Dr. Gary S. Varner			
Module: DACAMUX_32		Page: Page 0	
Path: C:\CustomIC\STRAW3\STRAW3			

A pair of 16-bit Scalers (Scaler_Block_multi)
 {forms 31 bit combined scaler count}



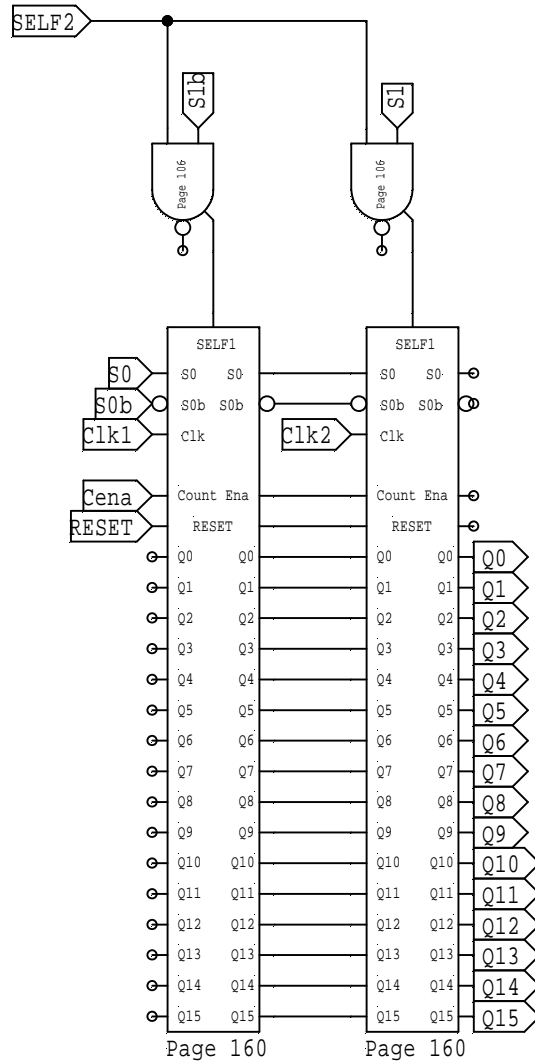
NOTE!!!
 For consistency, High count
 is in low address position



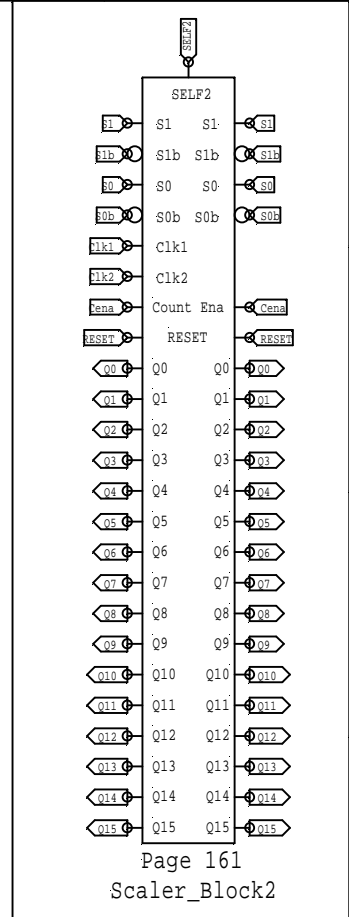
Page 160

University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created: \${Created}	Size: 5x7
Modified: \${Modified}	Rev A
Info: \${Info}	
Designer: \${Author}	
Module: \${Module}	Page: \${Page}
Path: \${File}	

A pair of 32-bit Scalers (Scaler_Block2)



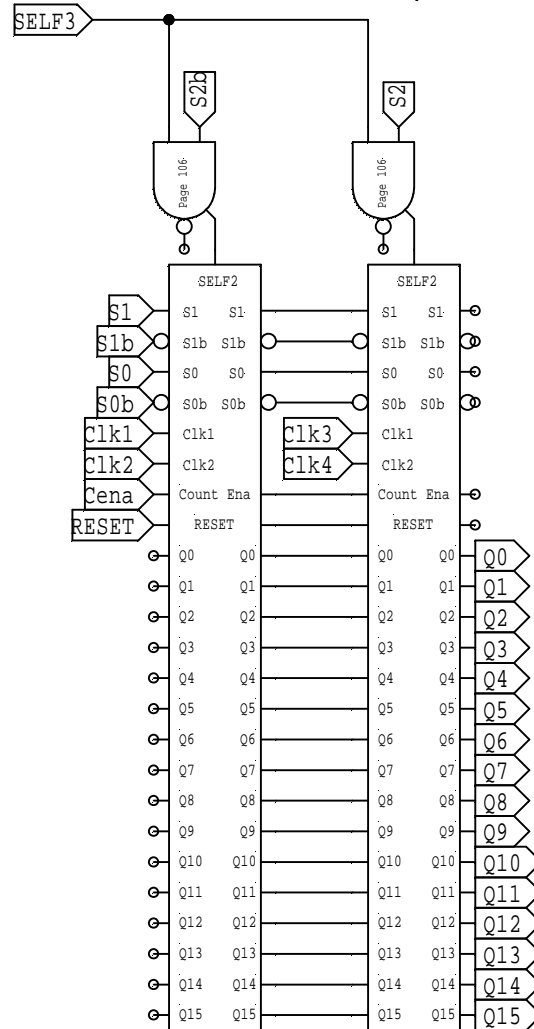
Scaler_Block_multi Scaler_Block2



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University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created:\$(Created)		Size: 5x7	
Modified:\$(Modified)		Rev A	
Info:\$(Info)			
Designer:\$(Author)			
Module:\$(Module)		Page:\$(Page)	
Path:\$(File)			

A quad of 16-bit Scalers (Scaler_Block4)

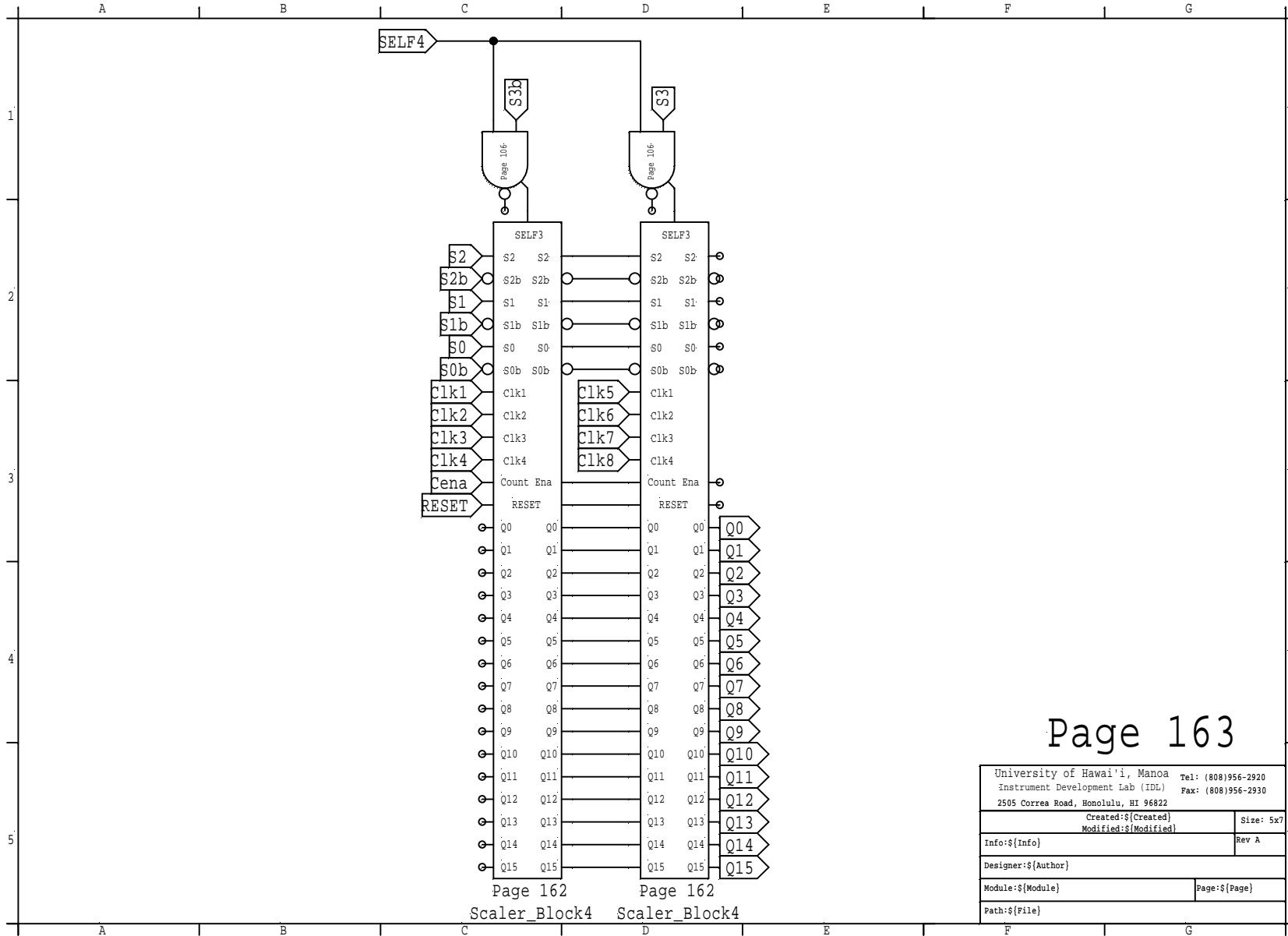


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Scaler_Block2 Scaler_Block2

Page 162

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: \${Created}		Size: 5x7	
Modified: \${Modified}		Rev A	
Info: \${Info}			
Designer: \${Author}			
Module: \${Module}		Page: \${Page}	
Path: \${File}			

An octal of 16-bit Scalers (Scaler_Block8)

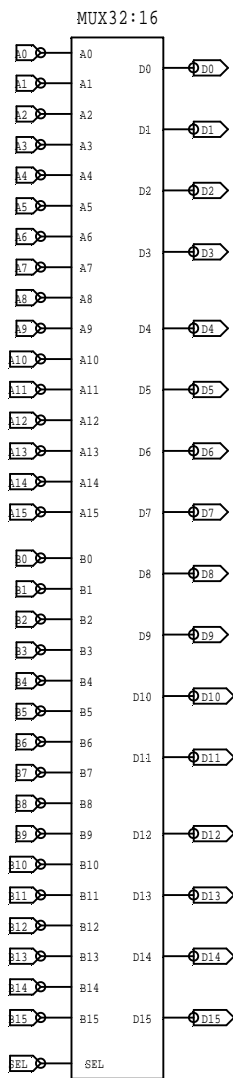


Page 163

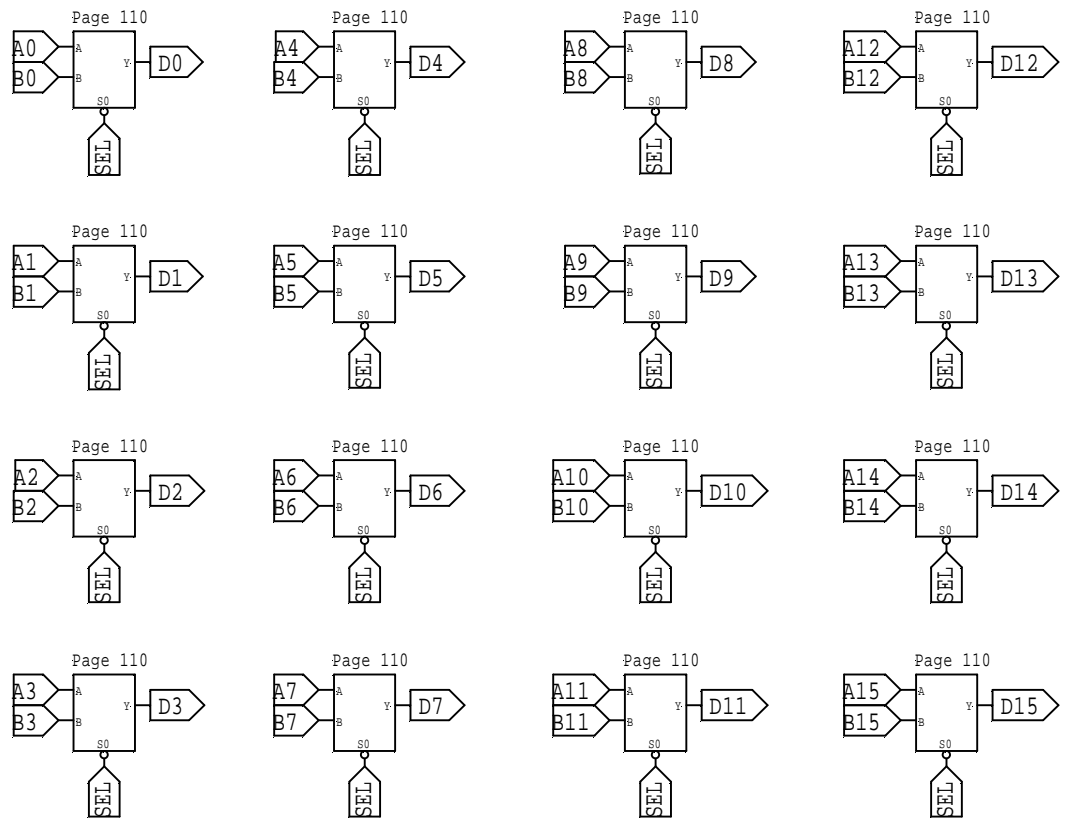
University of Hawai'i, Manoa		Tel: (808)956-2920
Instrument Development Lab (IDL)		Fax: (808)956-2930
2505 Correa Road, Honolulu, HI 96822		
Created: \${Created}	Size: 5x7	
Modified: \${Modified}	Rev A	
Info: \${Info}		
Designer: \${Author}		
Module: \${Module}	Page: \${Page}	
Path: \${File}		

A B C D E F G

16-bit bus select (mux16)



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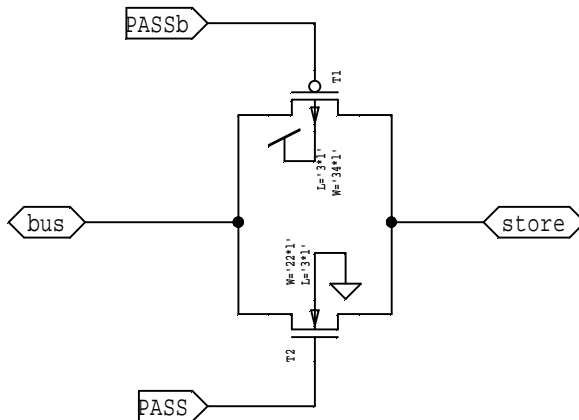
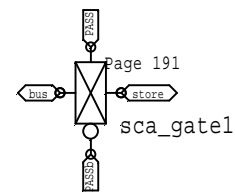
STRAW3 Page 177

S=0 ==> B; S=1 ==> A

University of Hawai'i, Manoa		tel: (808)956-2920
Instrument Development Lab (IDL)		Fax: (808)956-2930
2505 Correa Road, Honolulu, HI 96822		
Created: May 5, 1993 21:36:43	Size: 5x7	
Modified: Sep 4, 2003 11:13:45	Rev A	
Info: A/M 12-bit Bus select		
Designer: Dr. Gary S. Varner		
Module: mux16	Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3		

A B C D E F G

SCA Pass Transistor (sca_gate1)



STRAW3 HF version

Include models

```

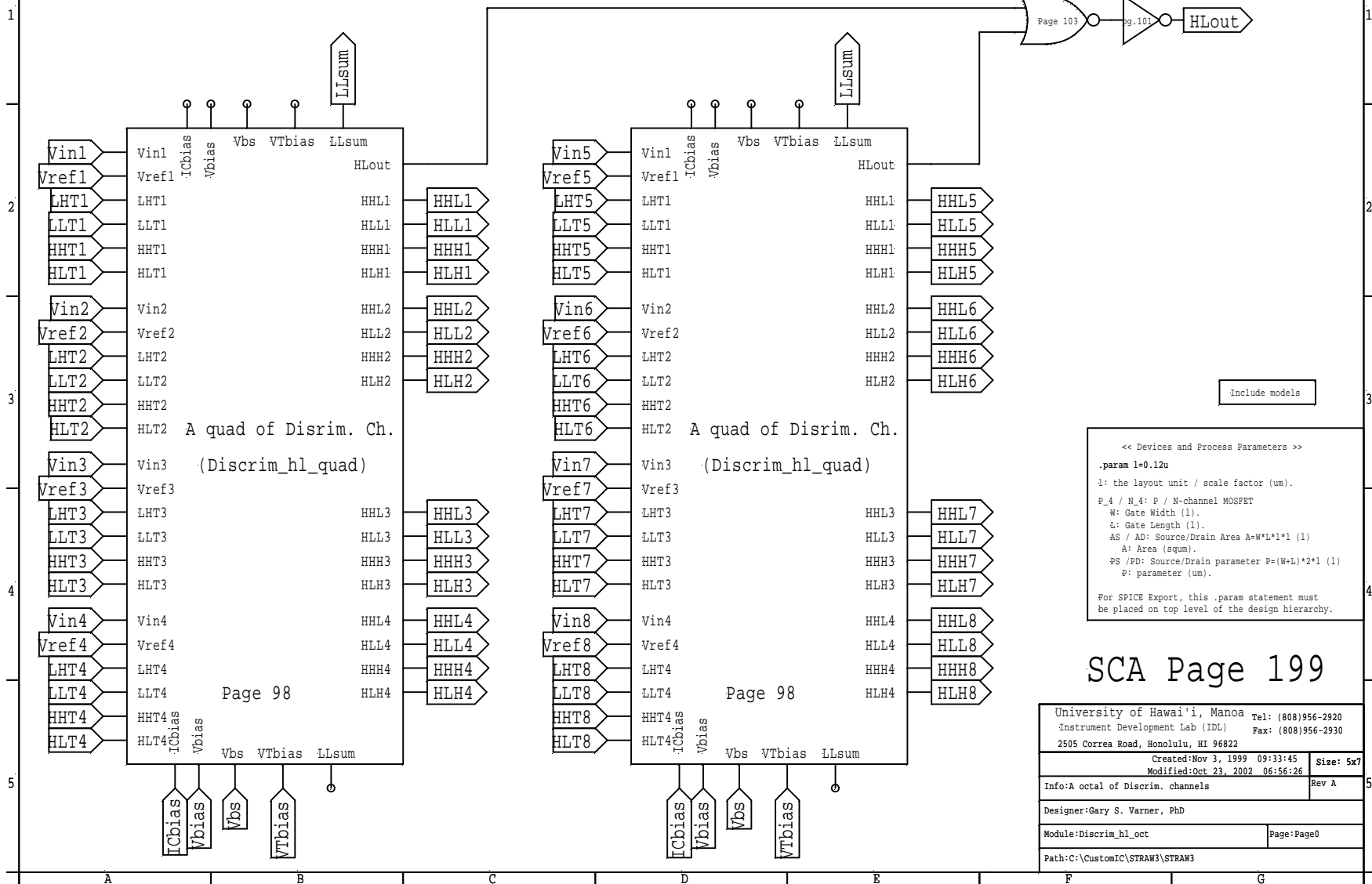
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

SCA Page 191

University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created: \${Created}	Size: 5x7
Modified: \${Modified}	Rev A
Info: \${Info}	
Designer: \${Author}	
Module: \${Module}	Page: \${Page}
Path: \${File}	

Set of 8 Discrim blocks (Discrim_hl_oct)



include models

```

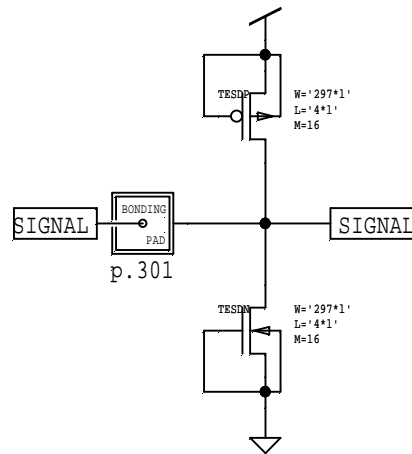
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

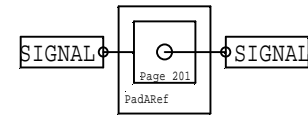
SCA Page 199

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: Nov 3, 1999 09:33:45	Size: 5x7		
Modified: Oct 23, 2002 06:56:26	Rev A		
Info: A octal of Discrim. channels			
Designer: Gary S. Varner, PhD			
Module: Discrim_hl_oct		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

PadARef



Include models



```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

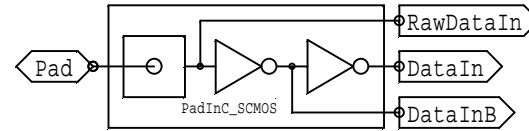
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

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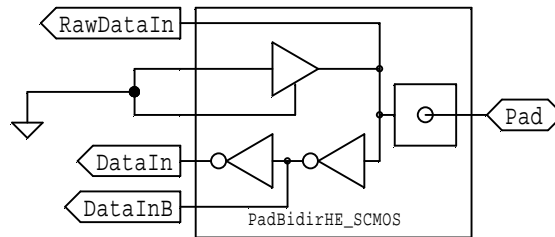
University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993	21:36:43	Size: 5x7	
Modified: Sep 6, 2003	08:31:22		
Info: Modified MOSIS AMI/HP 0.5um Hi-ESD Pad Lib		Rev A	
Designer: Gary S. Varner			
Module: PadARef		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

PadInC

Page 202



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Page 202

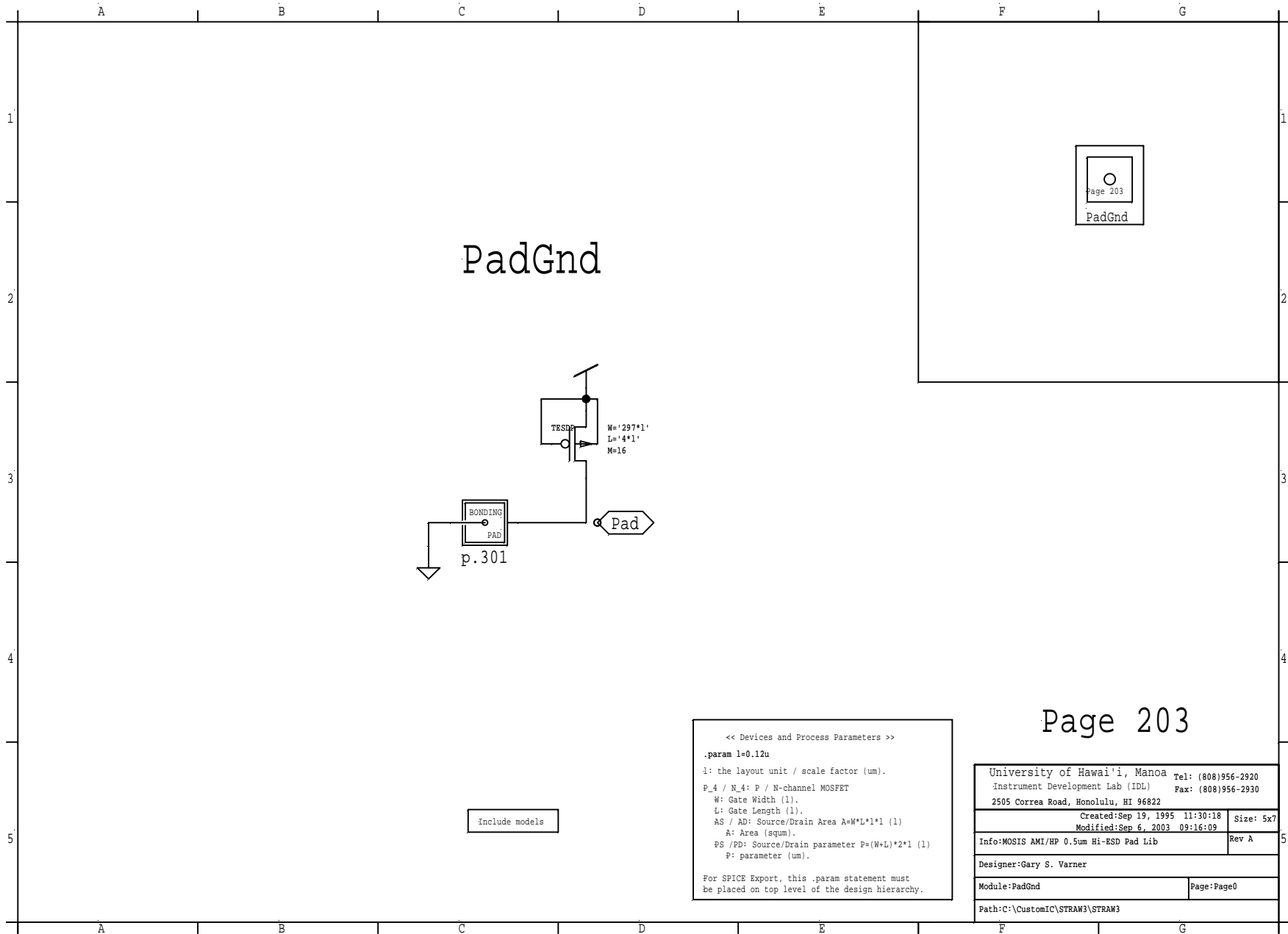
Include models

```

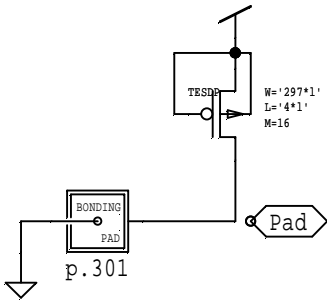
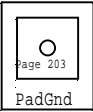
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (1).
L: Gate Length (1).
AS / AD: Source/Drain Area A=W*L*1 (1)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (1)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43		Size: 5x7	
Modified: Sep 6, 2003 09:16:09		Rev A	
Info: MOSIS AMI/HP 0.5um Hi-ESD Pad Lib			
Designer: Gary S. Varner			
Module: PadInC		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			



PadGnd



```

<< Devices and Process Parameters >>

.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (1).
L: Gate Length (1).
AS / AD: Source/Drain Area A=W*L*1*1 (1)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (1)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.

```

Include models

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University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: Sep 19, 1995 11:30:18		Size: 5x7	
Modified: Sep 6, 2003 09:16:09		Rev A	
Info: MOSIS AMI/HP 0.5um Hi-ESD Pad Lib			
Designer: Gary S. Varner			
Module: PadGnd		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

A B C D E F G

1

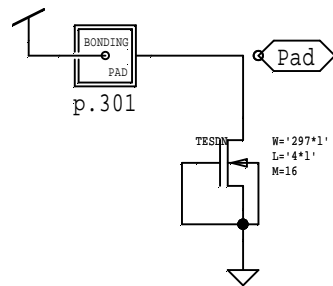
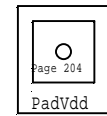
2

3

4

5

PadVdd



Include models

```

<< Devices and Process Parameters >>

.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.

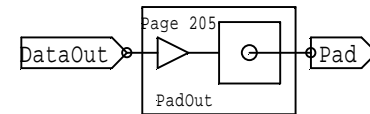
```

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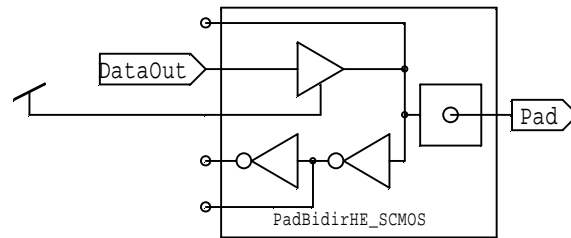
University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: Sep 19, 1995 11:35:20		Size: 5x7	
Modified: Sep 6, 2003 09:16:09		Rev A	
Info: MOSIS AMI/HP 0.5um Hi-ESD Pad Lib			
Designer: Gary S. Varner			
Module: PadVdd		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

A B C D E F G

PadOut



Page 210



Include models

```

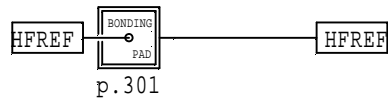
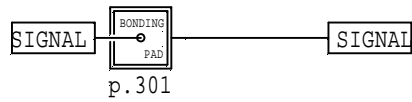
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

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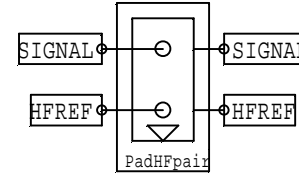
University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: Sep 15, 1995 09:05:31		Size: 5x7	
Modified: Sep 6, 2003 08:11:05		Rev A	
Info: MOSIS AMI/HP 0.5um Hi-ESD Pad Lib			
Designer: Gary S. Varner			
Module: PadOut		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

PadHFpair



Include models

Page 208



```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*l (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*l (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

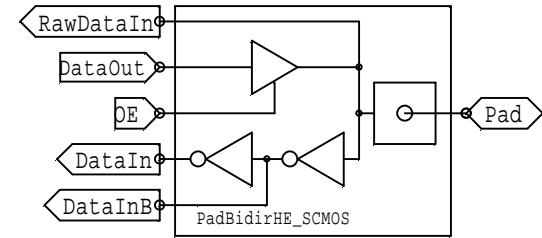
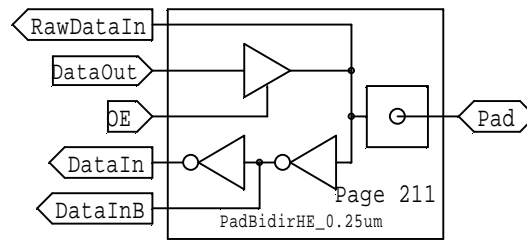
Page 208

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43		Size: 5x7	
Modified: Sep 6, 2003 08:31:22		Rev A	
Info: High Frequency (microstrip) 50 Ohm input			
Designer: Dr. Gary S. Varner			
Module: PadHFpair		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

Bidirectional Pad

This module is the technology independent implementation of the Bidirectional Pad. It can be used for TPR, however it contains no information for exporting to Spice. In order to specify a technology for exporting to Spice, instance the appropriate PadBidirHE below.

Include models



```

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

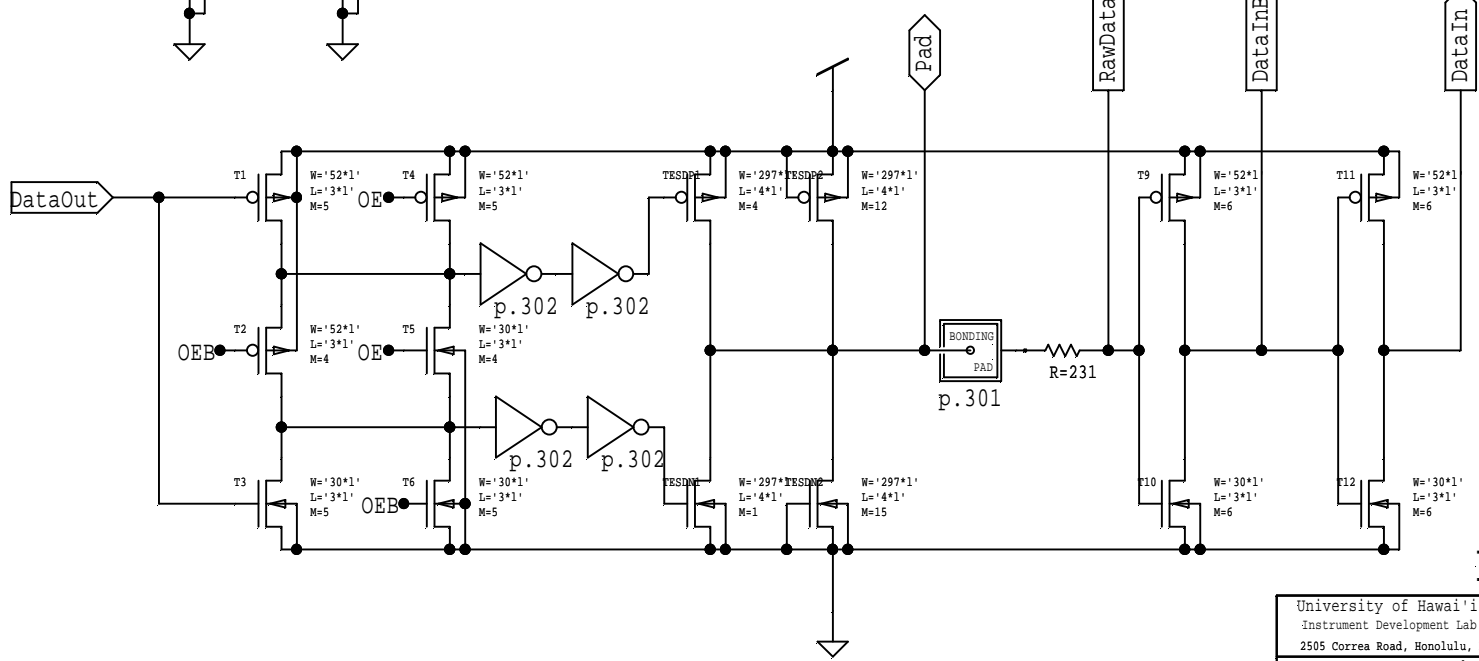
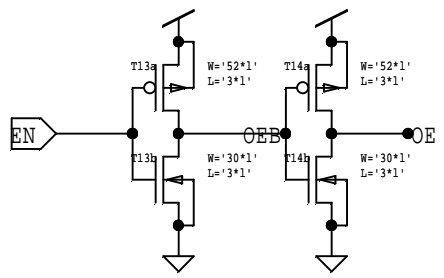
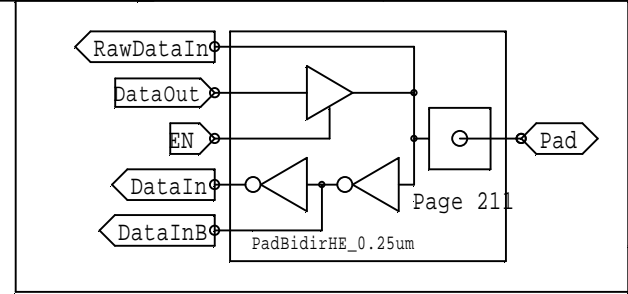
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

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University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993	21:36:43	Size: 5x7	
Modified: Sep 6, 2003	09:16:09	Rev A	
Info: MOSIS AMI/HP Hi-ESD Pad Lib			
Designer: Dr. Gary S. Varner			
Module: PadBidirHE		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

Hi-ESD Bidirectional Pad TSMC 0.25u MOSIS Technology

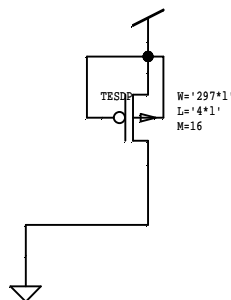
This pad can be used either for TPR export or for Spice export.



University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: May 5, 1993 21:36:43	Size: 5x7		
Modified: Sep 6, 2003 09:16:09	Rev A		
Info: 0.25um Bi-directional digital pad			
Designer: Dr. Gary S. Varner			
Module: Pad_BidirHE_0.25u		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

PadGndNC

Padless Ground Connect Spacer



Include models

```

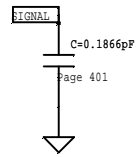
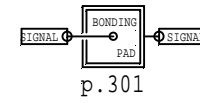
<< Devices and Process Parameters >>

.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (1).
L: Gate Length (1).
AS / AD: Source/Drain Area A=W*L*1 (1)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (1)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
    
```

University of Hawai'i, Manoa		Tel: (808)956-2920	
Instrument Development Lab (IDL)		Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created: Sep 19, 1995 11:30:18		Size: 5x7	
Modified: Sep 6, 2003 08:31:22		Rev A	
Info: Synthesized padless spacer			
Designer: Gary S. Varner			
Module: PadGndNC		Page: Page0	
Path: C:\CustomIC\STRAW3\STRAW3			

Pad_Bond

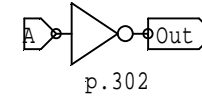
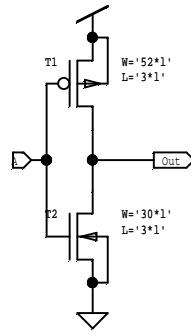


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University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created: Aug 15, 1996 10:36:13	Size: 5x7
Modified: Sep 6, 2003 09:16:09	Rev A
Info: Bonding pad physical definition	
Designer: Dr. Gary S. Varner	
Module: Pad_Bond	Page: Page0
Path: C:\CustomIC\STRAW3\STRAW3	

Generic digital IO Inverter

Inv



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University of Hawai'i, Manoa Tel: (808)956-2920	
Instrument Development Lab (IDL) Fax: (808)956-2930	
2505 Correa Road, Honolulu, HI 96822	
Created: May 5, 1993 21:36:41	Size: 5x7
Modified: Sep 6, 2003 09:16:09	Rev A
Info: Inverter (TIB) for IO Pad	
Designer: Dr. Gary S. Varner	
Module: PadBidir_Inv	Page: Page0
Path: C:\CustomIC\STRAW3\STRAW3	