LABRADOR
preliminary Internal Design Review

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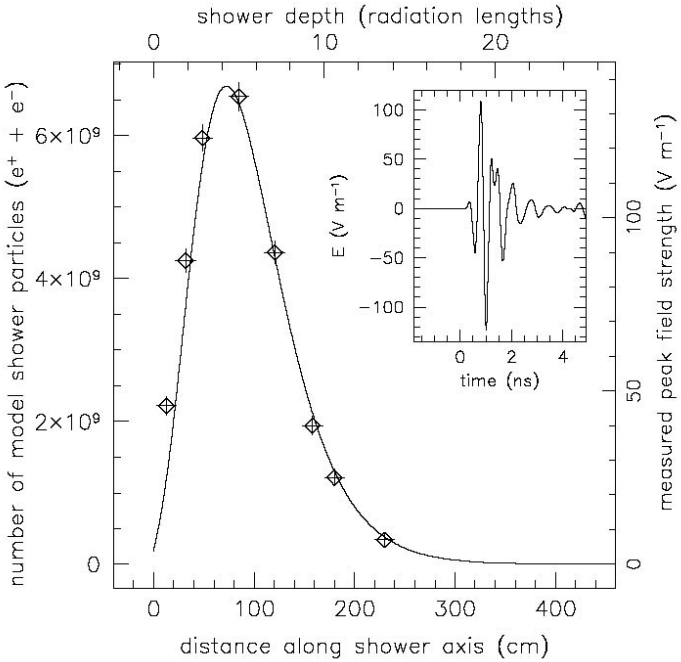
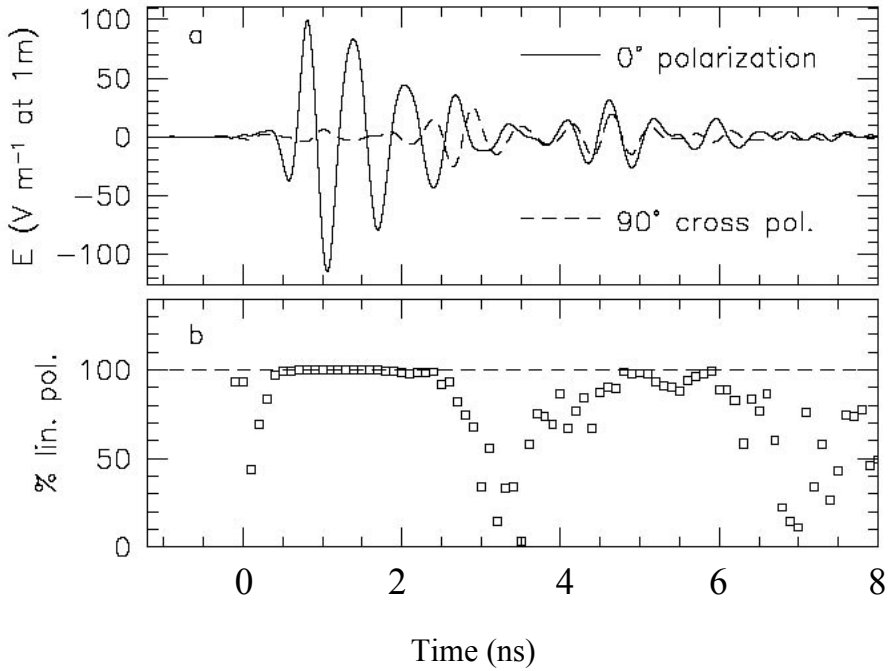
On the whipping post
ID Lab
10 Oct 2003

Topics (1 hour(?) + 1 hour)

- ANITA 'ARF' Architecture
  - Relation to triggering (STRAW3)
  - How parts go together
- LABRADOR
  - Large Analog Bandwidth Recorder And Digitizer with Ordered Readout
  - Design philosophy
  - Improved ADC, readout speed
- Review Items (critical)
  - It's the BandWidth Stupid
    - What learned from STRAW2
    - Engineering Tradeoffs
  - SPICE simulations (RLC)
  - 3-D EM sims (Zeland)

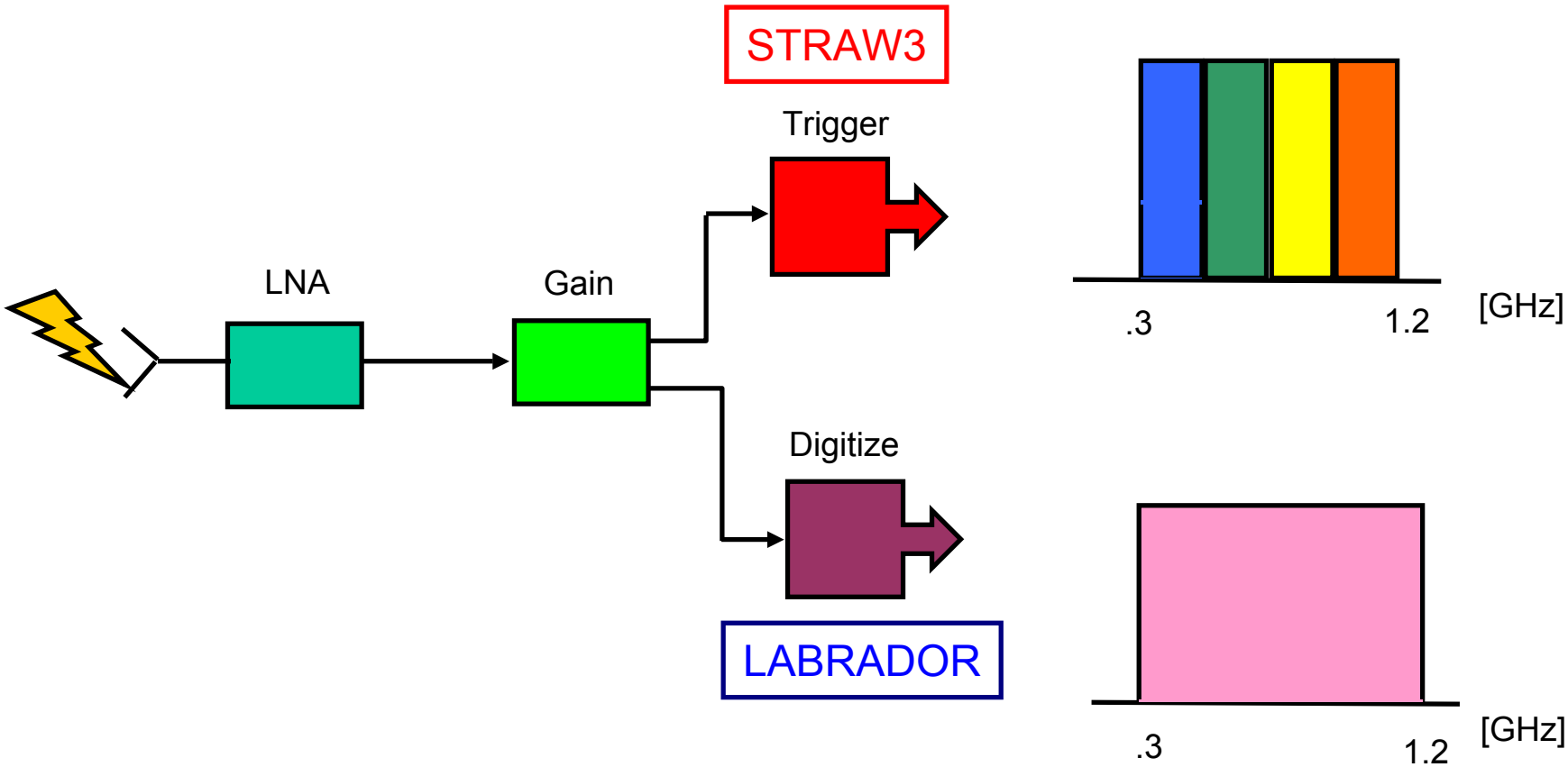
Askaryan Signature



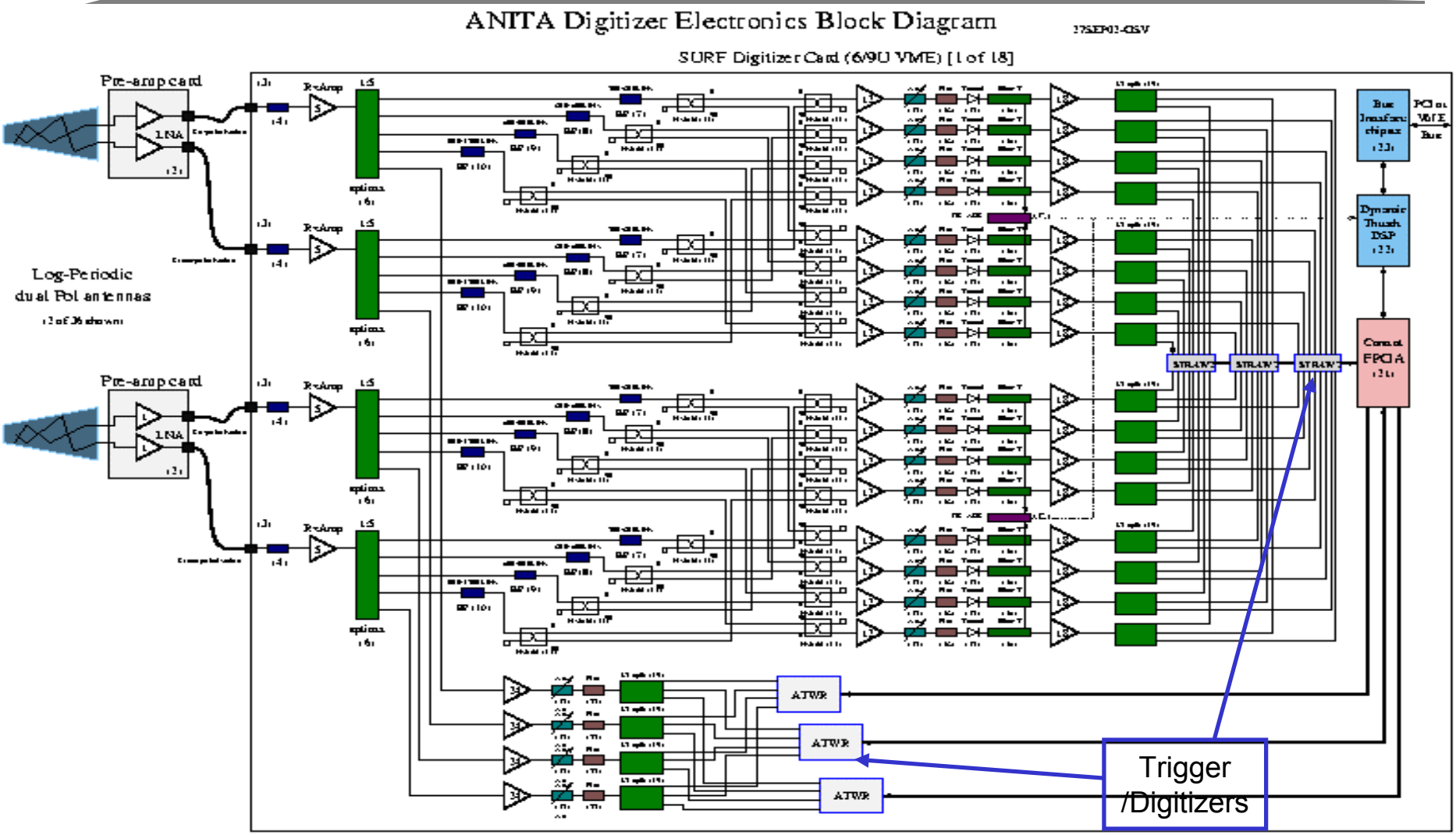


- Significant signal power at large frequencies
- Strong linear polarization (near 100%)

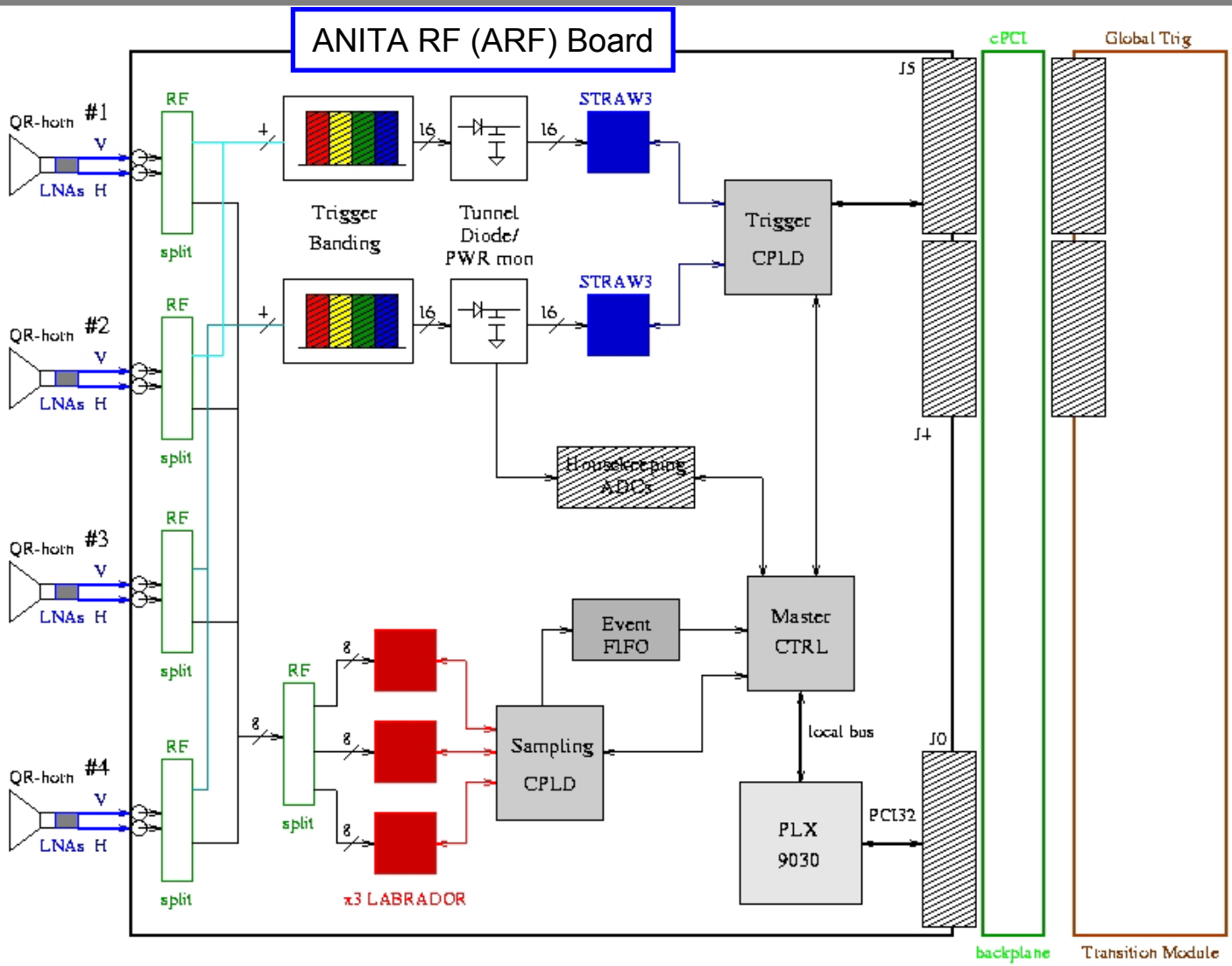
Proposed Signal Flow



Straw Man


ANITA Digitizer Electronics Block Diagram
SURF Digitizer Card (6/9U VME) [1 of 18]
Pre-amp card
LNA
Log-Periodic
dual Pol antennas
ATWR
ATWR
ATWR
Trigger
/Digitizers

August '03 Baseline



LABRADOR Goals

- Maximum input bandwidth
  - 50Ω impedance
  - Simplified architecture (no trigger functionality)
  - "best" RF coupling into Switched Capacitor storage cells
  - Classical engineering trade-offs
    - Input trace resistance vs. load capacitance
    - Storage capacitor kTC noise vs. load capacitance
    - Storage switch R_{on} vs. drain load capacitance
- Analog Transfer
  - Optimum speed
  - Individual channel parallel
- Improved ADC
  - Ramp type – no missing codes
  - Massively parallel to reduce conversion time

Address first

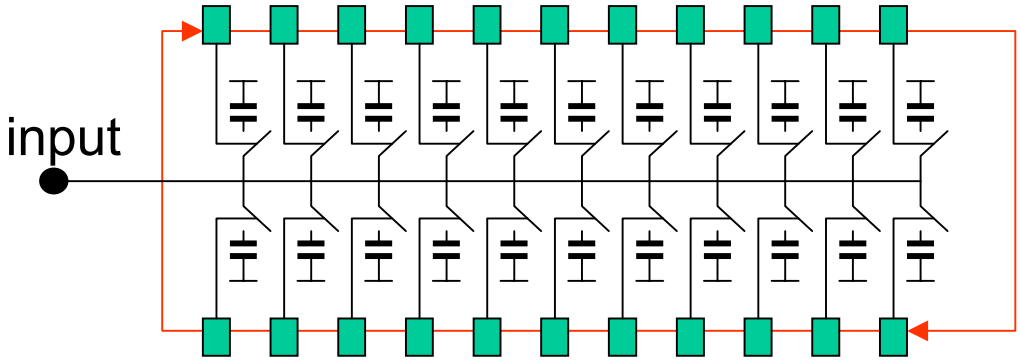
RF Transient Recorder Specs

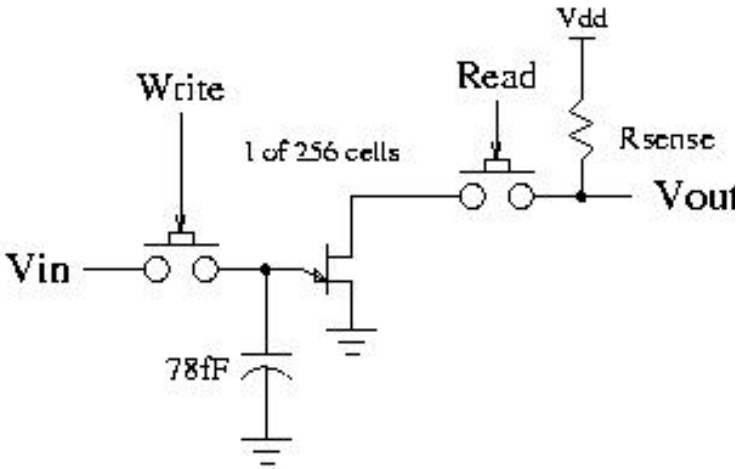
- >= 1GHz analog input bandwidth (200-1200MHz)
- multi-GSa/s sampling rate (Nyquist limit min.)
- minimum phase distortion for clean polarization
- dynamic range (>= 10 bits)
- internal Analog to Digital Conversion (ADC)
- short record length (100-200ns if optimally matched)
- ~~self-triggering with fine threshold adjustment~~
- ~~bi-polar triggering~~
- deadtimeless → conclude multi-hit buffering needed
- LOW POWER!! (need 36(40) * 2 channels)

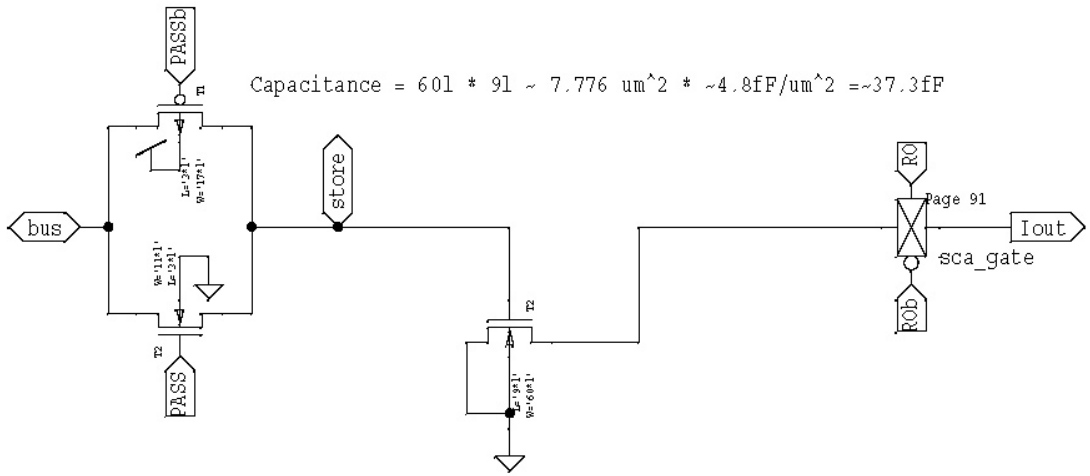
[Acqiris > 1kW] Target: 20W/channel → 20mW/channel

Switched Capacitor Array (SCA)

- Write pointer is ~4-6 gates open @ once

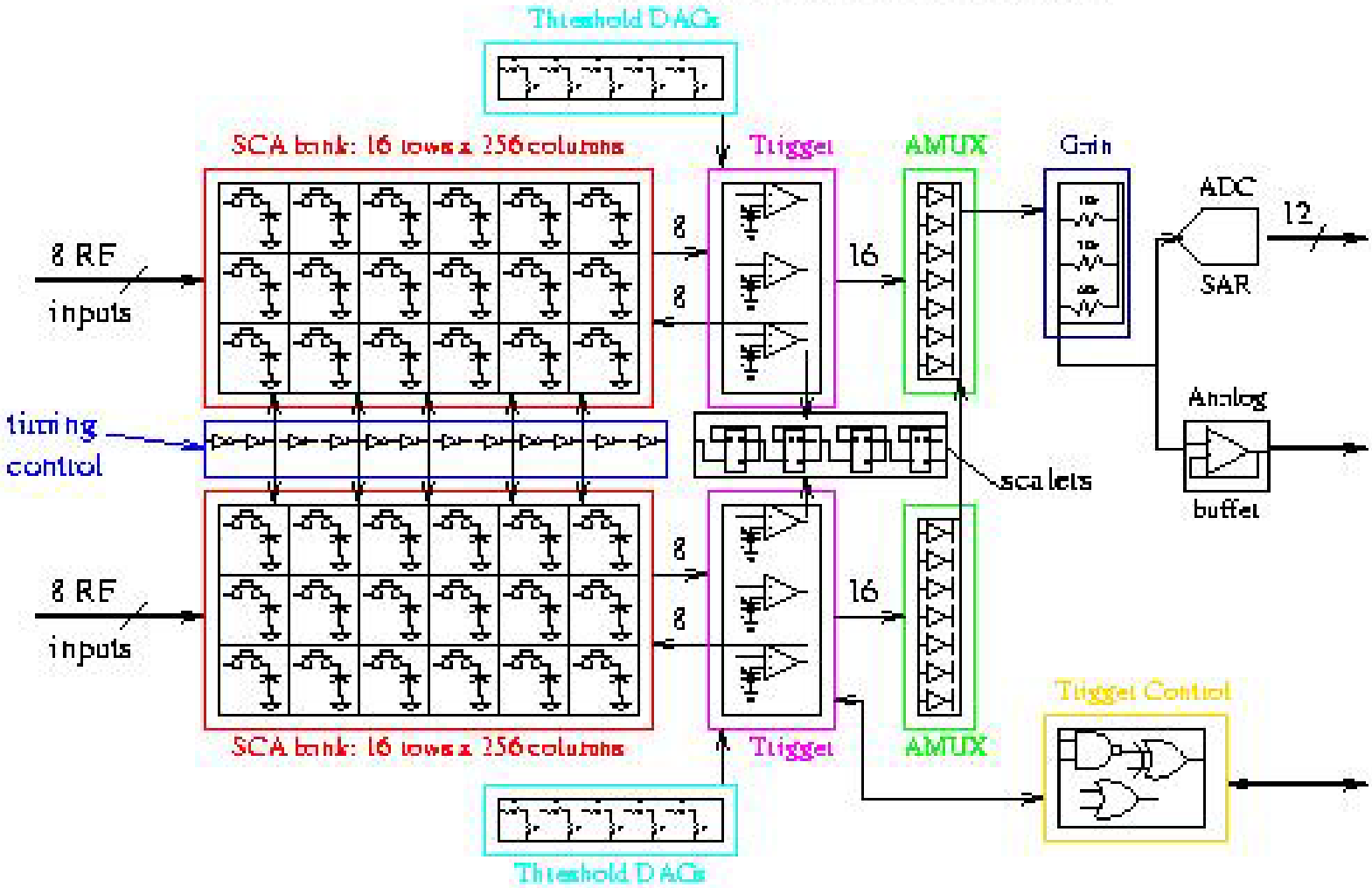






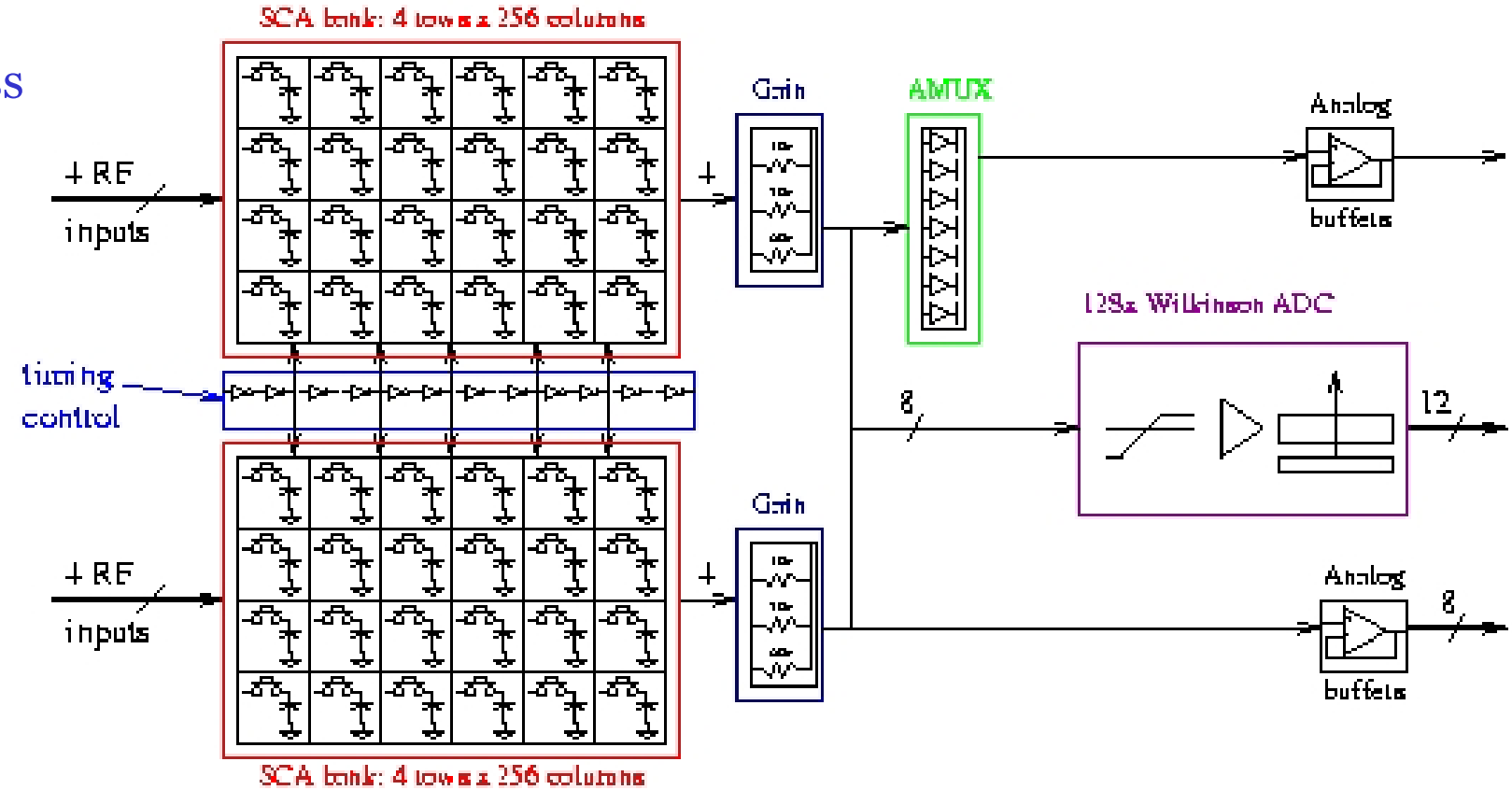
STRAW2/3 Architecture

- 0.25µm TSMC process

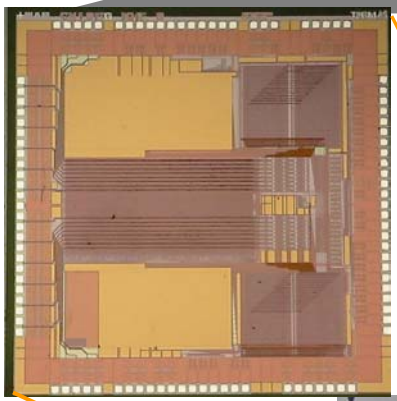


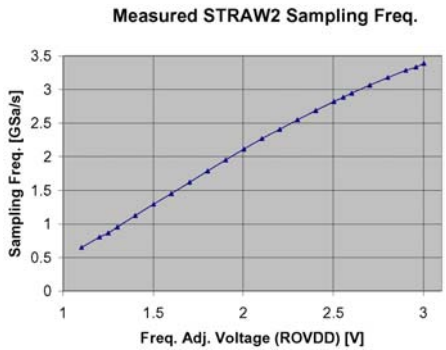
LABRADOR Architecture

- 0.25µm TSMC process



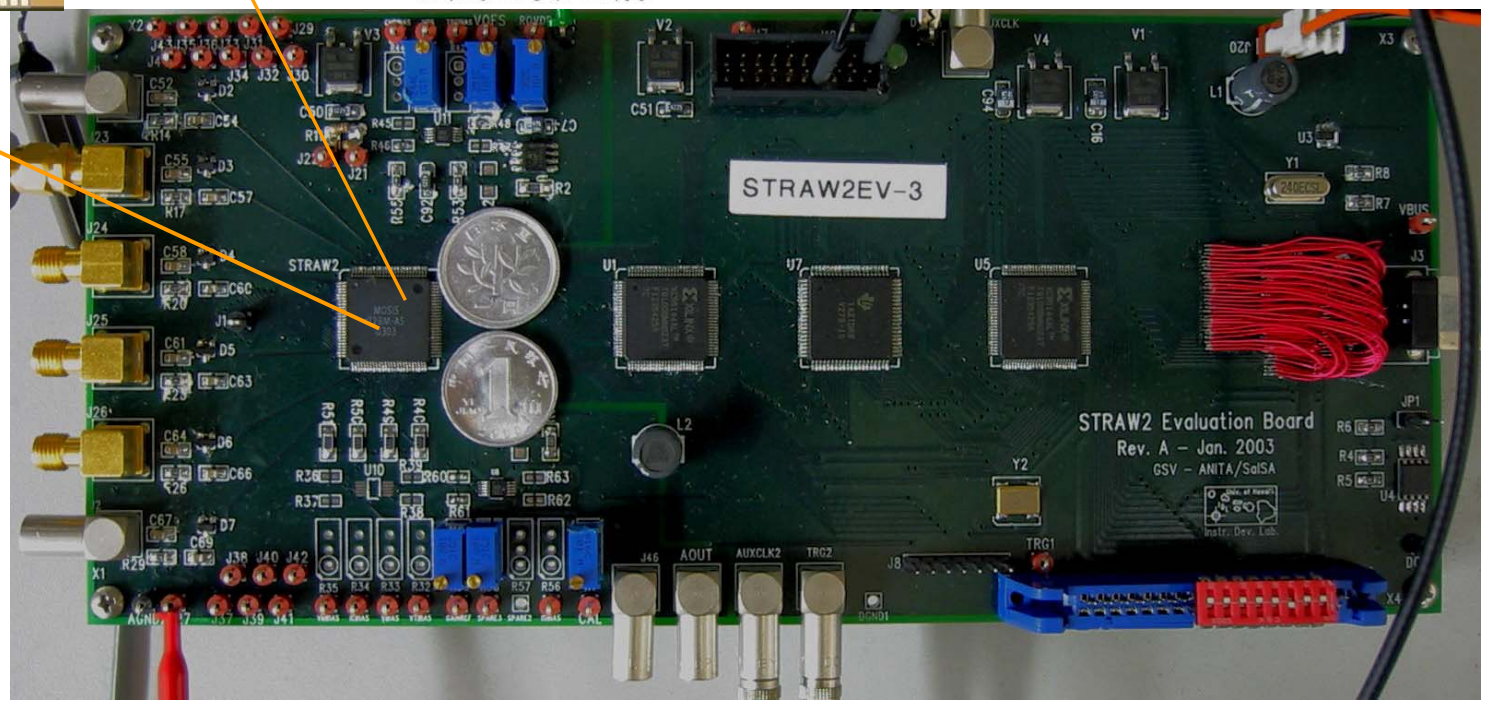
STRAW2 Evaluation



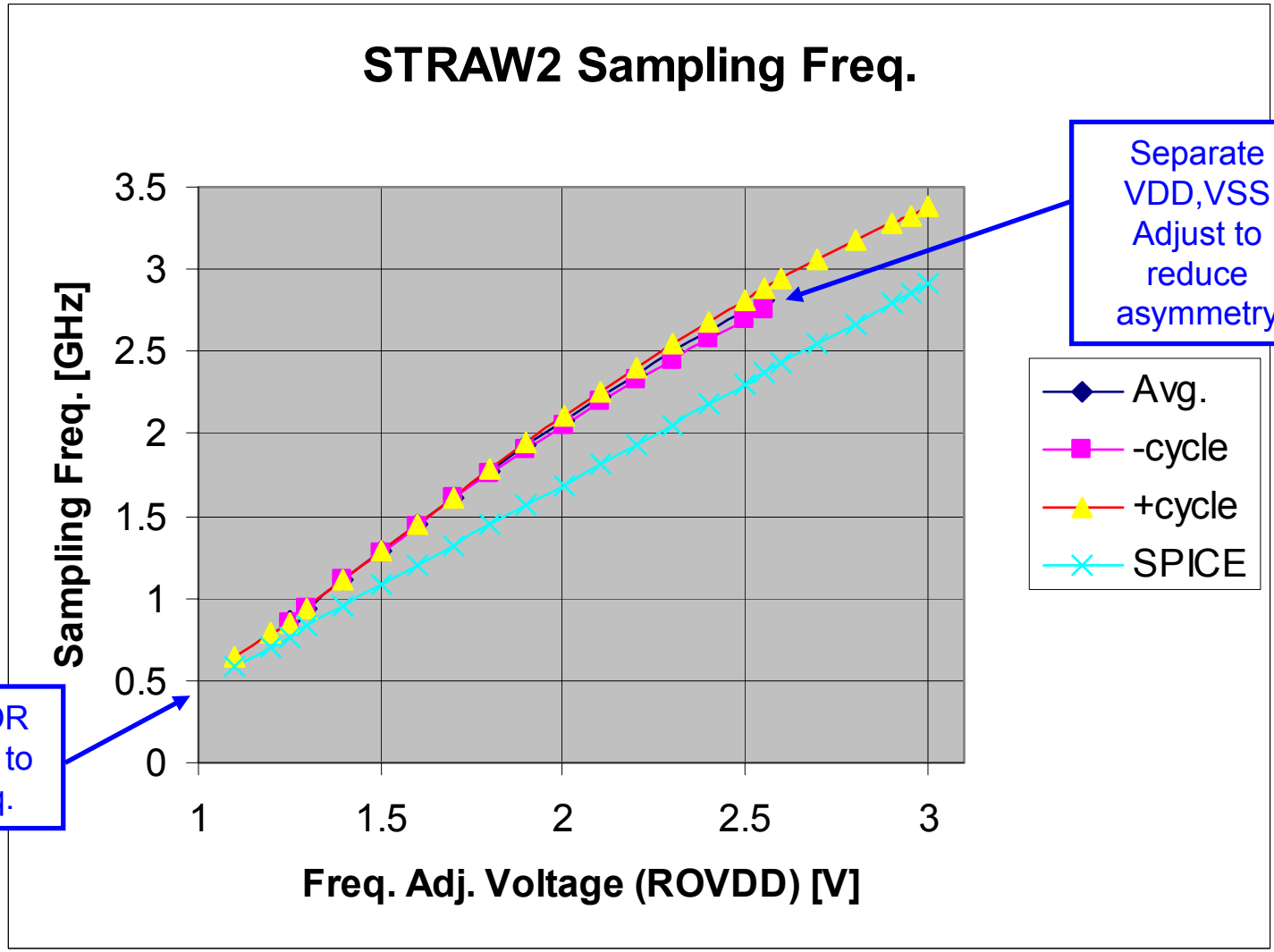


- Adjustable: 0.6 – 3.4 GSa/s
- 256 samples (70 – 300ns)

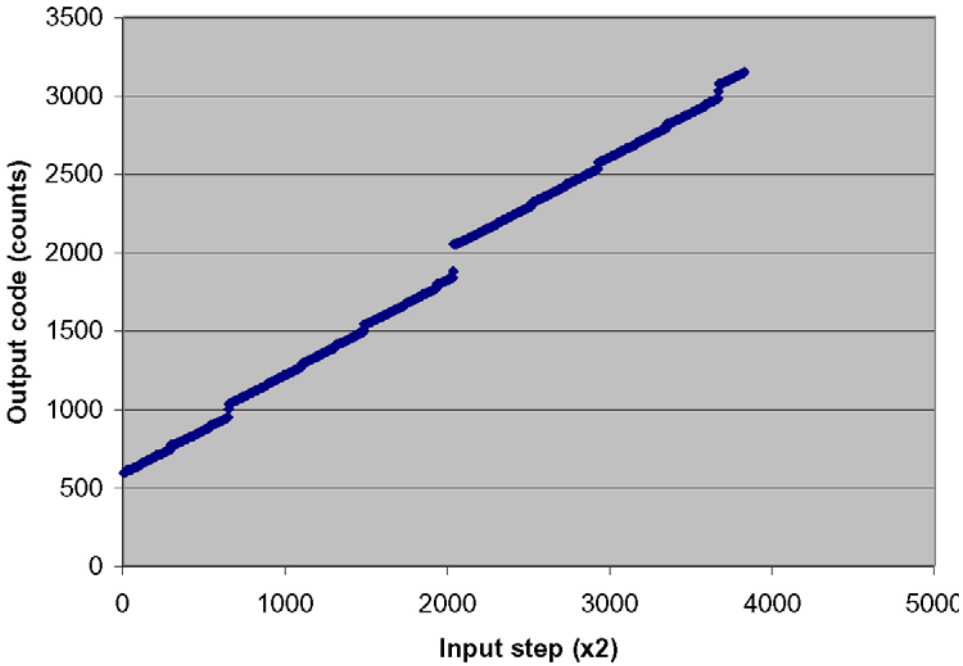
- RF signal input



Better than expected



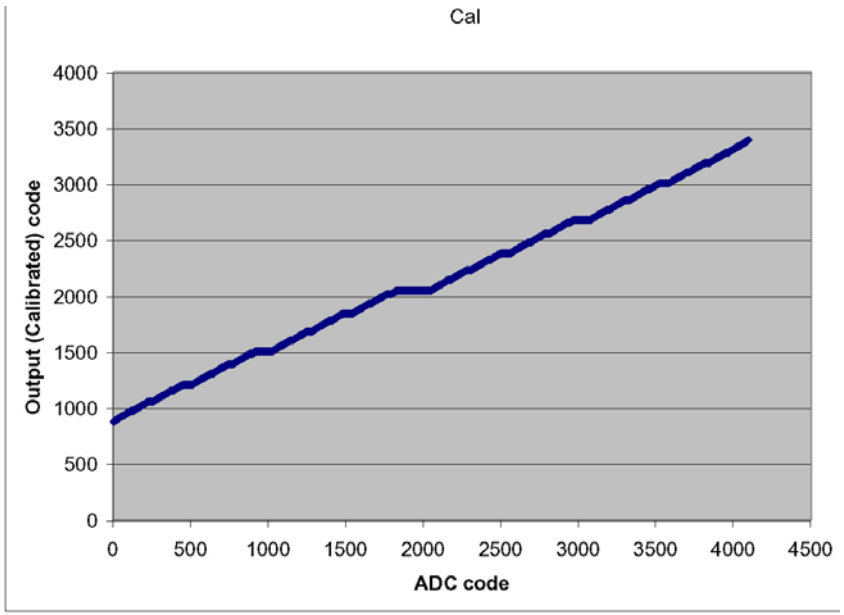
STRAW ADC Expectations



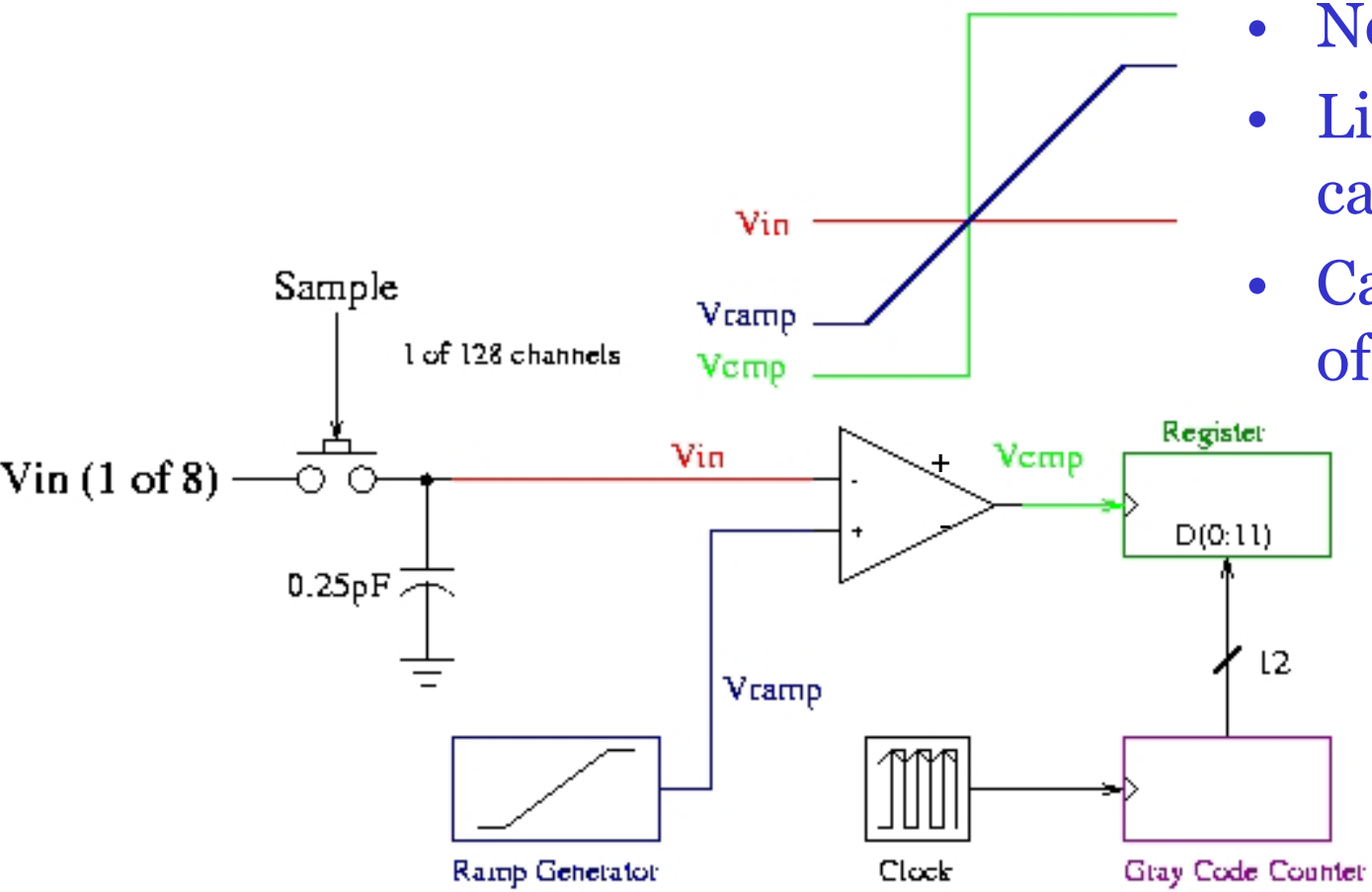
"worst case" for mismatch in a previous implementation of same SAR ADC w/R-2R ladder

Can correct to rather linear, but still differential sensitivity and calibration is a pain

Wilkinson type better – monotonic BUT, slower



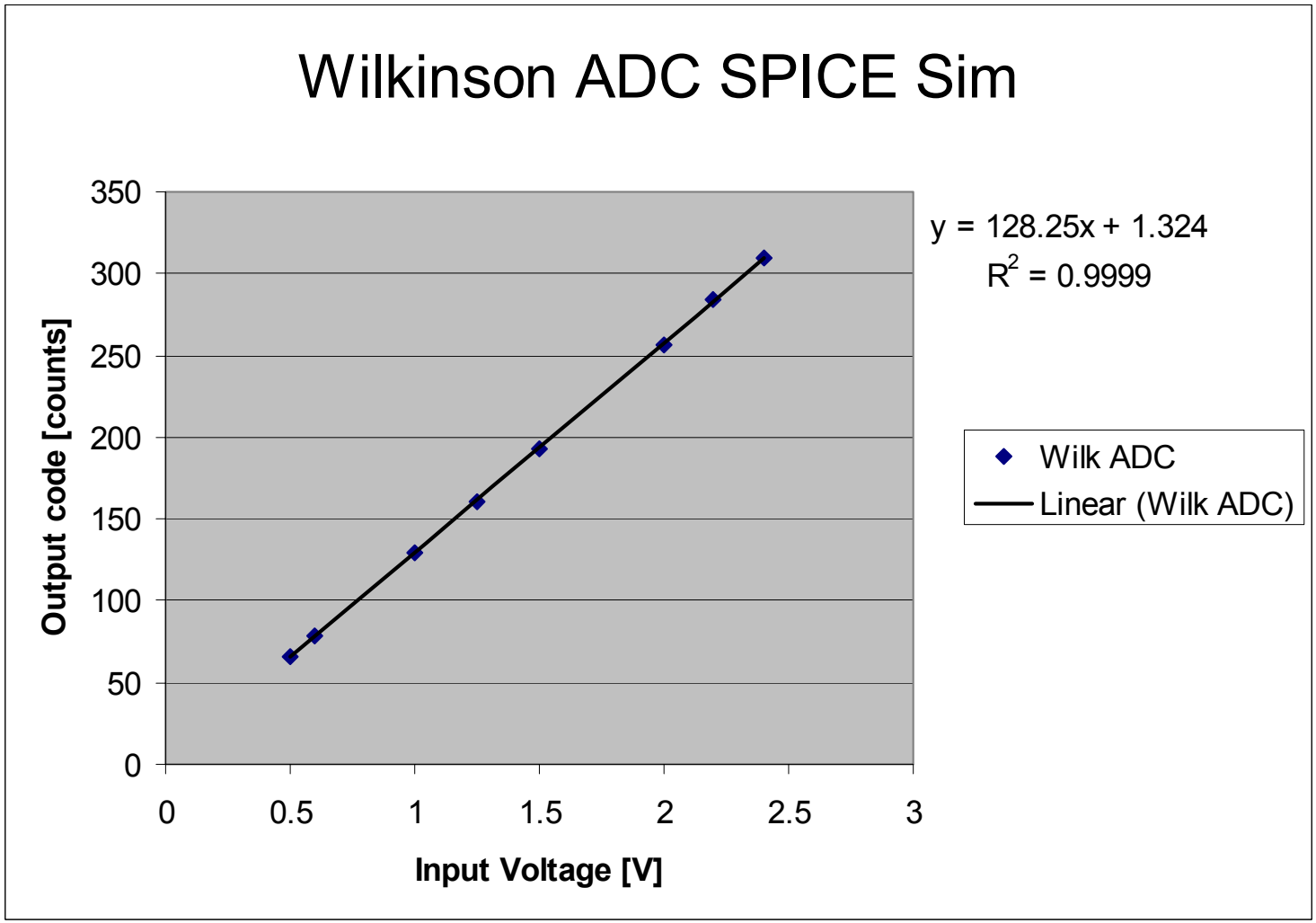
"Wilkinson" ADC



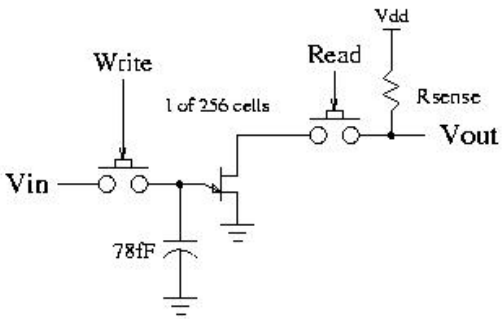
- No missing codes
- Linearity as good as can make ramp
- Can bracket range of interest

NB: SCA output not linear

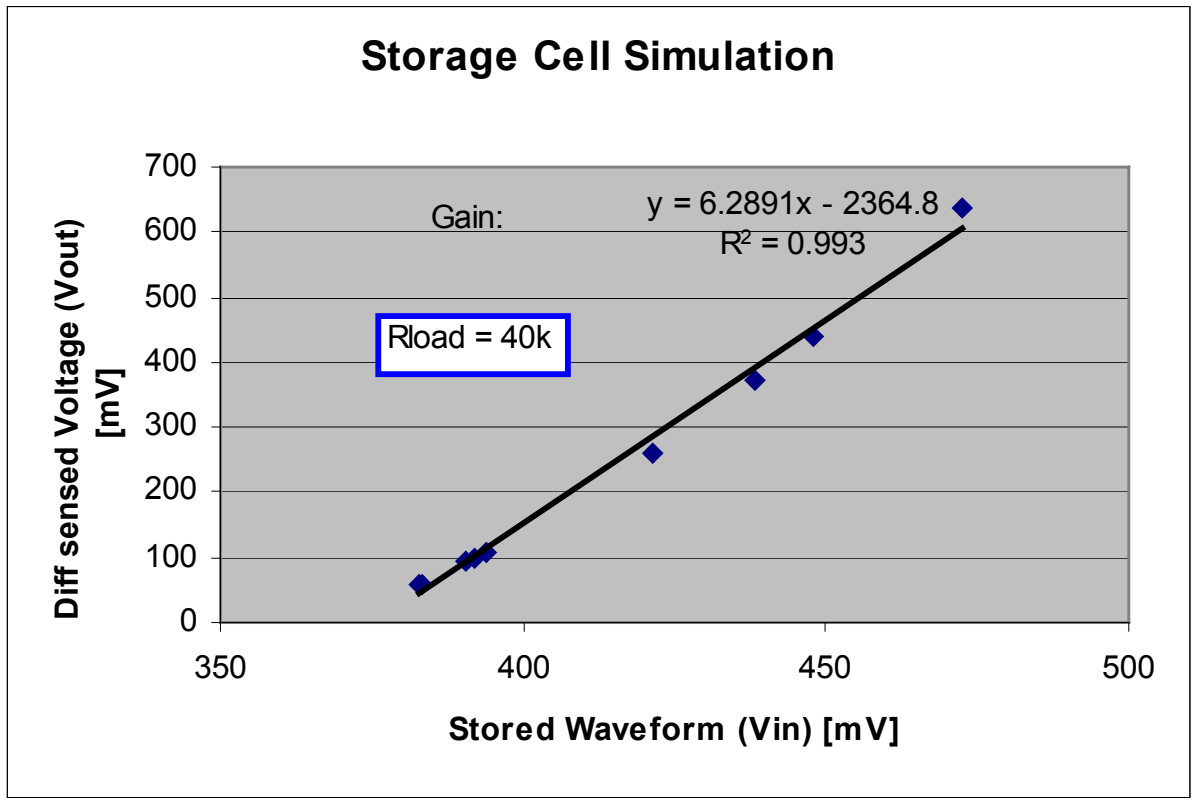
ADC Sim


Wilkinson ADC SPICE Sim
Output code [counts]
350
300
250
200
150
100
50
0
0
0.5
1
1.5
2
2.5
3
Input Voltage [V]
y = 128.25x + 1.324
R2 = 0.9999
Wilk ADC
Linear (Wilk ADC)

Transfer Curve



$$v_{rms} = \sqrt{\frac{kT}{C_{store}}} = 0.23mV$$



Readout speed comparison

IC	ADC	speed	Total Latency	Evt. Size
STRAW2 - GEISER	EXT	8MHz	384 µs	6kB
STRAW2 – DALI	EXT	1MHz	3,072 µs	
STRAW3 -- ARF	INT	2.5MHz	1,638 µs	8kB
STRAW3 -- FINESSE	EXT	10MHz(a)	410 µs	
LABRADOR -- ARF	INT	100kHz(b)	240 µs	4kB
LABRADOR -- serial	EXT	10MHz	210 µs	
LABRADOR -- parallel	EXT	20MHz©	12.8 µs	

(>300MB/s!!)

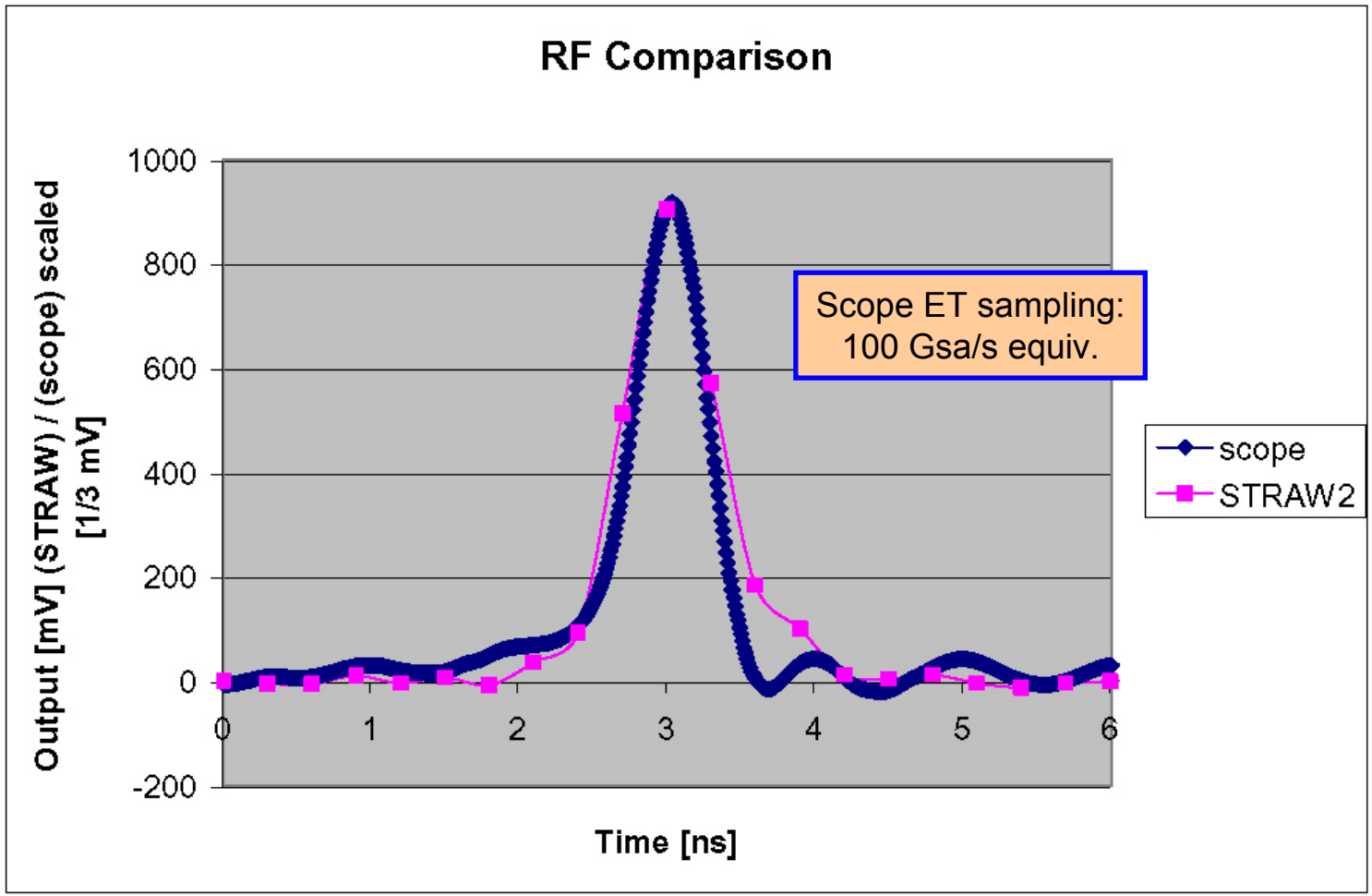
(a) 16 channels for STRAW3, 12 channels for STRAW2

(b) 12.8MHz effective: 128x ADC; 100MHz clock, 12b eff. – includes additional latency

© 8x 20MHz ADC in parallel

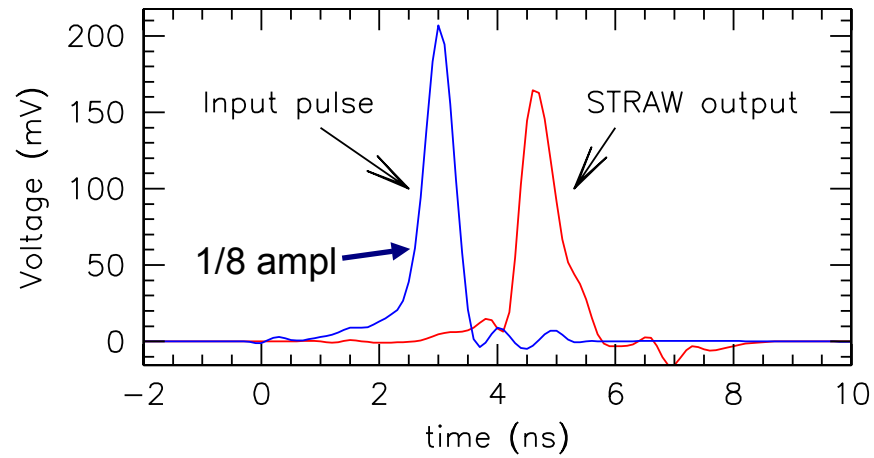
RF Response (1)

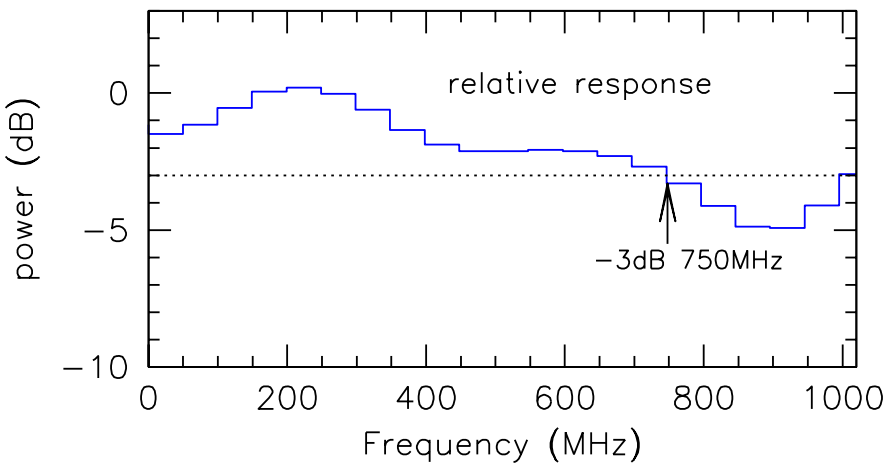
- Sub-ns transient ping: <= 100ps leading edge



RF Response (2)

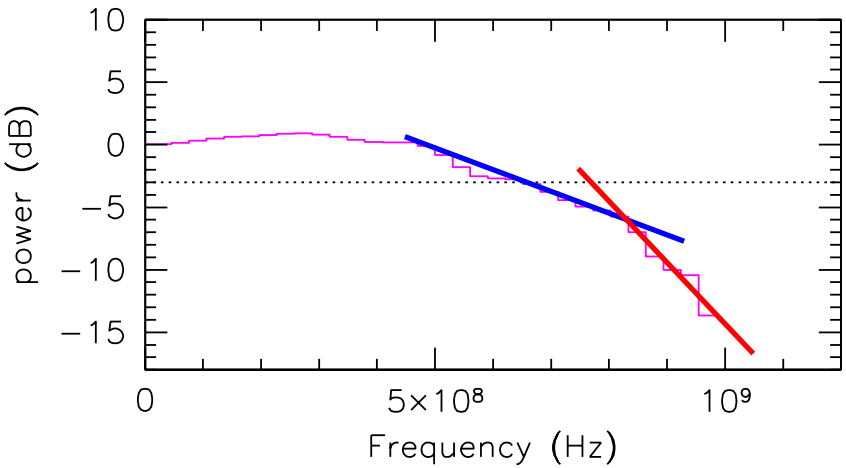
- Very nice tool: FFT analysis of RF transient pulse
- Have ideas how to improve – roll-off matches SPICE simulations of storage cells



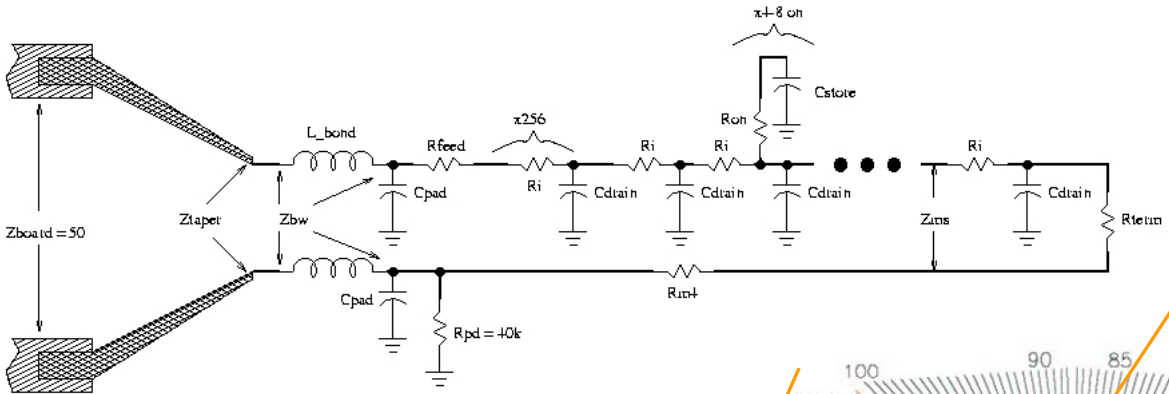


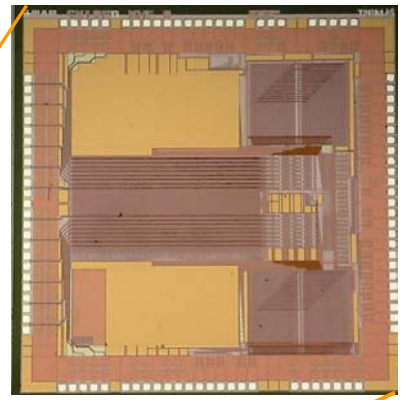
Understanding STRAW2 Performance

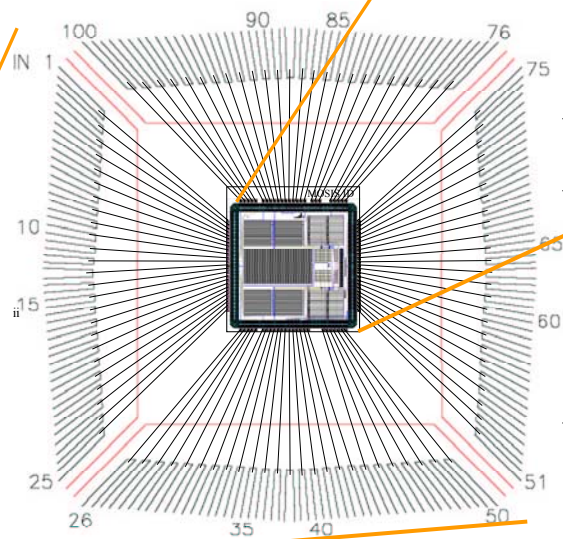
- Contributions considered:
  - Simple Estimates based on R(Z)LC
  - Coupling into package leadframe (TQFP-100)
  - On-chip “stripline”
- What is the real limitation?
  - Cannot rule out multiple contributions (2x poles?)

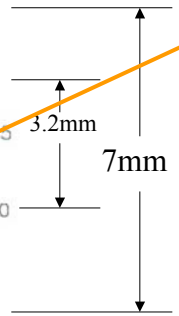


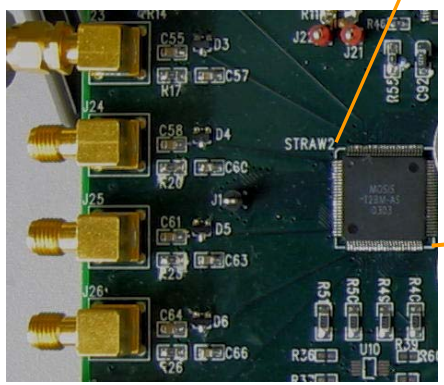
STRAW2 Model





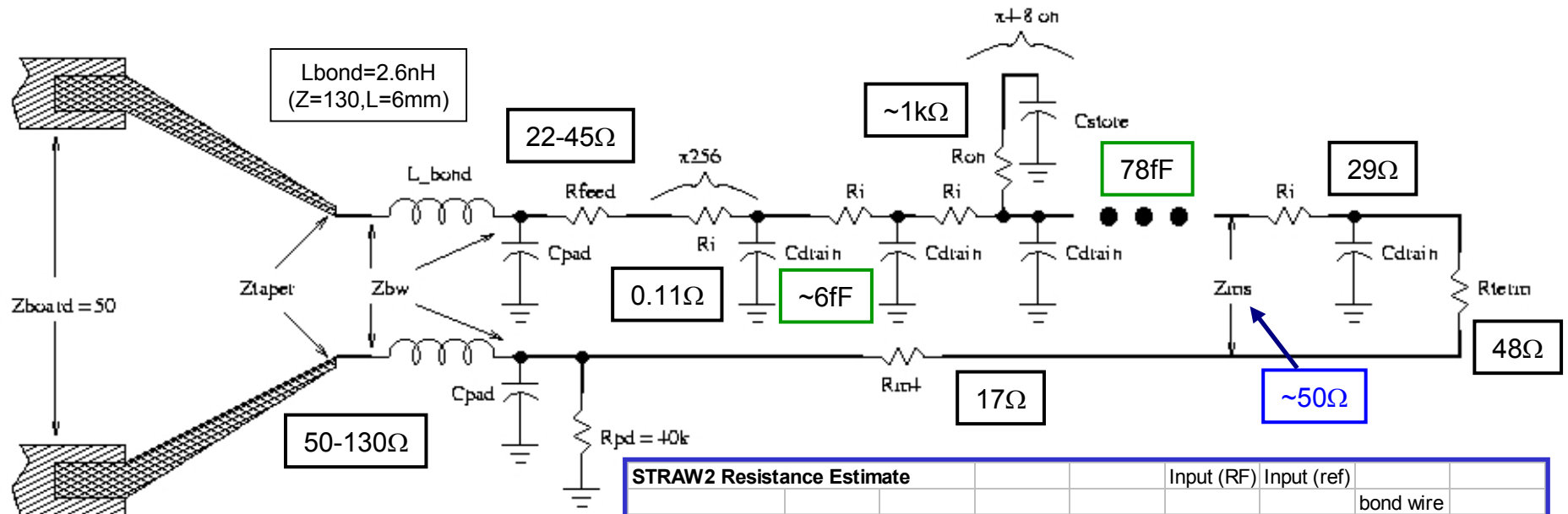




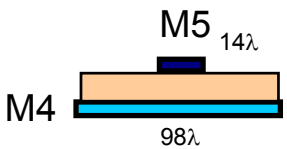


- Micro strip input

STRAW2 Equiv. Ckt.

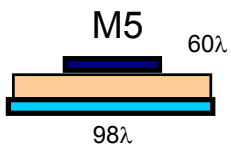


STRAW2



Z~50Ω

STRAW3



Z~30Ω

STRAW2 Resistance Estimate					Input (RF)	Input (ref)	
							bond wire
					0.0	0.1	pad
			70			0.2	M5-M4
Metal 4(sheet) =	0.07	Ohm/sq		243.5		17.0	typ length (sq.)
Metal 5(sheet) =	0.03	Ohm/sq	1704		51.1		typ length (sq.)
Poly contact =	5.1	Ohm	6	6	0.9	0.9	
via 1=	2.7	Ohm	6	3	0.5	0.9	
via 2=	5.35	Ohm	6	3	0.9	1.8	
via 3=	8.26	Ohm	6	3	1.4	2.8	
via 4=	11.34	Ohm	6		1.9		
					56.6	23.6	Total per feed
						48.3	Rterminator
		Measured:	**130**	Ohm		**128.5**	Grand Total

Naïve Calculations –EST.

Component	Length/area	Unit	Factor	Funit	Total [fF]	
Input traces	5	cm	0.2	pF/cm	1000	w.a.g.
bonding wire	150	mil	0.3	pF/wire	300	w.a.g.
input pad	60	um^2	187	fF/pad	187	Tanner
input protection	594	λ	1.1	pF/ckt	1100	SPICE
stripline area	2500	um^2	43	aF/um^2	107.5	MOSIS
stripline fringe	5	mm	60	aF/um	300	MOSIS
Switch Drains	256	switches	5.6	fF/drain	1433.6	SPICE
Open Switches	6	open	87	fF/gate	522	SPICE
TOTAL					**4.9501**	**pF**

$R=R_{feed}$ R~30Ω $C=C_{load}$ C~2.5pF

$$f_{3dB} = \frac{1}{2\pi RC} = 2.1GHz.$$

Bonding wire, series R limit

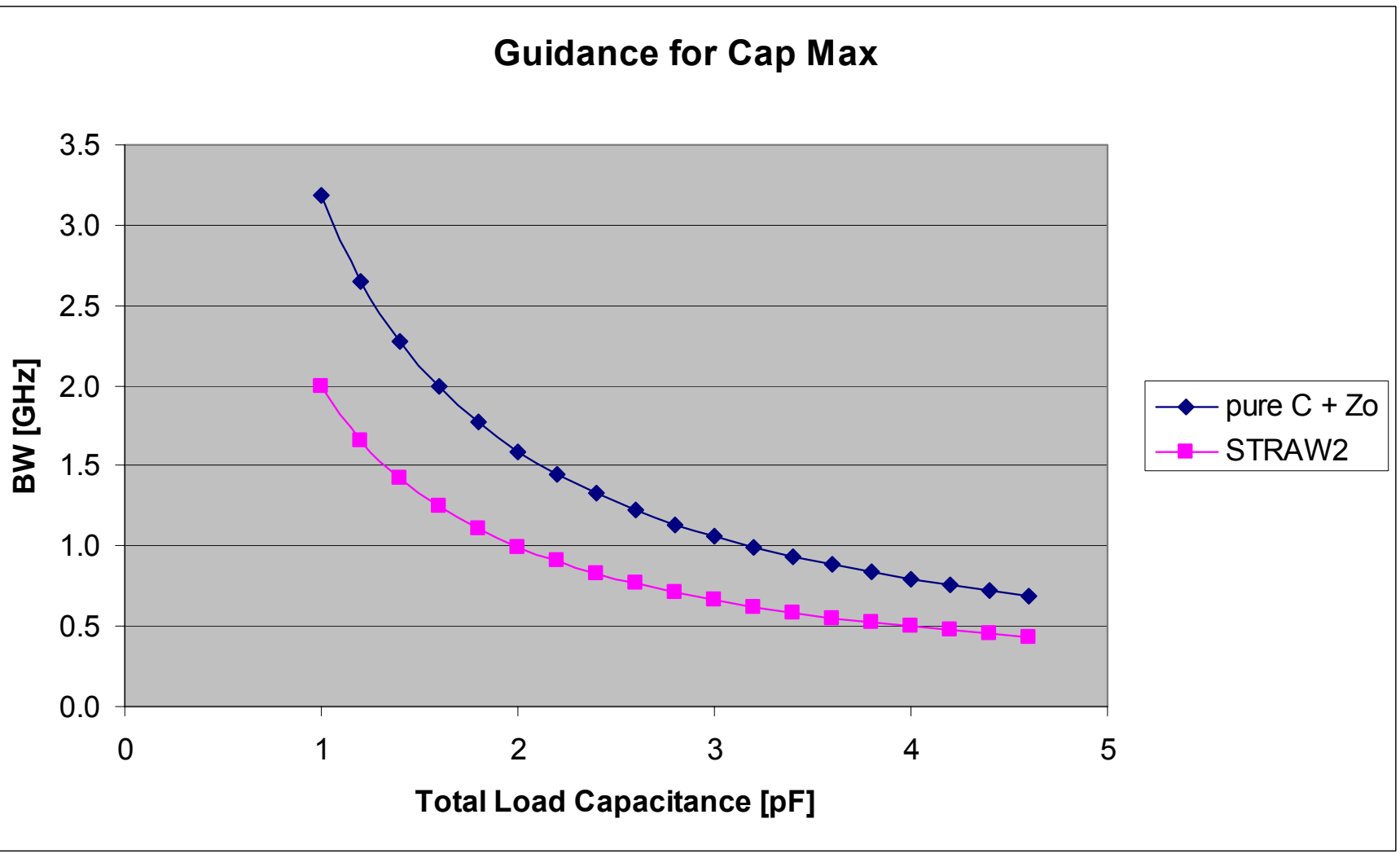
$Z=Z_0$ ~50Ω C~2.5pF

$$f_{3dB} = \frac{1}{2\pi ZC} = 1.27GHz.$$

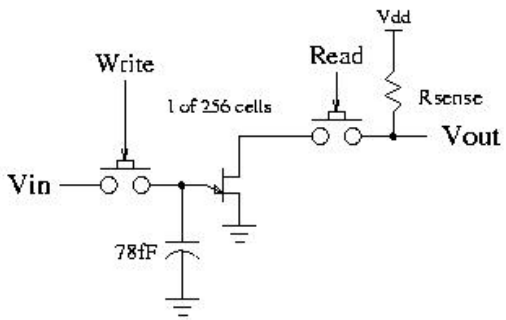
Lumped element

~80Ω C~2.5pF 800MHz C probably pessimistic, but 2nd pole?

Bounding Case



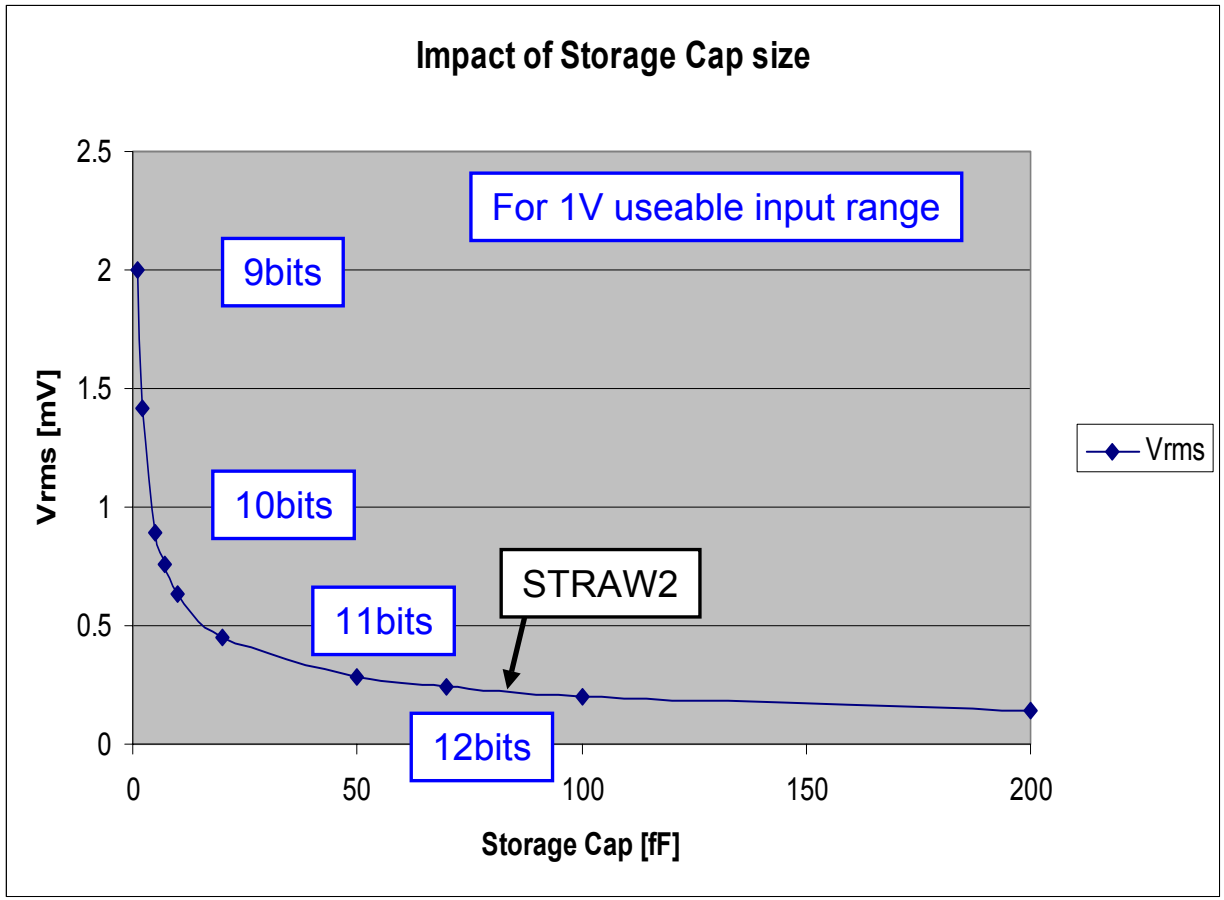
Storage Capacitor constraints



$$v_{rms} = \sqrt{\frac{kT}{C_{store}}} = 0.23mV$$

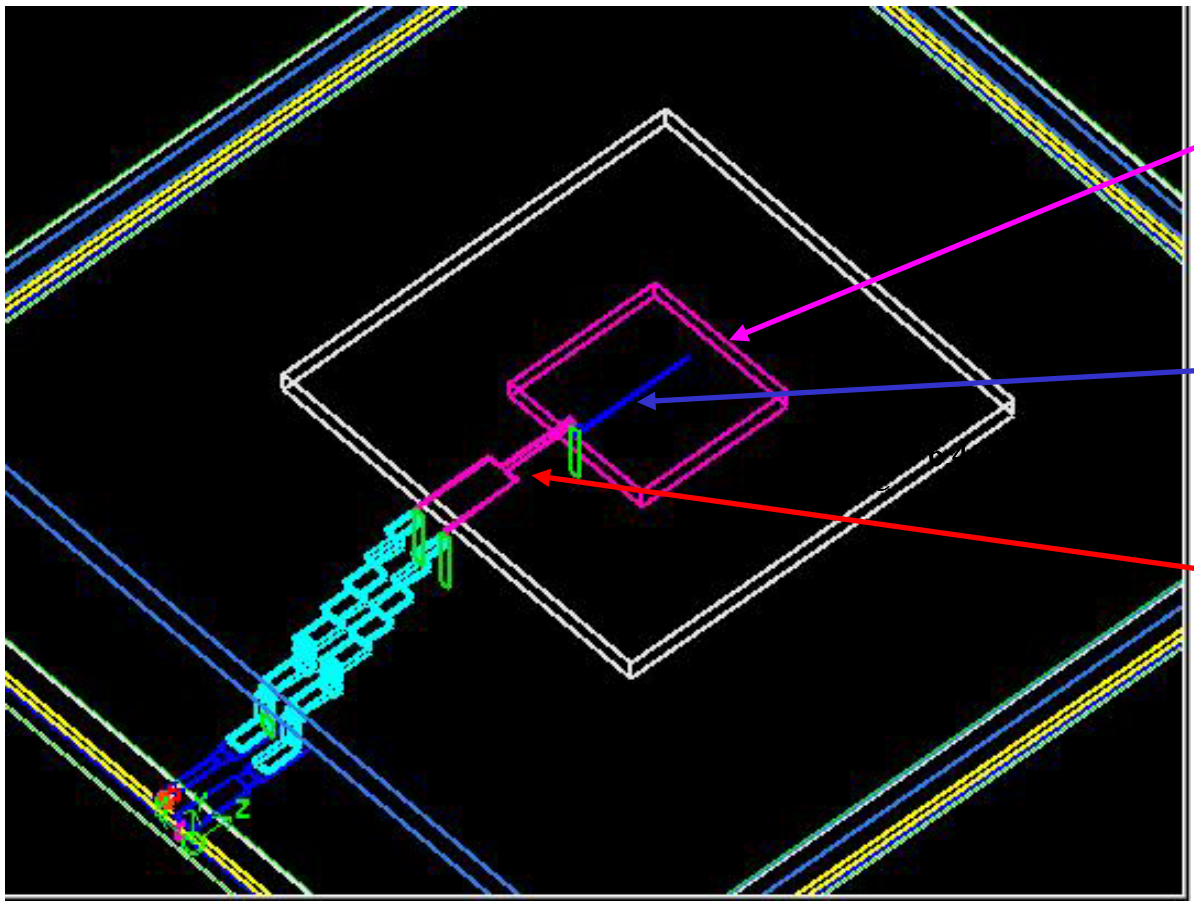
C_{store} only 78fF !!

Too big??



DC SPICE sim shows can make R_{static} ~ 920Ω, but there is a dynamic component also.

RF Coupling Simulation



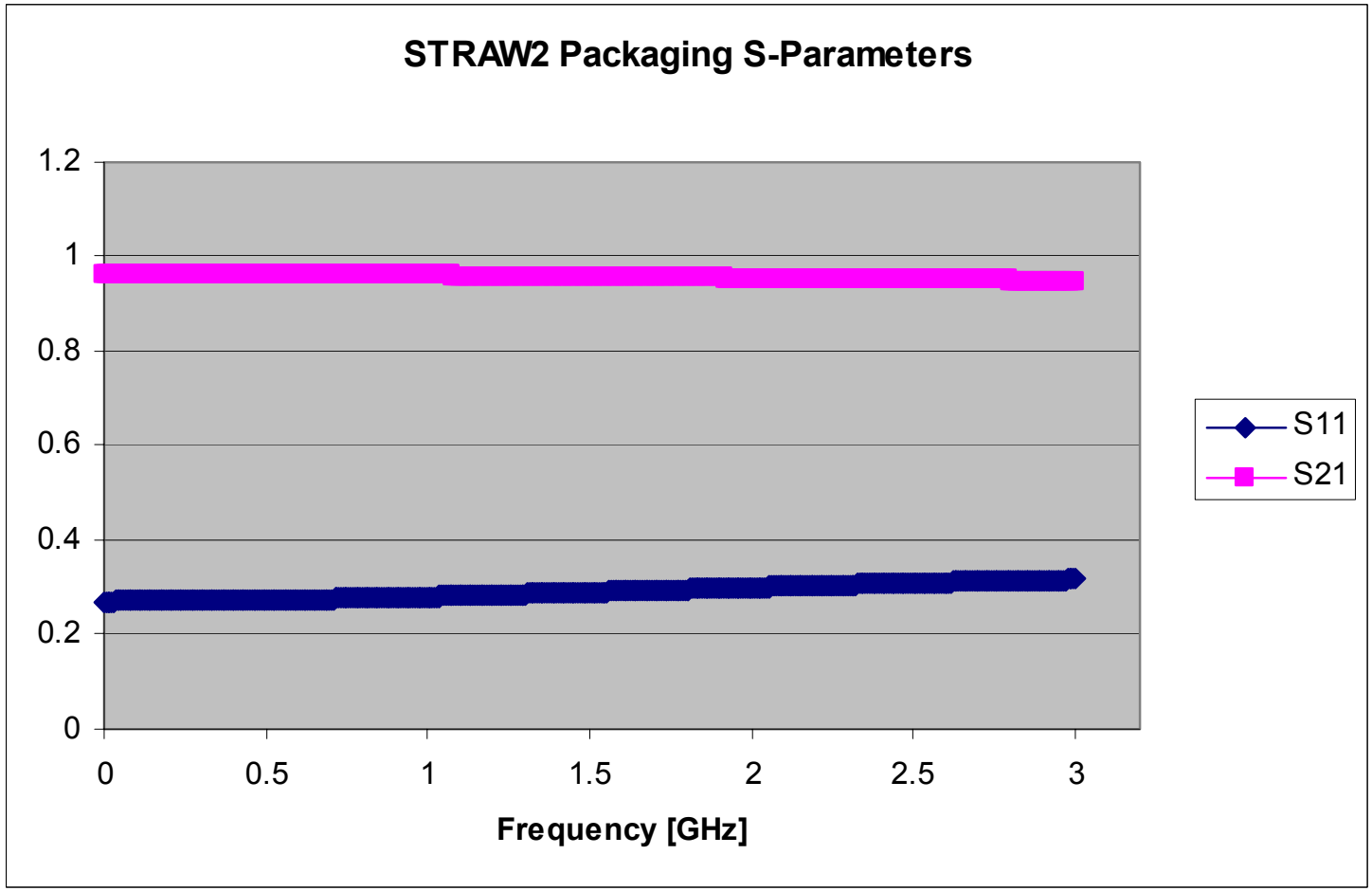
- Utilizes the LC program (FTDT algorithm)
  - Cray developed, available for free under Linux

S-Parameters

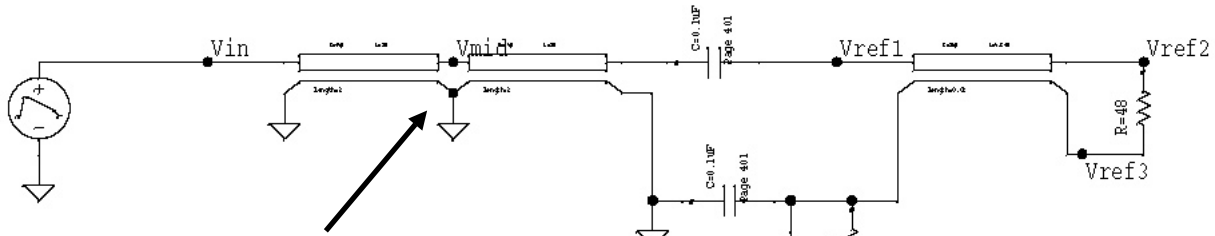
VSWR:

1.8 [1GHz]

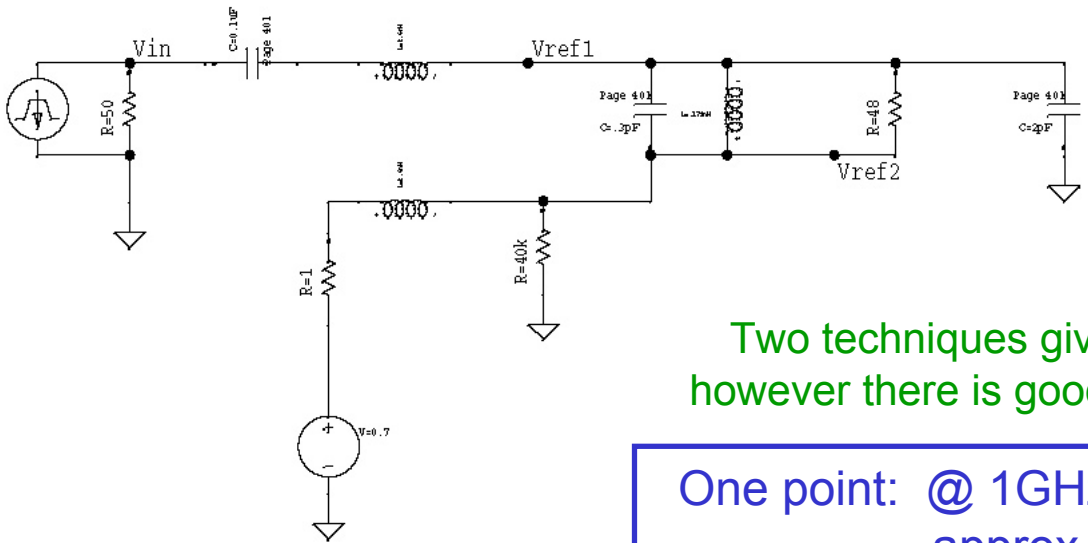
1.9 [2GHz]



SPICE stripline vs. lumped



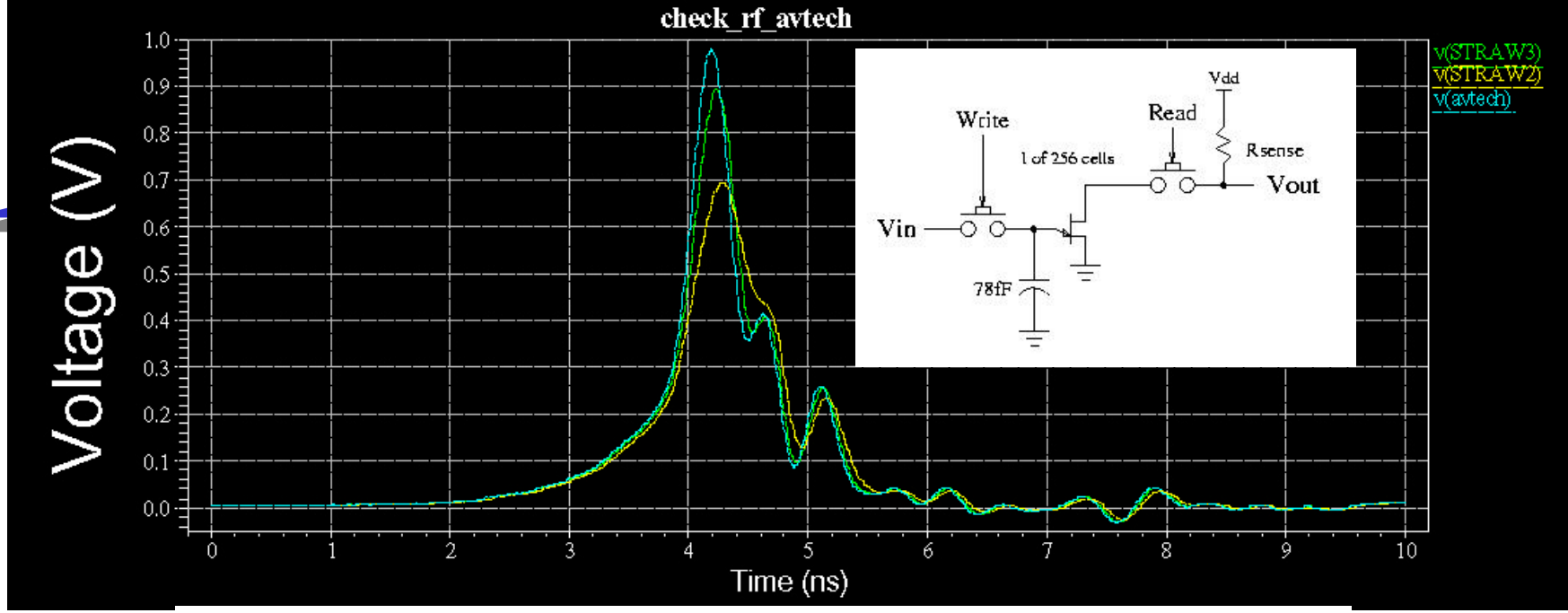
Transmission line – lossy (multiple elements)



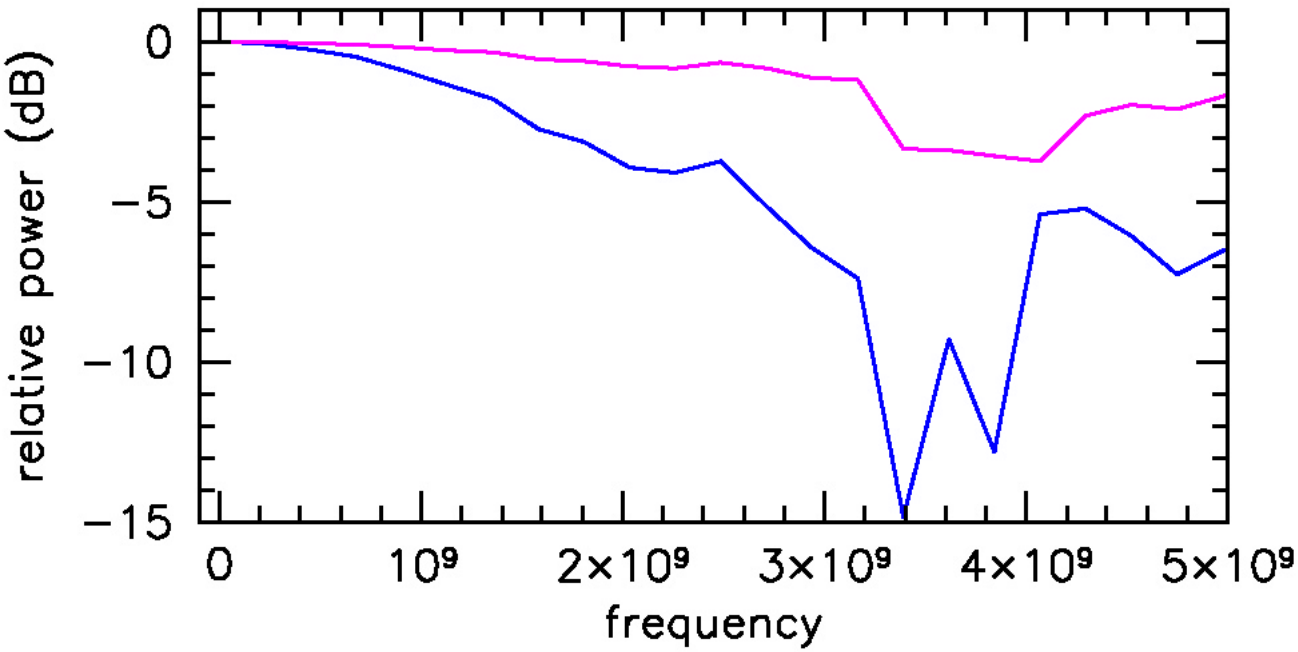
Two techniques give plausibly consistent results, however there is good reason to be skeptical (GIGO)

One point: @ 1GHz, length of on-chip stripline is approx.4-6° (STRAW2/3)

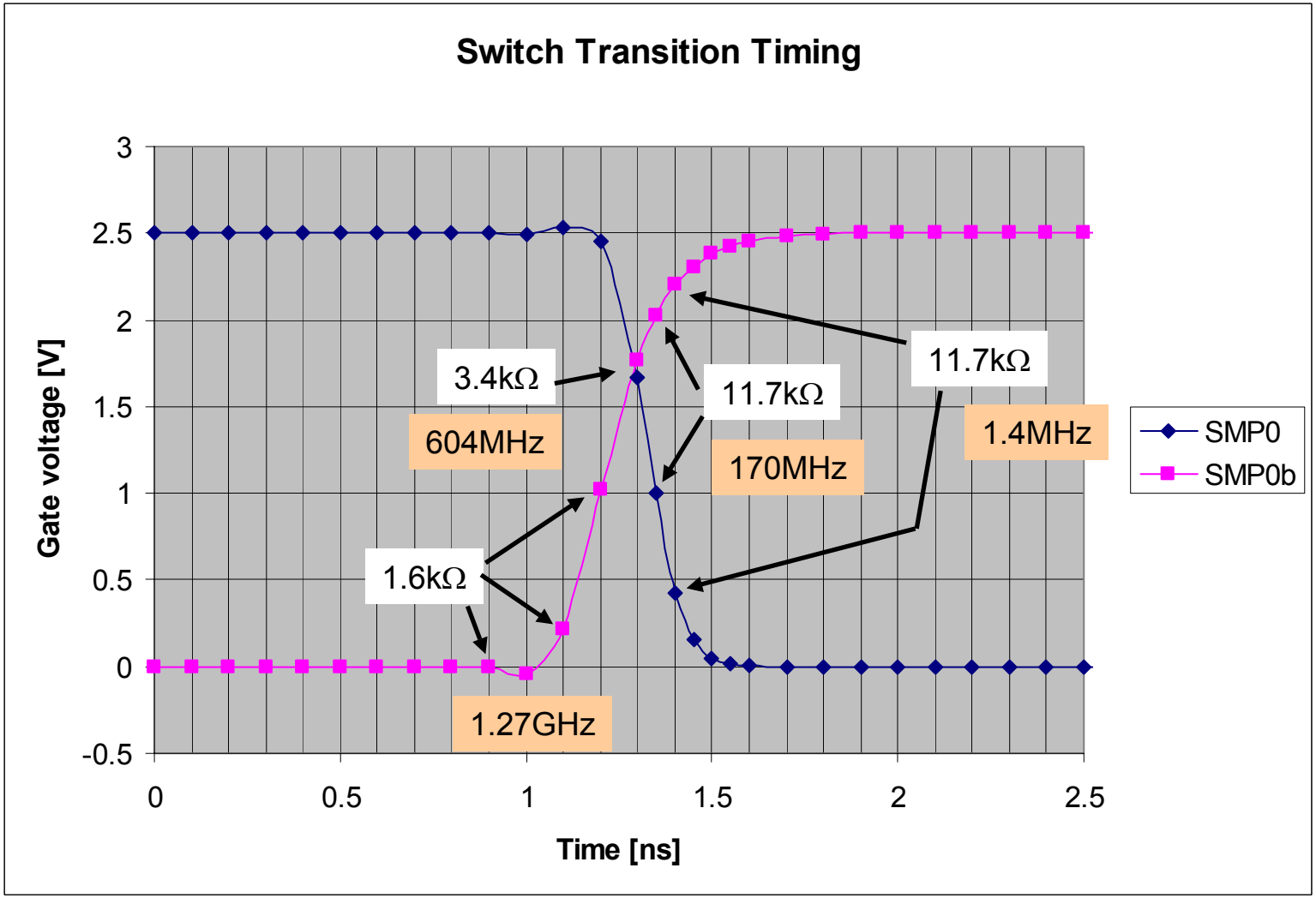
[~3° LABRADOR]



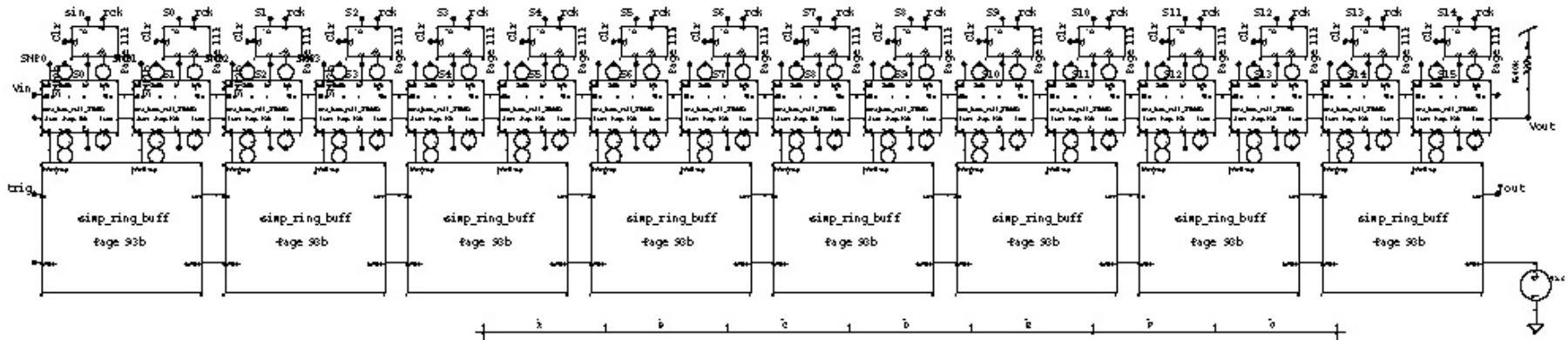
Tried after Last design Review – BW obtained Too High!!

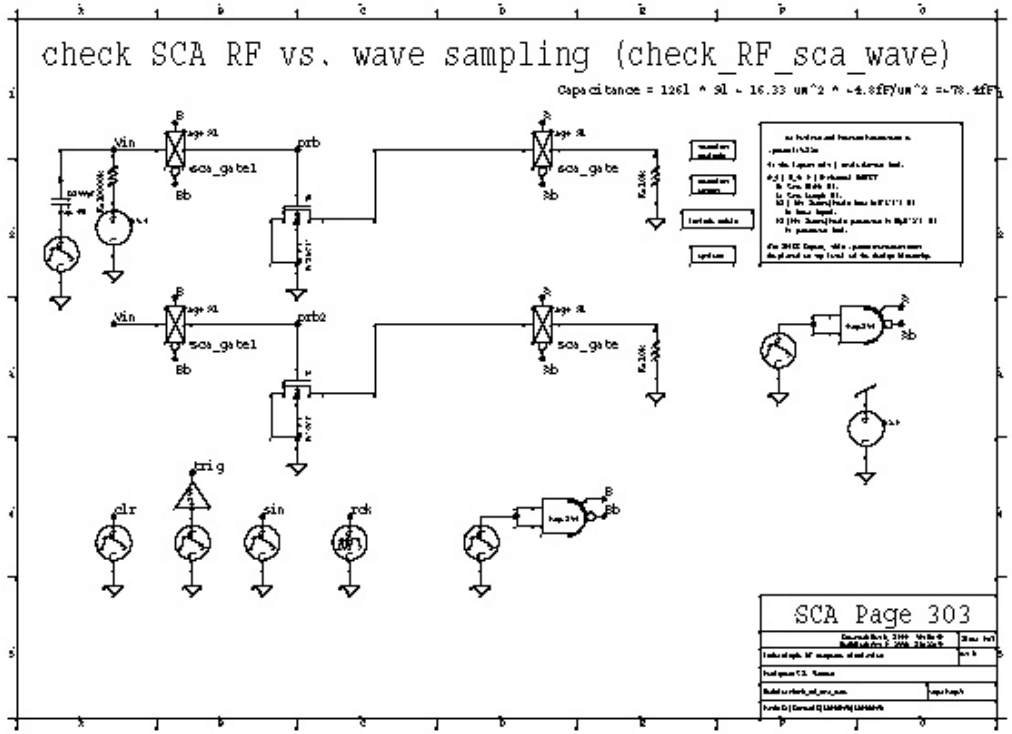


A worry...

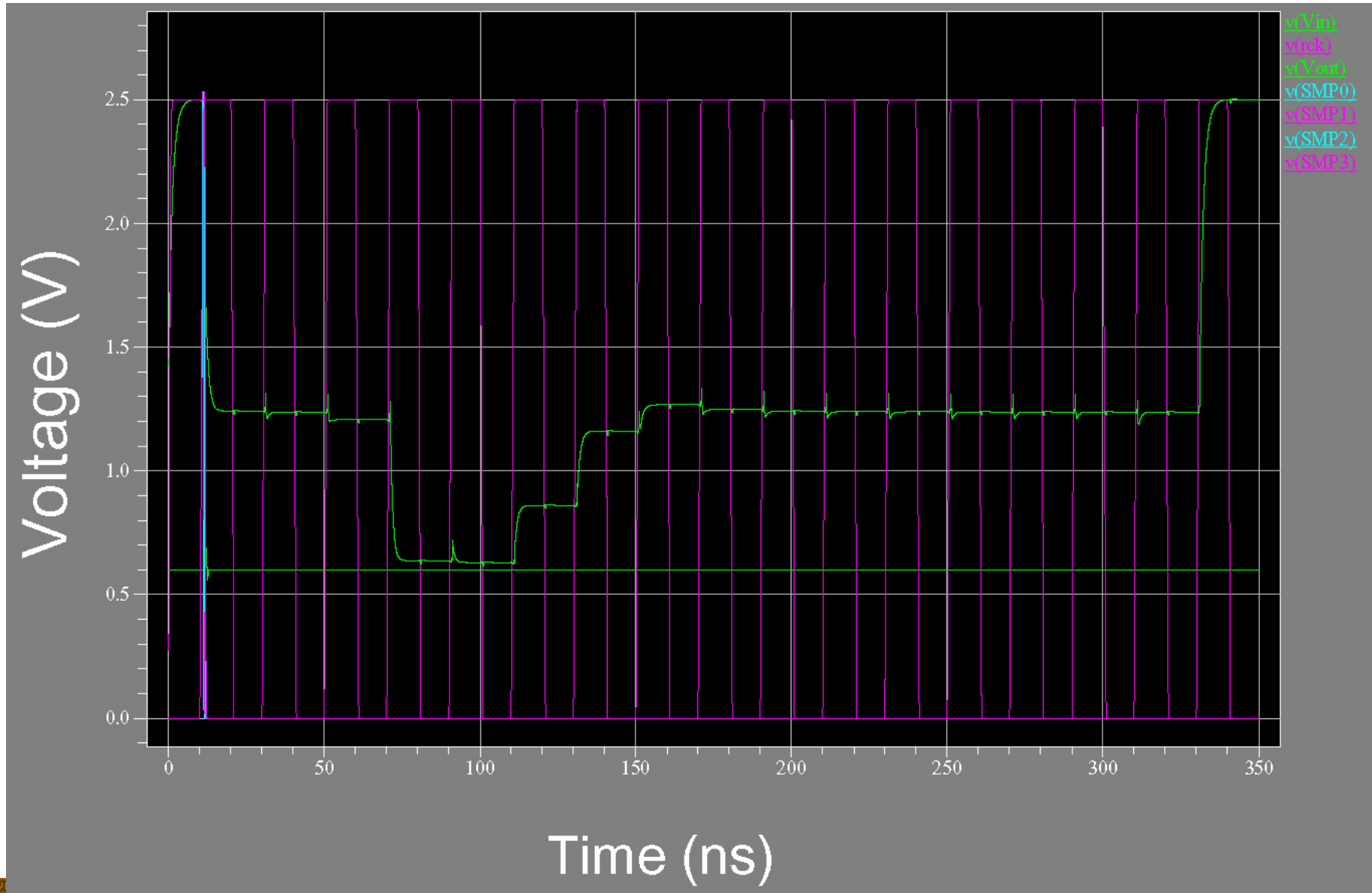

Switch Transition Timing
Gate voltage [V]
Time [ns]
3
2.5
2
1.5
1
0.5
0
-0.5
0
0.5
1
1.5
2
2.5
3.4kΩ
604MHz
11.7kΩ
170MHz
11.7kΩ
1.4MHz
1.6kΩ
1.27GHz
SMP0
SMP0b

SPICE Wave capture Sims

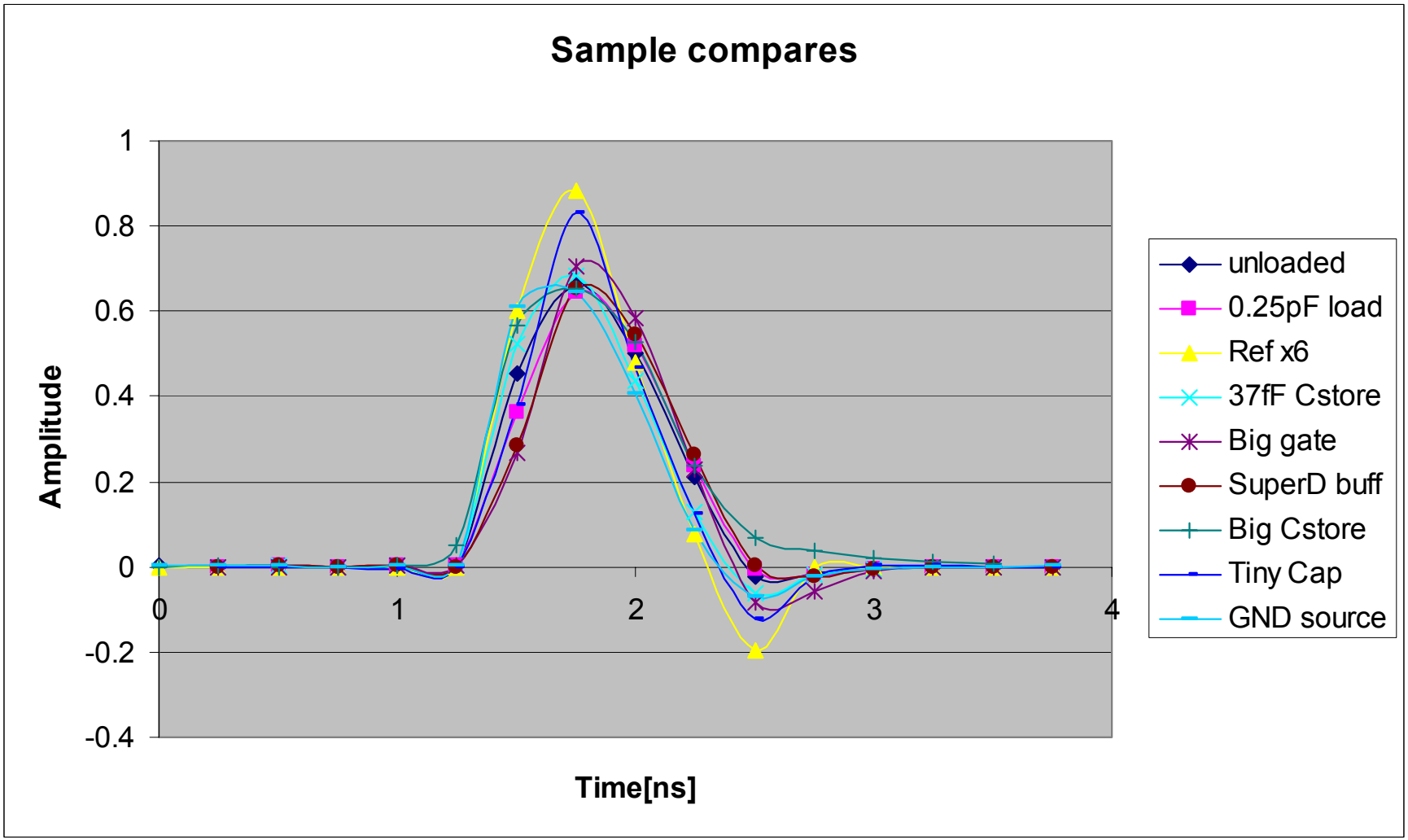


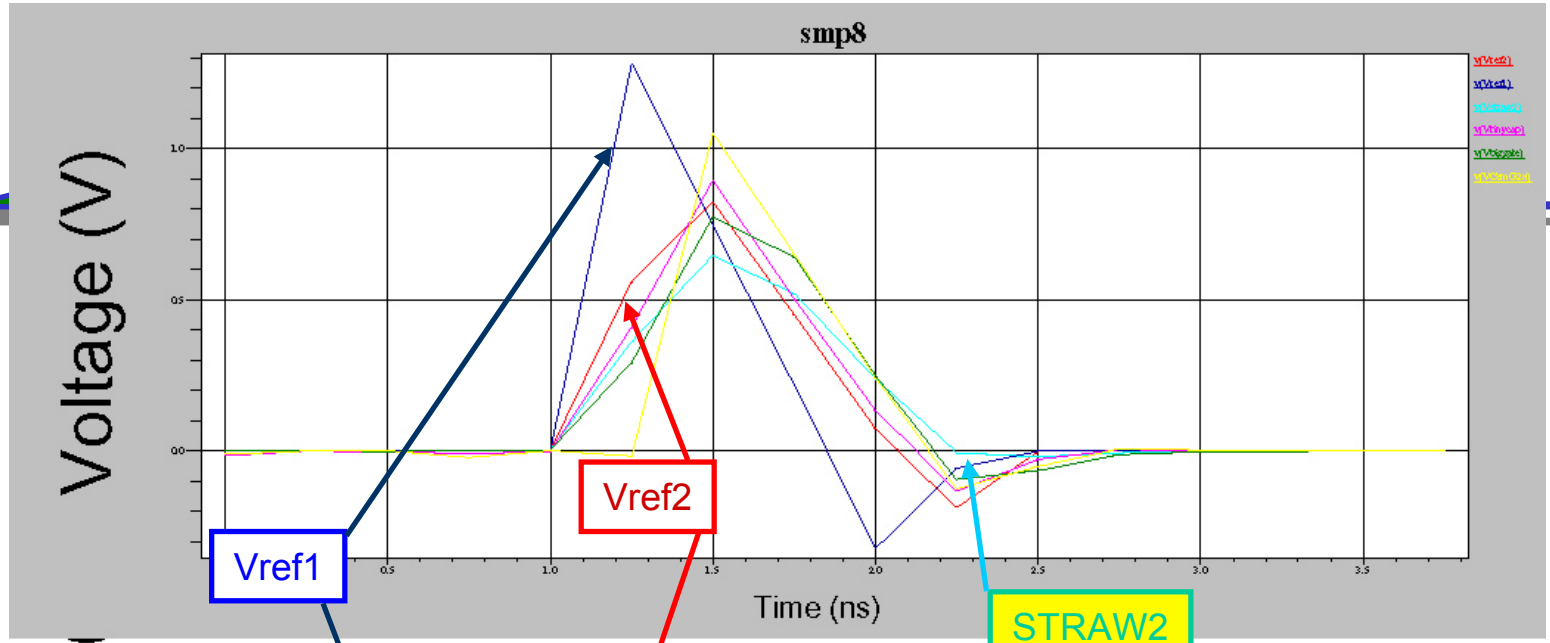


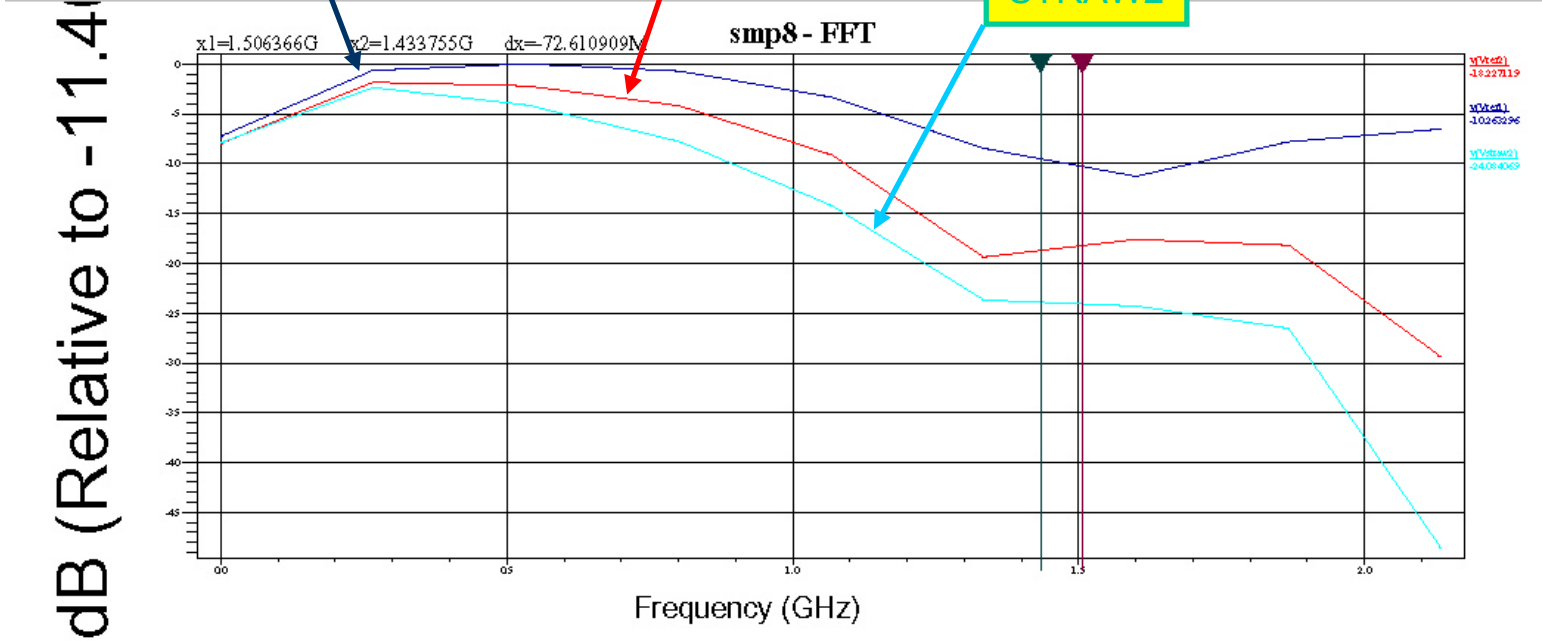
Raw Waveform



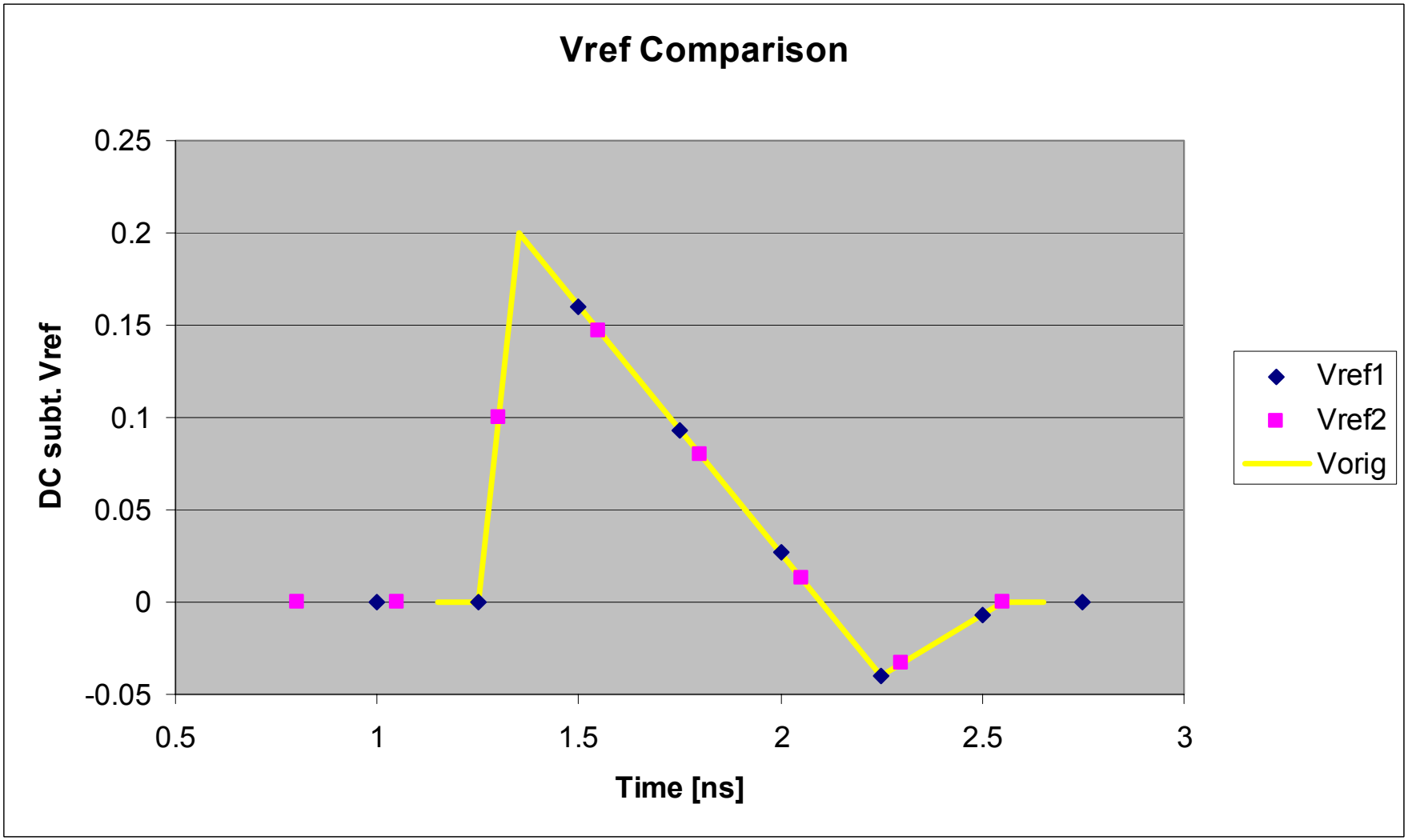
Simulation


Sample compares
Amplitude
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
0
1
2
3
4
Time[ns]
unloaded
0.25pF load
Ref x6
37fF Cstore
Big gate
SuperD buff
Big Cstore
Tiny Cap
GND source

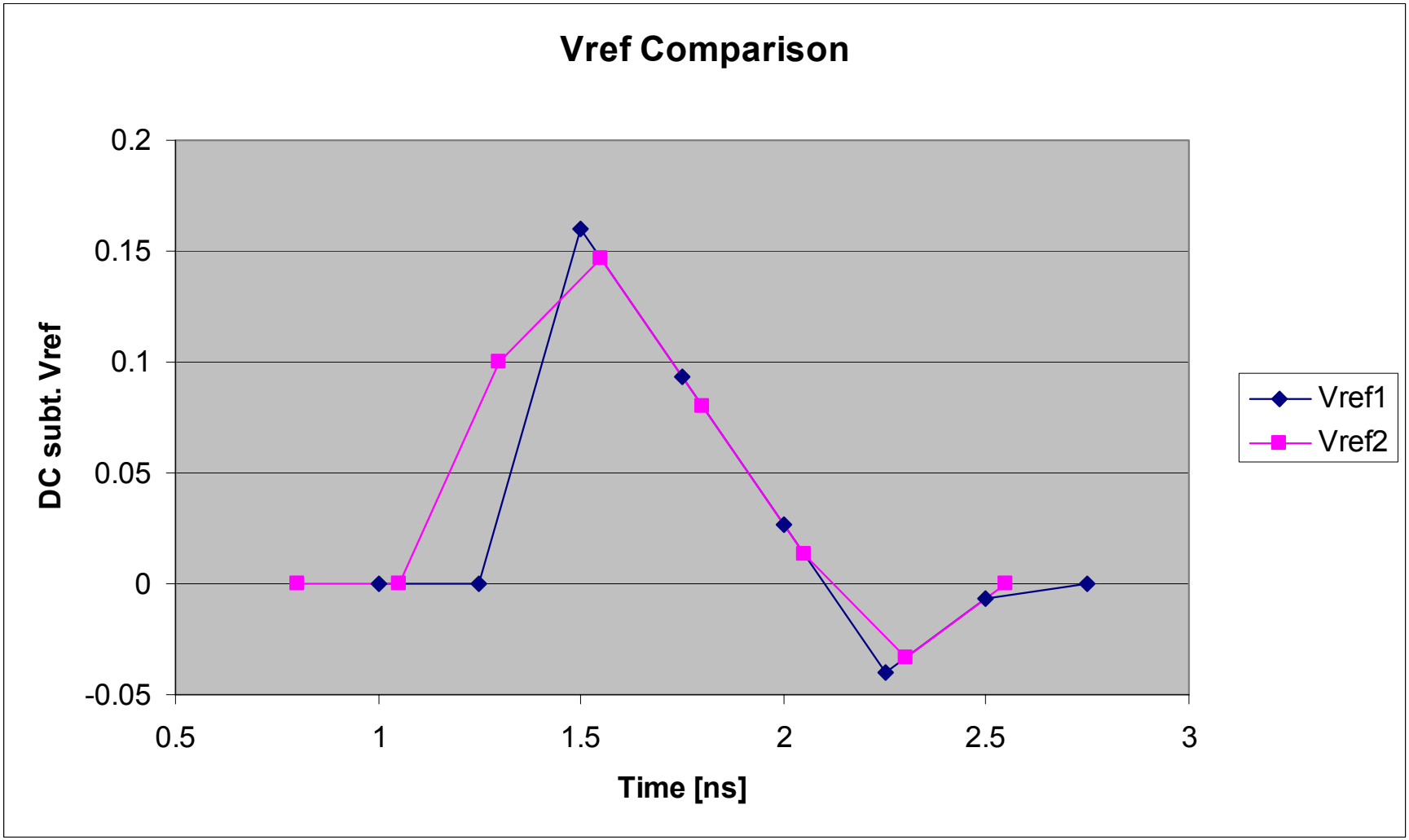

smp8
Voltage (V)
Time (ns)
Vref1
Vref2
STRAW2


smp8 - FFT
x1=1.506366G
x2=1.433755G
dx=-72.610909M
dB (Relative to -11.4
Frequency (GHz)

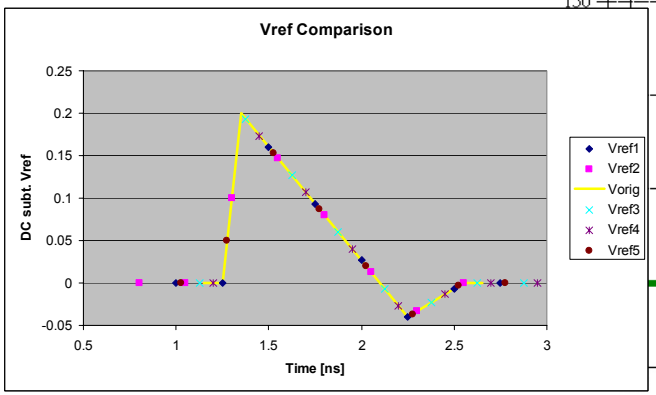
Cross-check

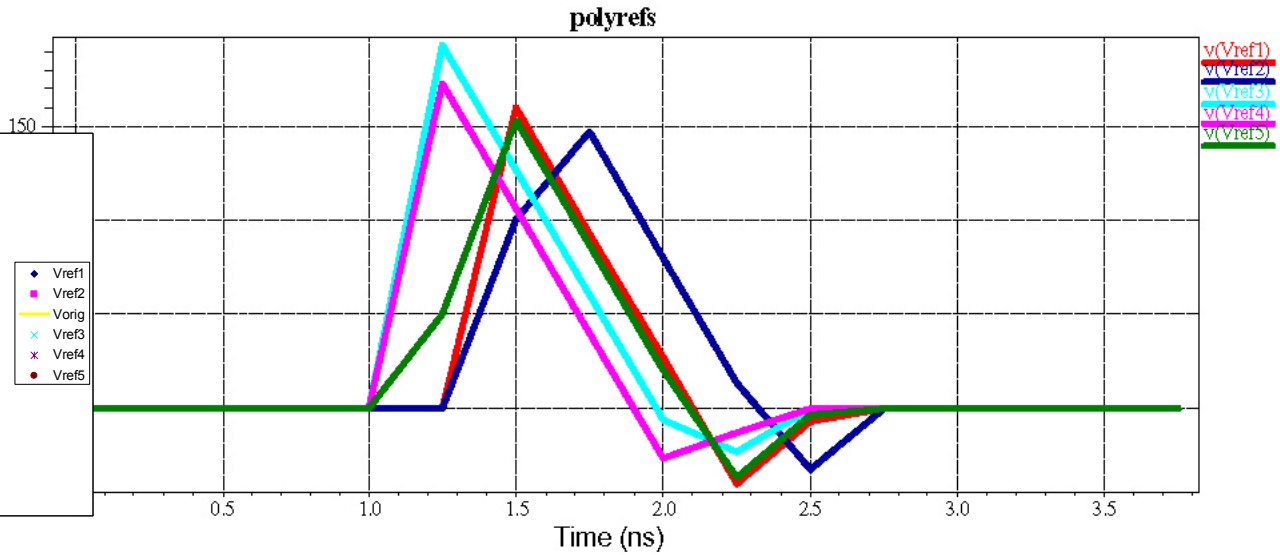

Vref Comparison
DC subt. Vref
0.25
0.2
0.15
0.1
0.05
0
-0.05
0.5
1
1.5
2
2.5
3
Time [ns]
Vref1
Vref2
Vorig

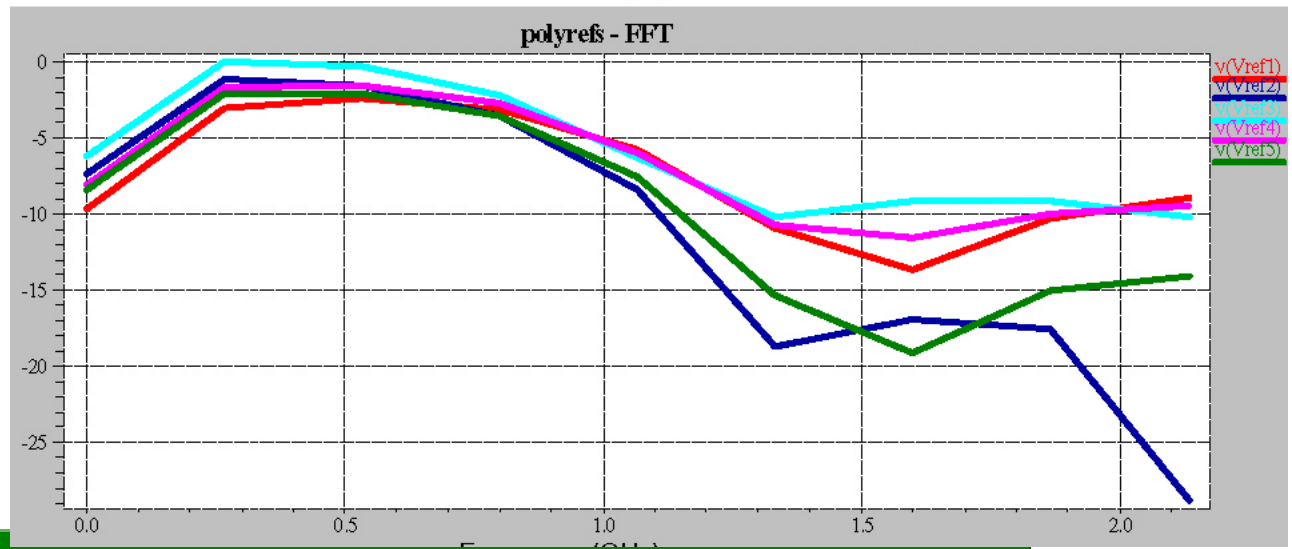
Cross-check (2)



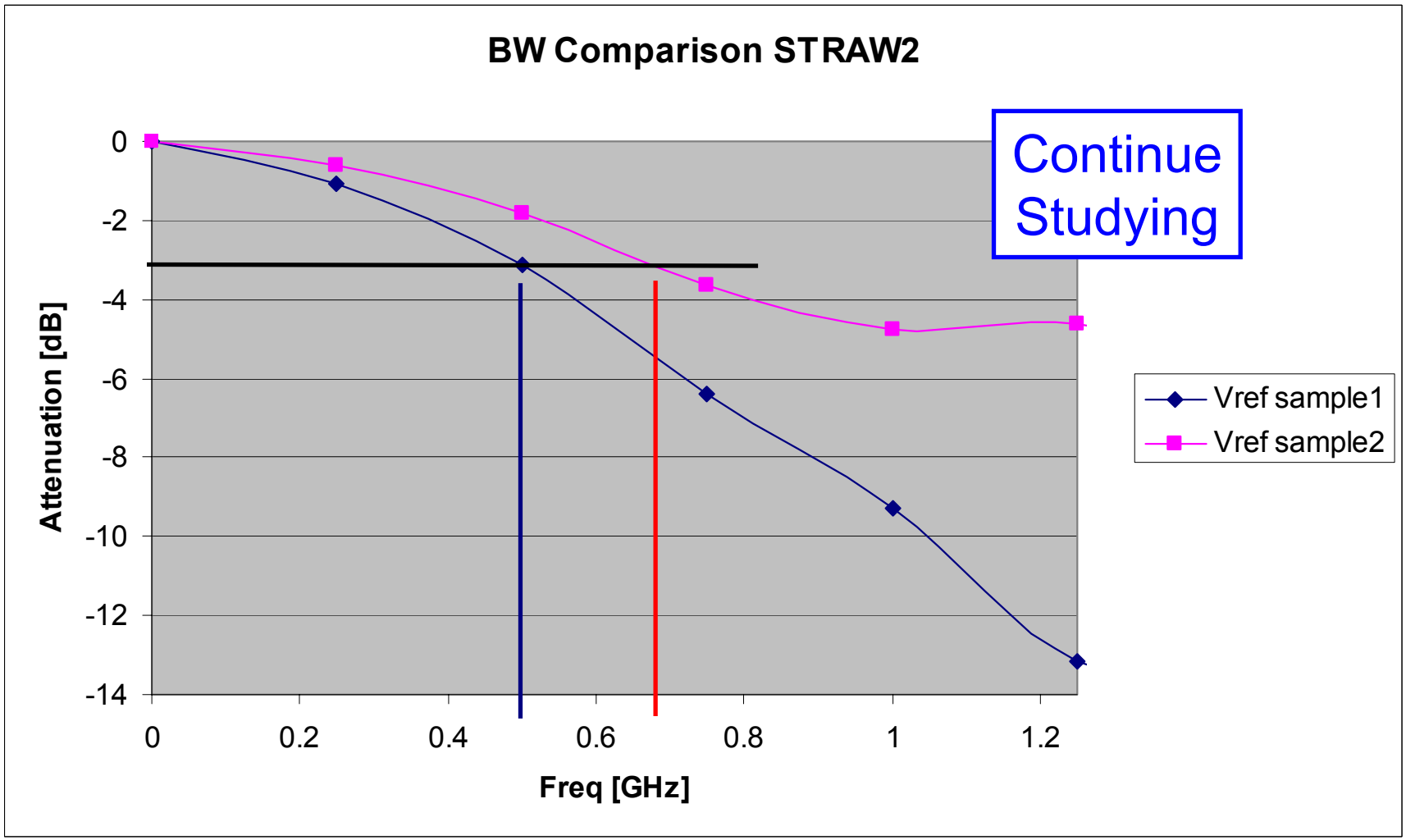
Cross-check (3)







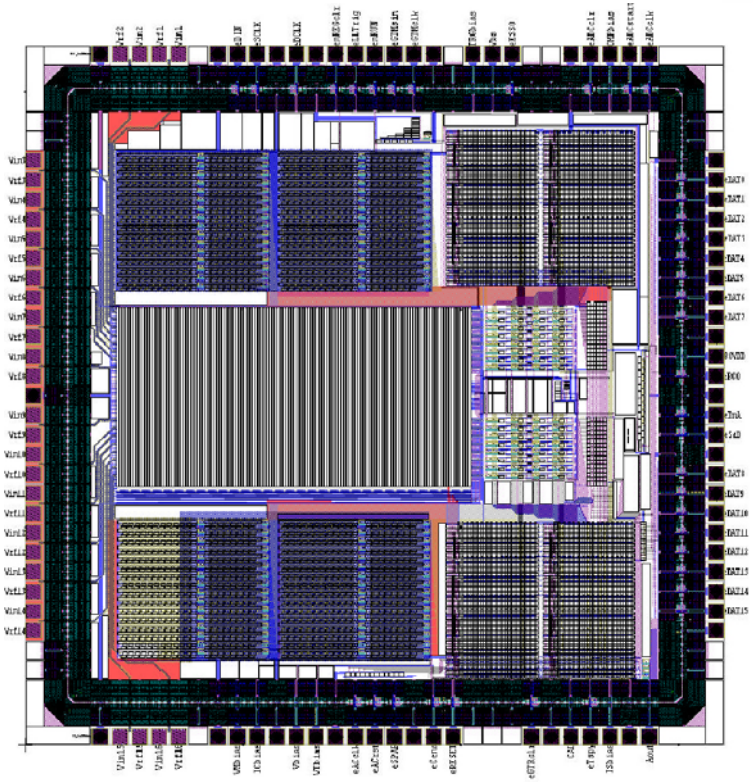
Treat as Systematic Error?



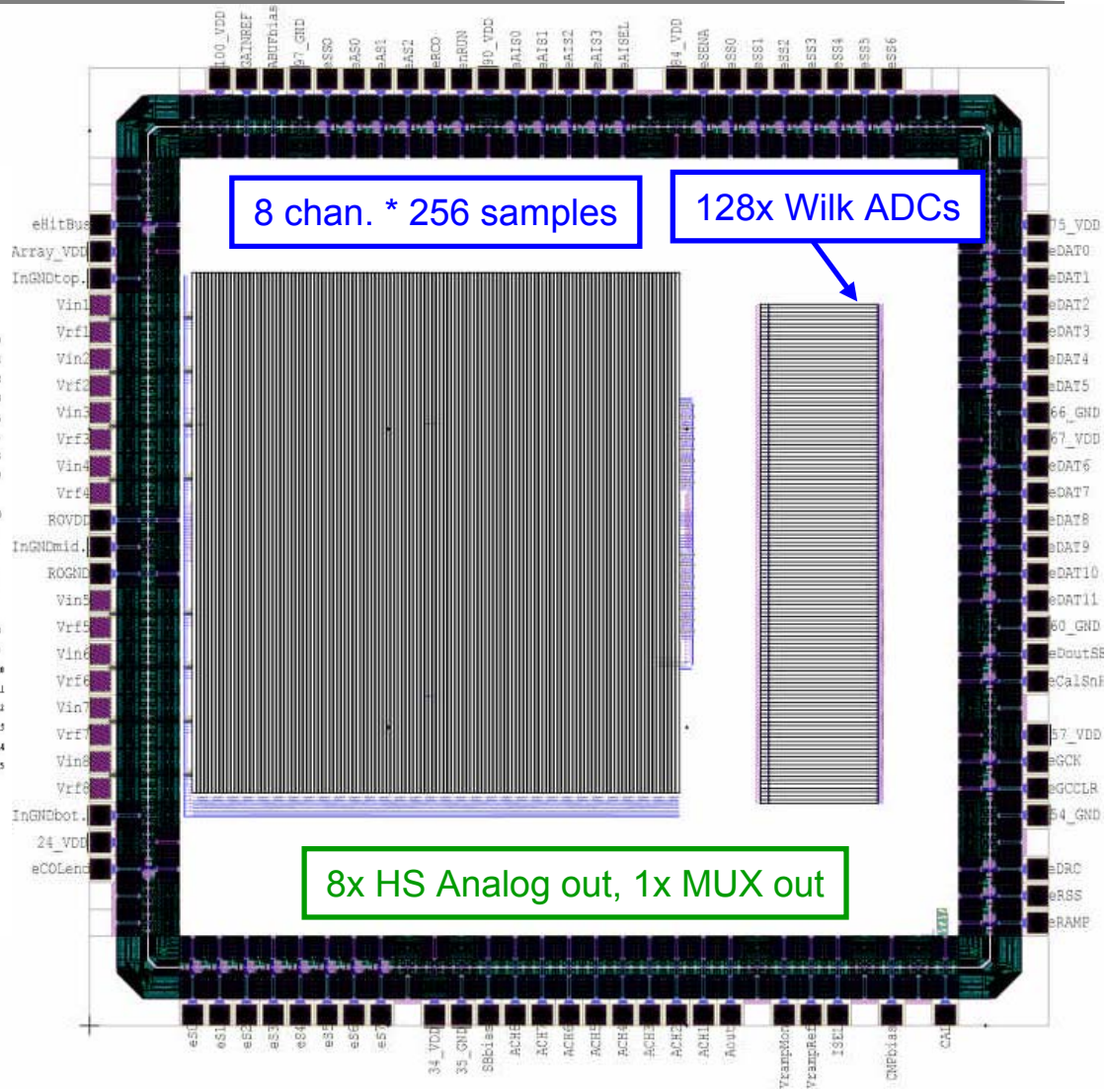
Convergence

```
*
* Accuracy and convergence options:
*      absi|abstol : 5e-010          absv|vntol : 1e-006          accurate : 0
*            cshunt : 0              dchomotopy : All             dcmethod : Standard
*            dcstep : 0        extraiter|newtol : 0                  fast : 0
*              gmin : 1e-012            gmindc : 1e-012            gramp : 6
*            gshunt : 0               kcltest : 1                kvltest : 0
*    maxdcfailures : 4              mindcratio : 0.0001        minsrcstep : 1e-008
*       numnd|itl1 : 200         numndset|dchold : 20          numns|itl6 : 50
*       numnx|itl2 : 80              numnxramp : 40              precise : 0
*      reli|reltol : 0.0005              relv : 0.0005           tolmult : 1
*
* Timestep and integration options:
*            absdv : 0.5          absq|chargetol : 1e-014            ft : 0.4
*           lvltim : 2                  maxord : 2                method : gear
*     mintimeratio : 1e-009               mu : 0.5            numnt|itl4 : 10
* numntreduce|itl3 : 3              poweruplen : 0                reldv : 0.35
*   relq|relchgtol : 0.0005             rmax : 2                  trtol : 10
*
* Model evaluation options:
*             dcap : 2                  defad : 0                 defas : 0
*             defl : 0.0001             defw : 0.0001             defnrd : 0
*           defnrs : 0                  defpd : 0                 defps : 0
*            deriv : 0      minresistance|resmin : 1e-005        modelmode : cachetable
*           moscap : 0           mosparasitics : 0                 scale : 1
*            scalm : 1                  tnom : 25                    wl : 0
*
* Linear solver options:
*     linearsolver : best              pivtol : 1e-014           zpivtol : 1e-006
*
```

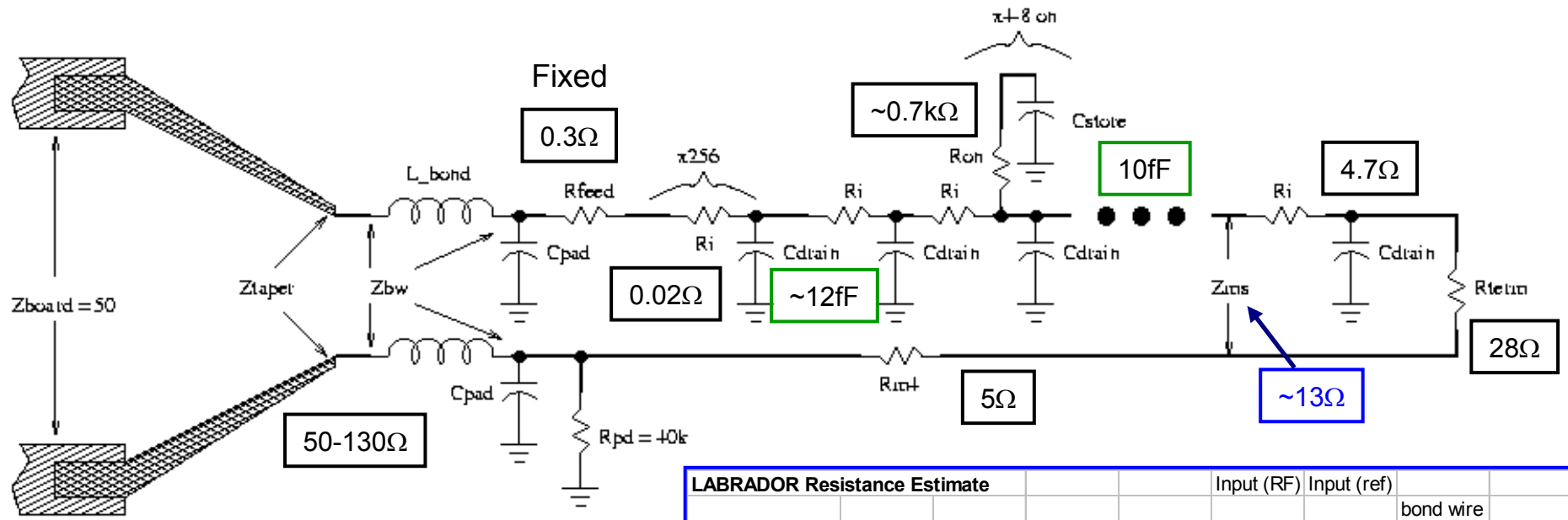
LABRADOR case

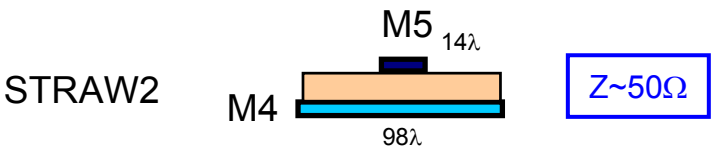


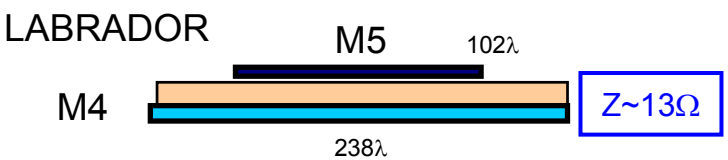
STRAW3



LABRADOR Equiv. Ckt.

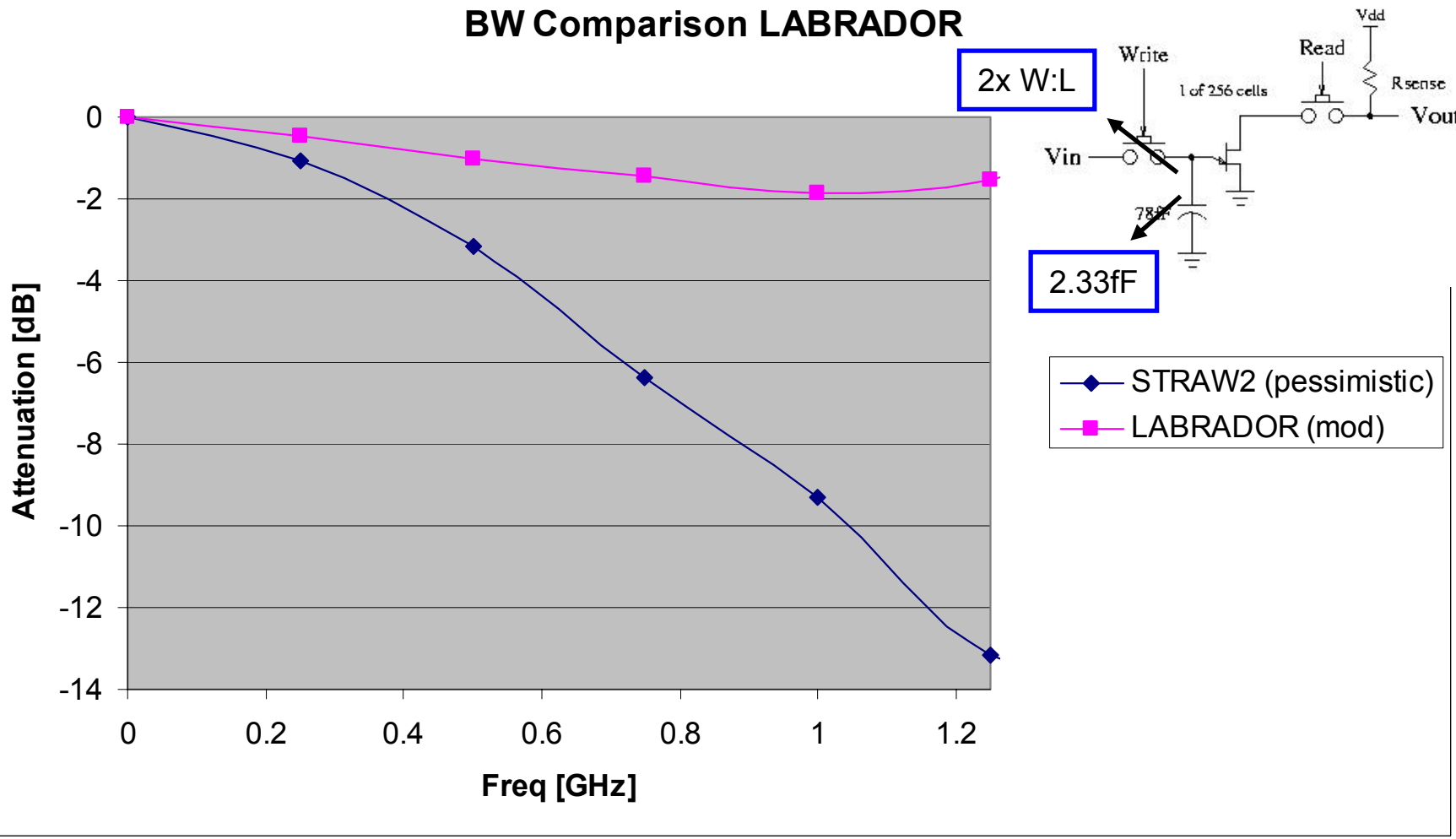






LABRADOR Resistance Estimate					Input (RF)	Input (ref)	
							bond wire
Length	17000	λ			0.0	0.1	pad
			70			0.2	M5-M4
Metal 4(sheet) =	0.07	Ohm/sq		71.42857		5.0	typ length (sq.)
Metal 5(sheet) =	0.03	Ohm/sq	166.6667		5.0		typ length (sq.)
Poly contact =	5.1	Ohm	6	6	0.9	0.9	
via 1=	2.7	Ohm	6	3	0.5	0.9	
via 2=	5.35	Ohm	6	3	0.9	1.8	
via 3=	8.26	Ohm	6	3	1.4	2.8	
via 4=	11.34	Ohm	6		1.9		
					10.5	11.5	Total per feed
						28	Rterminator
		Measured:		Ohm		**50.0**	Grand Total

Comparison


BW Comparison LABRADOR
Attenuation [dB]
0
-2
-4
-6
-8
-10
-12
-14
0
0.2
0.4
0.6
0.8
1
1.2
Freq [GHz]
2x W:L
2.33fF
Write
Read
Vdd
Rsense
Vout
Vin
1 of 256 cells
STRAW2 (pessimistic)
LABRADOR (mod)

LABRADOR – Best Guess onto chip

Component	Length/area	Unit	Factor	Funit	Total [fF]	
Input traces	5	cm	0.2	pF/cm	1000	w.a.g.
bonding wire	150	mil	0.3	pF/wire	300	w.a.g.
input pad	60	um^2	187	fF/pad	187	Tanner
input protection	594	λ	1.1	pF/ckt	1100	SPICE
stripline area	2500	um^2	43	aF/um^2	107.5	MOSIS
stripline fringe	5	mm	60	aF/um	300	MOSIS
Switch Drains	256	switches	~~5.6~~ 8fF	fF/drain	~~1433.6~~	~~SPICE~~
Open Switches	6	open	~~87~~	fF/gate	~~522~~	SPICE
TOTAL			2.3fF		**4.9501**	**pF**

0.3pF?

2.05pF

$Z=Z_0$ ~50Ω

C~2.35pF

$$f_{3dB} = \frac{1}{2\pi ZC} = 1.35GHz.$$

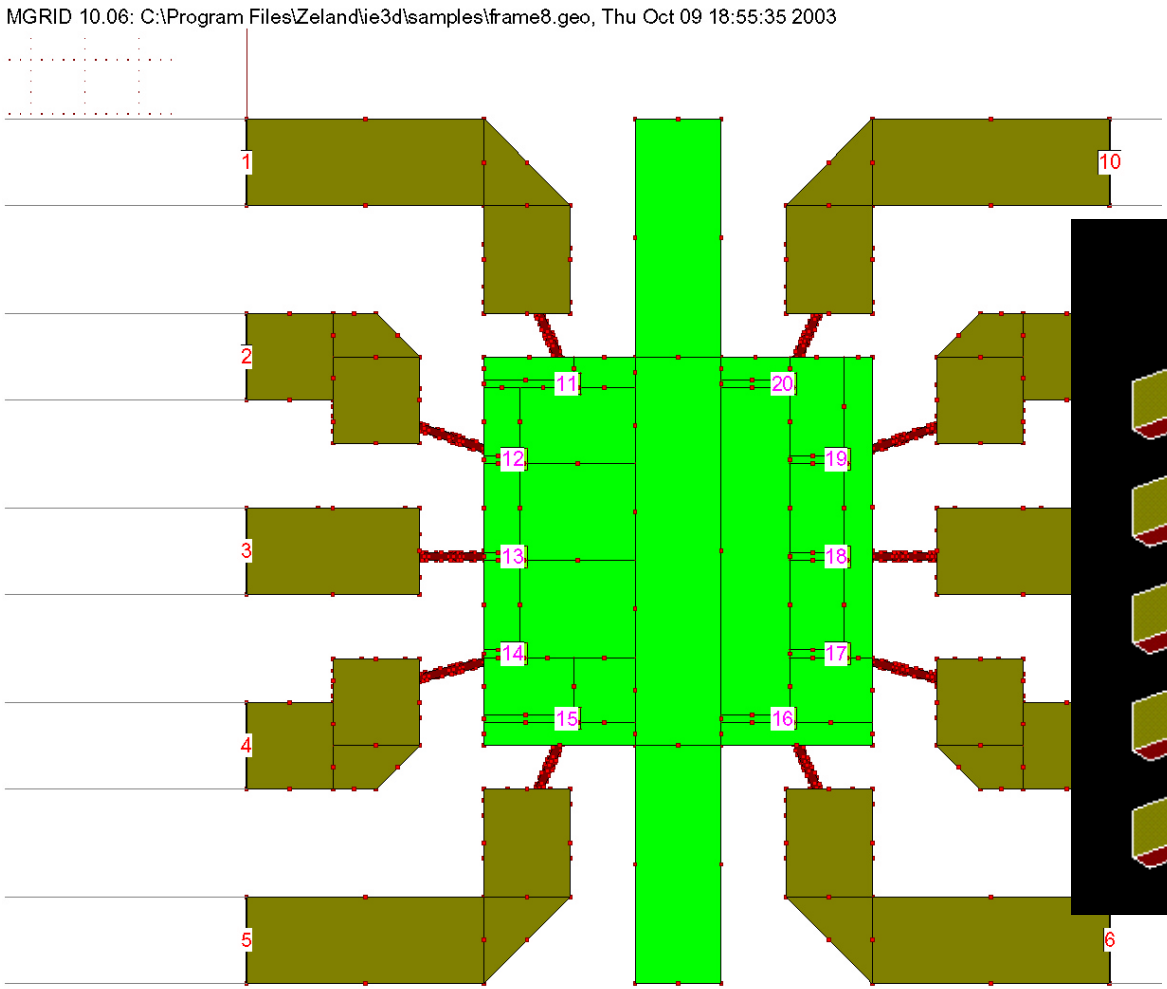
Hard to get much higher

Pessimistic case: full stripline Cap = .74pF
If use bigger transistors, Ctotal ~ 2.8pF

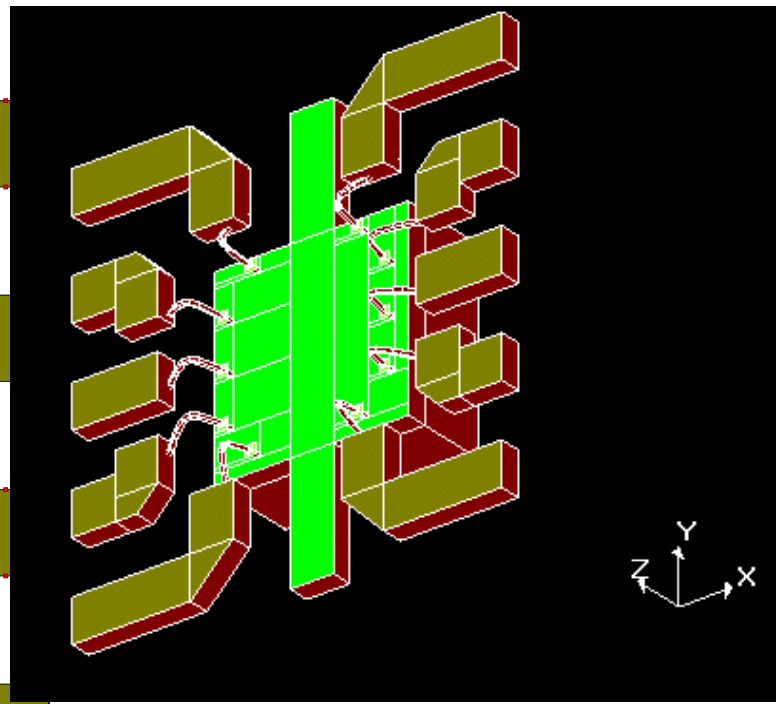
$$f_{3dB} = \frac{1}{2\pi ZC} = 0.876GHz.$$

[Min tran & full Cap = 1.46GHz]

Zeland Software



Serious Learning Curve
Basically as complex as AutoCAD

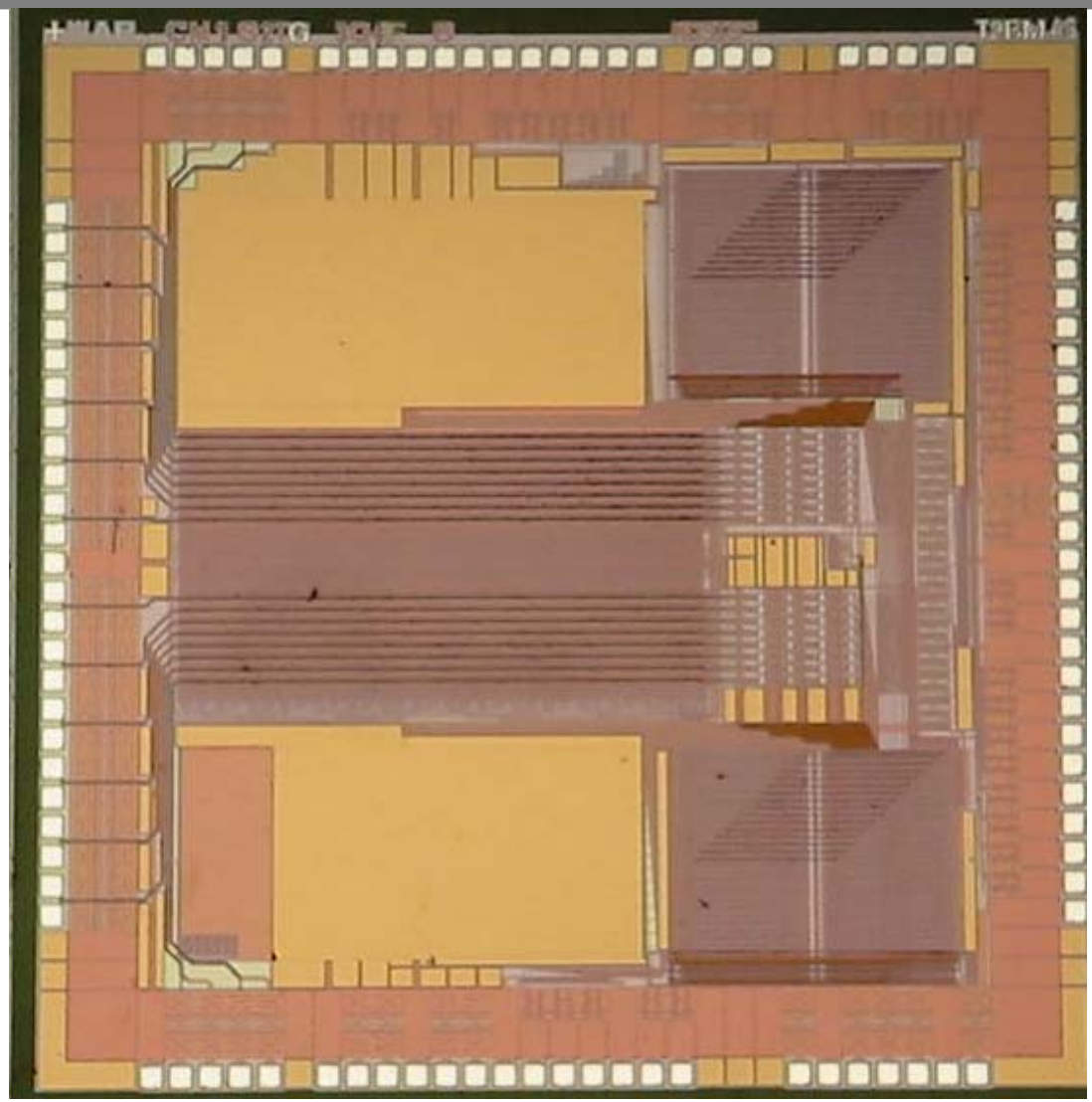


Best use of time?

Summary/Homework

- Package simulation
  - Geometry Input to Zeland quite elaborate
  - Will take some time
  - Not much can do about (BGA not really an option)
- Plans:
  - LABRADOR submission deadline (11/17)
    - Only mopping up after everyone disappears for Antarctica
  - Bite bullet and increase SPICE sim window enough to do AVTECH pulse simulation
  - Optimization: specific tuning:
    - Storage cap size
    - Storage gate size
  - Multi-dim optimization? (using 4x software tools…)
- Action Items from this meeting (another mtg?)
- Hope at least can sign-off on general issues

Back-up slides



Summary:Design Issues for ANITA

- RF amps/filter mounting
  - Directly onto back of antennas? (modular)
    - Better performance, but power, cooling, cabling issues
  - Miteq LNAs adequate?
  - Sufficient sensitivity (w/ power limit, multi-notch filters) ??
- Trigger architecture:
  - Global, local, cluster (half-array) ??
  - Logic on ARF boards ??
  - Multi-leveled ?? Multi-band ??
  - VETO ?? RCP & LCP generation ??
- Signal digitizing:
  - Random interleaving (longer record length) ??
  - Alternatives to current plan ??
  - Multi-buffering (ping-pong) depth ??

High-speed Digitizers

- Kleinfelder speed but not high analog BW
- Analog BW tough
- Comm. ADC very high P