DUMAND SC Digitizer ASIC Specification

E. Hazen, E. Gergin, A. Mavretic
T. Lozic, M. Jenko, D. Orlov *Boston University*

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1 General Description

This note describes the Digitizer ASIC for the DUMAND (Deep Underwater Muon and Neutrino Detector) SC (String Controller). ***This specification is preliminary, and is subject to revision as the logic design proceeds.***

The digitizer system comprises a single large ASIC (application-specifc integrated circuit), described here, and various supporting circuitry. We plan to fabricate the ASIC using Vitesse Semiconductor's VGFX100 GaAs gate-array technology. The logic design is being done at Boston University on our Mentor Graphics CAE system.

This digitizer measures arrival time of both leading and trailing edges of 27 ECL inputs (24 Optical Modules and 3 Calibration Modules). When any input changes state, the time is recorded to 1nS. The time, along with a binary channel (input) number is output as a parallel word. Internal buffering is provided for at least 100 events to accomodate fluctuations in input rate. The output of the digitizer is a 40-bit TTL double word, designed to be compatible with the Gazelle "Hot-Rod" high-speed serial communications chipset, but can be interfaced to other devices.

2 ASIC Specifications

2.1 Clock

The ASIC operates at 500MHz, using an external two-phase clock. This clock will be provided using a crystal-controlled oscillator, which will be located adjacent to the ASIC on the same PCB. If it is necessary, the time relationship of the two clock phases will be trimmed with an external circuit.

2.2 I/O pins

Following is a list of the I/O pins. Test pins are not included.

number	Name	I/O	*type*	*description*
2	CLK1	I	ECL Diff	500 Mhz clock ϕ 1
2	CLK2	I	ECL Diff	500 Mhz clock ϕ 2
27	ID0..ID26	I	ECL	fast data inputs
9	AUX0..AUX8	I	TTL	aux data inputs
1	AUXCK	O	TTL	aux data clock
40	D0..D39	O	TTL	parallel data out
1	DVAL	O	TTL	data valid flag
1	DSTB	I	TTL	data read strobe
1	DCLK	O	TTL	data clock
2	SCW0,SCW1	I	TTL	control/config data from SC computer
2	SCR0,SCR1	O	TTL	control/config data to SC computer
1	ENRO	I	TTL	enable roll-over words
1	ENNL	I	TTL	enable null words
1	HSMOD	I	TTL	handshake mode select
2 ?	NLRT	I	TTL	set null word rate
?	TEST?	I	?	Test inputs
?	TEST?	O	?	Test outputs

3 Design Details

3.1 Operation

For each input transition, a 10-bit *time field*, 5-bit *channel number*, and 1 bit *up/down flag* are transmitted. Every 1μS (when a carry occurs from the 10th time bit), a roll-over word with *channel number* = 0 is transmitted. The *time field* of roll-over words is by definition zero, so the 10 time bits and *up/down flag* are available for auxiliary data. An overflow bit is set to indicate lost data if any of the FIFO buffers overflows.

3.2 Block-by-Block Description

Refer to the attached block diagram, and data format table.

3.2.1 Input - Edge Detector

Each of the 27 inputs is sampled by two edge-triggered flip-flops, one driven by each clock phase. The resulting signals (F1 and F2) are XORed, producing a signal Z which identifies when a change of state takes place. The Z's are logically ORed to produce a TRIGGER signal, which indicates that data should be recorded. The output of this block is two sets of 27 sampled data bits (F1 and F2), and a TRIGGER signal.

3.2.2 Clock

The clock is a 9 bit synchronous counter, clocked at 500MHz. Its outputs are latched by the TRIGGER signal from the input block. The carry output of the counter itself generates a TRIGGER, resulting in an extra ("roll-over") word being inserted in the data stream every 1uS.

3.2.3 Clock Roll-Over and Aux Data

When a 1uS roll-over occurs, the 9 bits of clock data in the phase 0 data are replaced by 9 bits of external "slow" data (from hydrophones in DUMAND). An extra bit (RO) is added to flag roll-over words. Note that roll-over words may contain valid data also.

3.2.4 Primary FIFO Buffers

The data is then written to two FIFO buffers, one driven by each clock phase. Data is only written when a TRIGGER is recieved from the front-end. A new word may be written to each FIFO every 2nS.

If a FIFO is full when a write is attempted, a reserved bit (OF) is set in the top word to indicate an overflow condition, and the data is not written. However, a "roll-over" word is a special case–it is always written, possibly over-writing the top word in the FIFO. In this case the OF bit is set as well.

These FIFOs are designed to have zero latency; that is data written in on one clock cycle is available at the output immediately without any time required for "fall-through".

3.2.5 "Tag" FIFO and Data Selector

The "Tag" FIFO contains three extra bits, which keep track of the order in which words were written into the two primary FIFOs. Based on the

contents of the Tag FIFO, the read logic selects words out of the two primary FIFO buffers in time order.

3.2.6 Encoder

The encoder scans the FIFO outputs, and looks for state changes. Each state change produces an output word with time and channel number.

The data bits (F1 and F2) of the FIFO output words are XORed, producing 27 signals (Z), which are latched. A Z=1 represents an input which has changed state. The Z's are stored in 27 flip-flops, each with it's own reset input.

The Z's feed a 27-input priority encoder. Each clock cycle (every 2 nS) it produces as output a 5-bit binary number for the lowest-numbered active input. This becomes the channel number in the output data stream. The priority encoder also resets the corresponding latch.

Roll-over words require special treatment by the encoder. A roll-over word may contain valid data, as well as the auxiliary data which is encoded in the time bits. A roll-over word (with *channel number* = 31) is output first, followed by normal data words for any valid data in the word.

3.2.7 Secondary FIFO Buffer

The encoded data is stored, two words at a time, in the **Secondary FIFO**. The depth of the **Secondary FIFO** is not known exactly at this time, but will be at least 50 double words. Data may be written to the **Secondary FIFO** at a rate of one double word every two clock cycles (every 4nS).

The FIFO is a true "fall-through" FIFO. Data written at the "top" (input) is clocked downwards to the last unoccupied location.

Data may in principle be read from the FIFO at a rate of one double word every two clock cycles (4nS). In normal DUMAND operation, one double word is transmitted off-chip every 80nS to the Gazelle Hot-Rod laser encoder chip. In "test" handshake mode, data may be read at a rate which is limited only by the external hardware (in practice probably 20nS per word).

3.2.8 Output Encoding

The output of the **Secondary FIFO** is 34 bits (two 17-bit data words). Six bits are added to form a 40 bit output word (the Gazelle Hot-Rod chip expects 40 bit words). One extra bit flags a "null" word (see below). Four

parity bits are added, one for each 9 bits in the data. A spare bit (set to zero) completes the 40 bits.

3.2.9 Null Words

Periodically, a **Null word** is inserted in the output data, containing the clock reading (9 bits). This is used in DUMAND by on-shore circuitry which measures and corrects for clock drift. The frequency at which **Null words** are transmitted is selectable by configuration inputs to the ASIC. The exact choice of frequencies is not determined, but the rate will be approximately 100 KHz.

3.2.10 Output Word Format

The 40-bit output words are formatted as follows:

Data Words

bit numbers	*description*
0	null/data flag (zero for data)
1–17	first data word
18–34	second data word
35	not used (zero)
36	parity for bits 0, 4, 8...
37	parity for bits 1, 5, 9...
38	parity for bits 2, 6, 10...
39	parity for bits 3, 7, 11...

Null Words

bit numbers	*description*
0	null/data flag (one for **Null word**)
1–9	current time
10–35	not used (zero)
36	parity for bits 0, 4, 8...
37	parity for bits 1, 5, 9...
38	parity for bits 2, 6, 10...
39	parity for bits 3, 7, 11...

3.2.11 Output Handshaking

The output handshaking can work in two modes, as selected by the HSMOD pin.

DUMAND mode: One word is output every 80 nS. The DCLK pin outputs a 12.5 MHz clock, which drives the word clock input of the Hot-Rod chip directly.

Test mode: When an output word is ready, the DVAL output goes active. An external circuit must then assert DSTB. The ASIC will then de-assert DVAL. The output data is valid during the period while DVAL is active.

3.3 Configuration Options

Three inputs allow various special features of the digitizer to be selectively disabled for testing.

input pin	*function*
ENRO	enables 1μS roll-over words
ENNL	enables 100μS null words
HSMOD	selects output handshake mode
NRLT0,1	selects NULL-word output rate

Description of internal data in DUMAND digitizer ASIC

Inputs

ID0..ID26	input data from OMs and CMs; sampled asynchronously at 1GHz

Edge Detector

F1(26:0)	phase zero sampled data
F2(26:0)	phase one sampled data
TR	trigger: 1 indicates valid data

primary FIFOs

Fn(26:0)	phase zero sampled data
CLOCK(9:1)	clock time in 2nS units
CLOCK(0)	clock LSB (identifies phase 0/1)
OF	1 = overflow

"Tag" FIFO

D0	1 = valid data in FIFO 1
D1	1 = valid data in FIFO 2
R	1 = a roll-over word
V	logical "OR" of D0+D1+R

Encoder Output

CHAN(4:0)	channel number 0..26 or 31
CLOCK(9:0)	clock time or aux data
UD	0 = falling edge; 1 = rising edge
OF	1 = primary FIFO overflow

Second FIFO

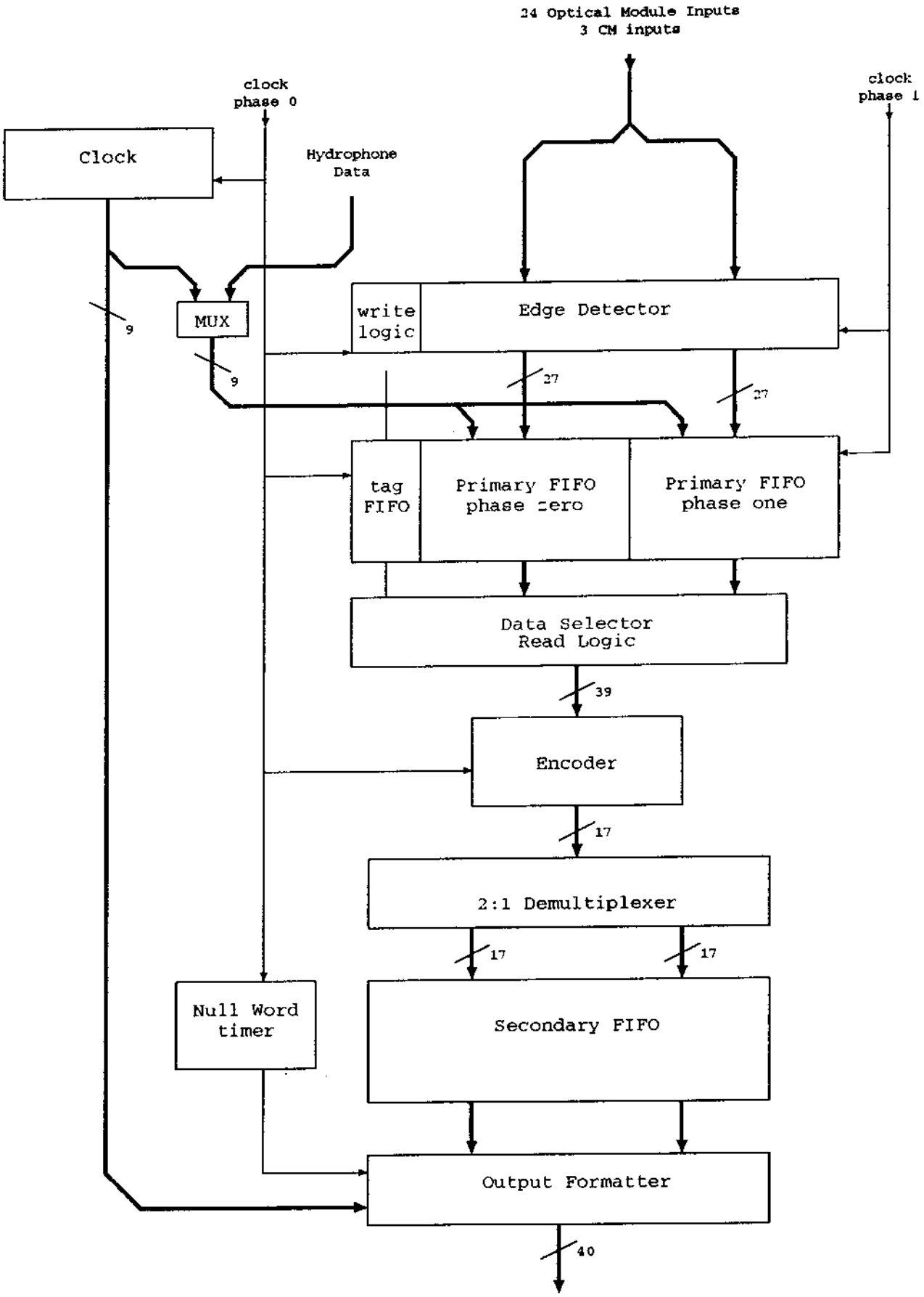
WORD1(16:0)	17 bit word #1 (format as "Encoder Output")
WORD2(16:0)	17 bit word #2 (format as "Encoder Output")
OF	1 = second fifo overflow

Hot-Rod encoder output (normal data)

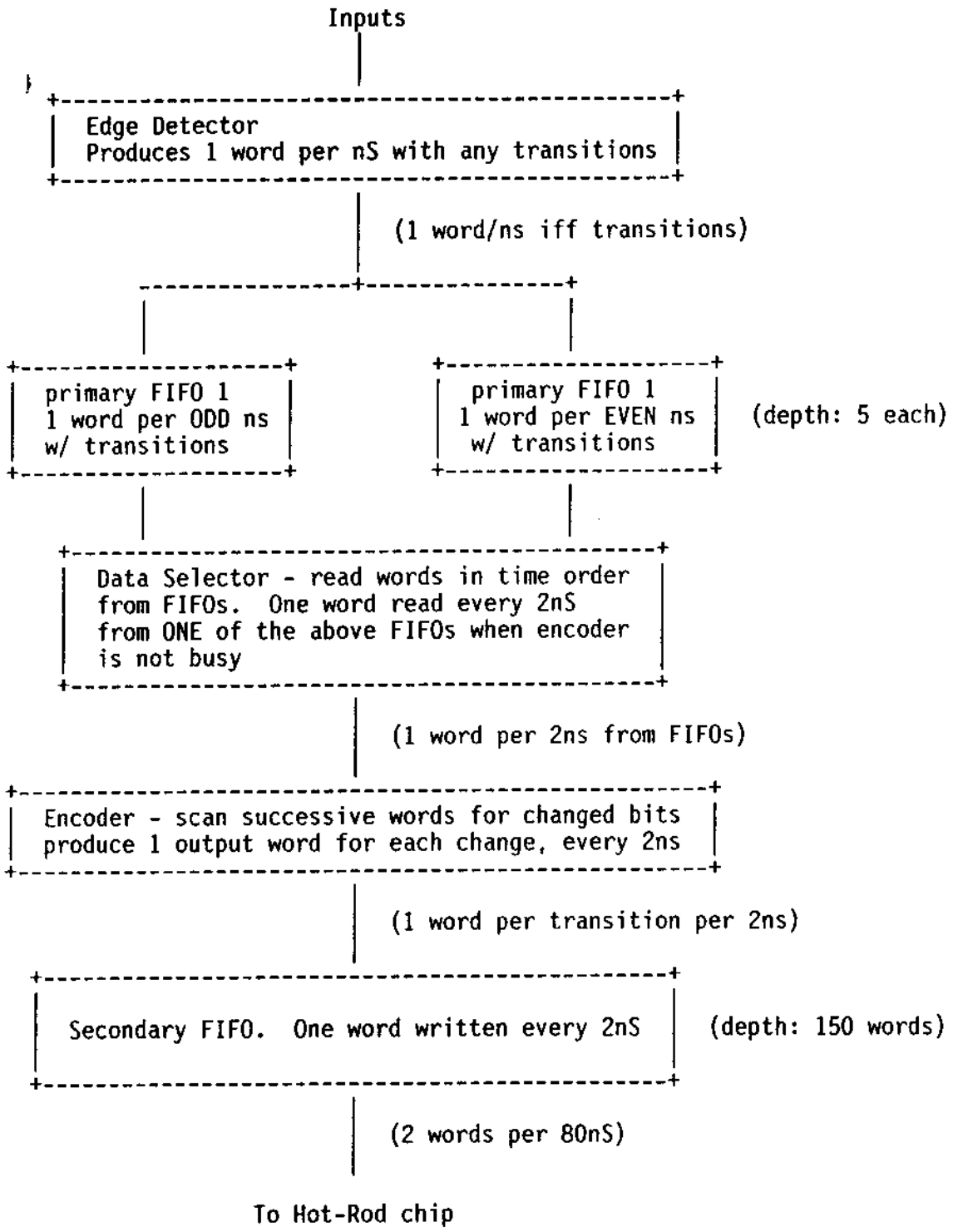
WORD1(16:0)	as above
WORD2(16:0)	
OF	
0	indicates normal data
PARITY(3:0)	parity

Hot-Rod encoder output (NULL word)

CLOCK(8:0)	clock time
1	indicates NULL word
PARITY(3:0)	parity


24 Optical Module Inputs
3 CM inputs
clock
phase 0
clock
phase 1
Clock
Hydrophone
Data
MUX
9
9
write
logic
Edge Detector
27
27
tag
FIFO
Primary FIFO
phase zero
Primary FIFO
phase one
Data Selector
Read Logic
39
Encoder
17
2:1 Demultiplexer
17
17
Null Word
timer
Secondary FIFO
Output Formatter
40

DUMAND Digitizer Queueing



DUMAND Digitizer ASIC internal data formats