DIR-2-91

DUMAND SBC FAST DIGITIZER DESIGN REPORT

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Abstract

This report describes the electronics requirements for the DUMAND fast SBC digitizer. A possible implementation of the digitizer as a large ASIC (application-specific integrated circuit) is presented. Engineering and ASIC manufacturing cost estimates are presented.

Contents

Chapter 1

Summary

The SBC (String Bottom Controller) must digitize signals from 24 OMs (Optical Modules) on a string in the DUMAND detector. The OM signals are digital, with the pulse height encoded as time-over-threshold. The SBC digitizer measures the arrival time to 1nS and transmits a data word to shore.

The SBC must handle bursts of very high rates on it's inputs, although the average rate is low. We calculate a worst-case burst of 96 words at an average rate of about 4 nS per event. This was calculated for a single muon traveling directly downwards near a string, producing a double hit in every OM. The proposed design can handle a burst of 120 words at a rate of 2nS per word.

In addition, the SBC digitizer must be extremely reliable. Assuming a desired MTBF (mean time between failures) of 10 years for the array, each SBC must have a MTBF of 100 years! We have studied the reliability of the technologies we propose to use in the digitizer and believe that they meet our requirements.

We have studied the digitizer requirements in detail, and believe that the most reliable way to implement it is in a large ASIC (Application-Specific Integrated Circuit). At least two ASIC technologies are currently available (GaAs and Silicon ECL) which allow us to integrate the entire digitizer on a single IC. We describe in detail our proposed design, and present representative quotations from vendors of each technology.

We have estimated the cost of producing the SBC digitizer ASIC, both the direct costs of purchasing the ICs, and the engineering required. The costs are summarized in Section 4.

We believe that Boston University is well qualified to successfully complete the design and manufacturing of the SBC digitizer electronics.

Chapter 2

SBC Digitizer Requirements

2.1 Performance

2.1.1 General Requirements

The SBC digitizer must meet several basic requirements, as summarized in Section 1 above. We describe them in more detail here.

The SBC must digitize pulses from 24 OM's and 3 CM's with a least count of .98 nS ($1\mu S/1024$) [hereafter referred to as "1nS" and "1GHz" to keep things simple]. Both leading and trailing edges of each pulse are digitized. Any arbitrary signal on the inputs can be digitized, provided that the total number of input transitions doesn't exceed the internal buffer size. 7 auxiliary inputs (for hydrophones, etc) are sampled at 1MHz.

The data for an entire string is transmitted to shore on a fast fiber-optic link. The digitizer must provide multiplexing to send the data for 24 OMs on a single fiber.

The trigger processor at the shore station requires that the data be received in time-order, so any multiplexing scheme must preserve the ordering of the data across multiple input channels.

2.1.2 Rates and Buffering

The most expensive part (in terms of logic complexity) of the digitizer is the internal buffer, therefore we have done extensive work to determine the minimum safe buffer size and required buffer readout rate.

First, a simple analysis of the worst-case hit rate. This occurs, it turns out, when a muon travels downward at 48 deg degrees, thus emitting Cerenkov

light directly downwards parallel to a string, illuminating each OM in turn. The delay between hits is:

Given:	OM spacing	= 10m	
	speed of Cerenkov light	= (3/4)c	$(2.24 \cdot 10^8$ m/sec)
	speed of signal in optical fiber	= (2/3)c	$(1.99 \cdot 10^8$ m/sec)
Then:	photon time of flight	= 44.6 nS/10m	
	signal time of flight	= 50.3 nS/10m	
	time between hits	= 5.7 nS	

Determining the required buffer depth is complex. We have performed extensive computer simulations, and present our results in *Dumand Internal Report* DR-1-91. Our prelimary results show that buffer depths of five for the first buffer (FIFO #1) and 100 for the second buffer (FIFO #2) are adequate, but more simulation work is required.

2.2 Proposed Design

This section gives a quick overview of our proposed digitizer design. For more detail, see Appendix A.

The OM and CM data comes in on optical fibers. The fibers connect to optical receiver boards, which plug into the main fast SBC board. The output of the optical receiver cards are differential ECL signals, which feed directly into the digitizer chip.

The fast digitization is accomplished by semi-custom ICs. The OM and CM data is fed directly to the digitizer, along with a 1GHz master clock. The output of the digitizer feeds directly to a serializer-encoder (perhaps the Gazelle Hot Rod) chip, and then to a laser driver.

On-chip buffering is provided for >100 events, to handle bursts. The worst-case burst expected is one double pulse on each of the 24 OM inputs, within approximately 400 nS.

For each transition, a 10-bit time word, 5-bit channel number, and 1 bit up/down flag are transmitted, making a 17-bit data field. Every $1\mu S$ (when a carry occurs from the 10th time bit), a roll-over word with channel number = 0 is transmitted. The time field of roll-over words is replaced by a 4-bit roll-over counter, and 7 bits of environmental data). An overflow bit indicates lost data, if the internal buffers are full when an event occurs.

Two 17-bit data fields are combined, along with error detection bits, to form a 40-bit word. This 40-bit word is sent directly to the laser encoder (Gazelle Hot Rod chip).

When there is no data to transmit, the digitizer continuously transmits "null" words with channel number = 0 and a valid time.

2.3 Performance of Proposed Design

Here is a quick summary of the performance of our proposed design:

1. Resolution
   - 1 nS time resolution of up and down transitions on all inputs.
   - 10 bit time sent with each transition
2. Rate Capability
   - 25 MHz continuous
   - 500 MHz for bursts of 10 nS
   - 167 MHz for bursts of up to 100 events
3. Special Features
   - Periodic re-synchronization of fiber-optic link
   - Null words sent when idle to calibrate clock drift
   - Auxiliary environmental data inputs (7) sampled at 1 MHz

2.4 Reliability

The entire SBC system should have a MTBF (mean time between failures) of at least 100 years. Assuming linear failure rate, this gives a 10% probability of failure of one string in 10 years (in a 10-string detector). We have yet to do a detailed study of the reliability requirements for the digitizer.

It appears that the reliability of the digitizer ASICs will not be a problem. The reliability of large ASICs is well documented, particularly for ECL. Failure rates are typically given in units of a FIT (failure in time), where 1 FIT = 1 failure/10^9 hours. Typical stated failure rates for ECL ICs are less than 10 FITs, and for GaAs, less than 100 FITs. A 100 FIT failure rate corresponds to 1 failure / 10^5 years.

Chapter 3

Engineering Reccomendation

3.1 ASIC Technologies

We propose to use ASICs to integrate most of the fast SBC electronics. The digitizer could possibly be built using discrete logic, but it would require a large number of ICs, and it is extremely difficult to achieve 1 GHz or even 500 MHz operation with discrete ICs on a printed circuit board.

An ASIC is a custom IC fabricated from a logic design made up of simple, tested, standard elements from a library supplied by the manufacturer. The design of an ASIC is quite similar to the design of a logic circuit on a PCB, but the IC vendor worries about the "hard" part—the physical layout. Once the logic design is accepted by the manufacturer, they guarantee success; that is they guarantee that the IC produced will meet our specifications.

Several technologies, summarized in the table below are used to produce fast ASICs.

	DELAYS (ps)		Max recomm.	Complexity	Usable Speed
	Gate	Flip-Flop	Clk speed	(gates)	(in SBC)
1. ECL (1.5u)	200pS	400pS	1.2 GHz	≈30K	660 MHz
2. ECL (.8u)	100pS	200pS	≈2 GHz	80K	1.3 GHz
3. GaAs (SCFL)	100pS	200pS	2 GHz	6K–10K	1.3 GHz
4. GaAs (1.5u)	175pS	500pS	1 GHz	≈30K	650 MHz
5. GaAs (.8u)	125pS	350pS	600 MHz	60K	580 MHz
6. CMOS (.8u)	500pS	1nS?	200MHz?	>100K	260 MHz

1. Silicon Emitter-Coupled Logic. Old technology, power-hungry. Proven.
2. .8μm ECL. Quite new, but straightforward scaling of existing technology.
3. Gallium Arsenide Source-Coupled FET Logic. Relatively new; somewhat lower power than ECL. Electrically quite similar to ECL. Fastest production ASIC technology.
4. Gallium Arsenide Direct-Coupled FET Logic. Substantially lower power than ECL, comparable speed. 1.5μm feature size has existed for several years.
5. Gallium Arsenide DCFL, .8μm feature size. Newly introduced by Vitesse semiconductor. Although this logic is in principle fast enough to run at >1GHz, the physical characteristics of the IC package limit it's speed to 580 MHz.
6. Silicon Complimentary Metal-Oxide Semiconductor. Old technology, but specs given are for state-of-the-art .8μm feature size. Still not quite fast enough for us.

3.1.1 Speed

The Usable Speed is my estimate of the maximum speed we could operate the SBC digitizer at if built using the technology, calculated as follows:

$$\text{max speed} = ((\text{FF delay}) + (3 \cdot \text{Gate delay})) \cdot \text{derating factor}$$

This assumes that a maximum of 3 levels of combinatorial logic are required between flip-flops. The derating factor (typically 1.5) is for IC manufacturing process variations, operating temparature variations, etc. See Note 5 below for a special note on 0.8μm GaAs.

3.1.2 Density

The "complexity" column is the approximate number of simple gates (i.e. 2-input OR) which can typically be fabricated on a single chip. We estimate that the current design will require approximately 40,000 gates (assuming one chip per string).

3.1.3 Summary

3.2 Design Partitioning

A 1GHz digitizer can be implemented in at least two ways. The first is a single ASIC containing the entire digitizer. This currently appears possible only with 0.8μm ECL technology. An attractive alternative is to use SCFL GaAs for the digitizer itself, and a second, lower–speed technology for the large memory buffer. We are currently exploring this possibility. If the digitizer and buffer memory are implemented separately, about 15,000 gates are needed for the digitizer, and 25,000 for the buffer memory.

3.3 In-House Engineering Requirements

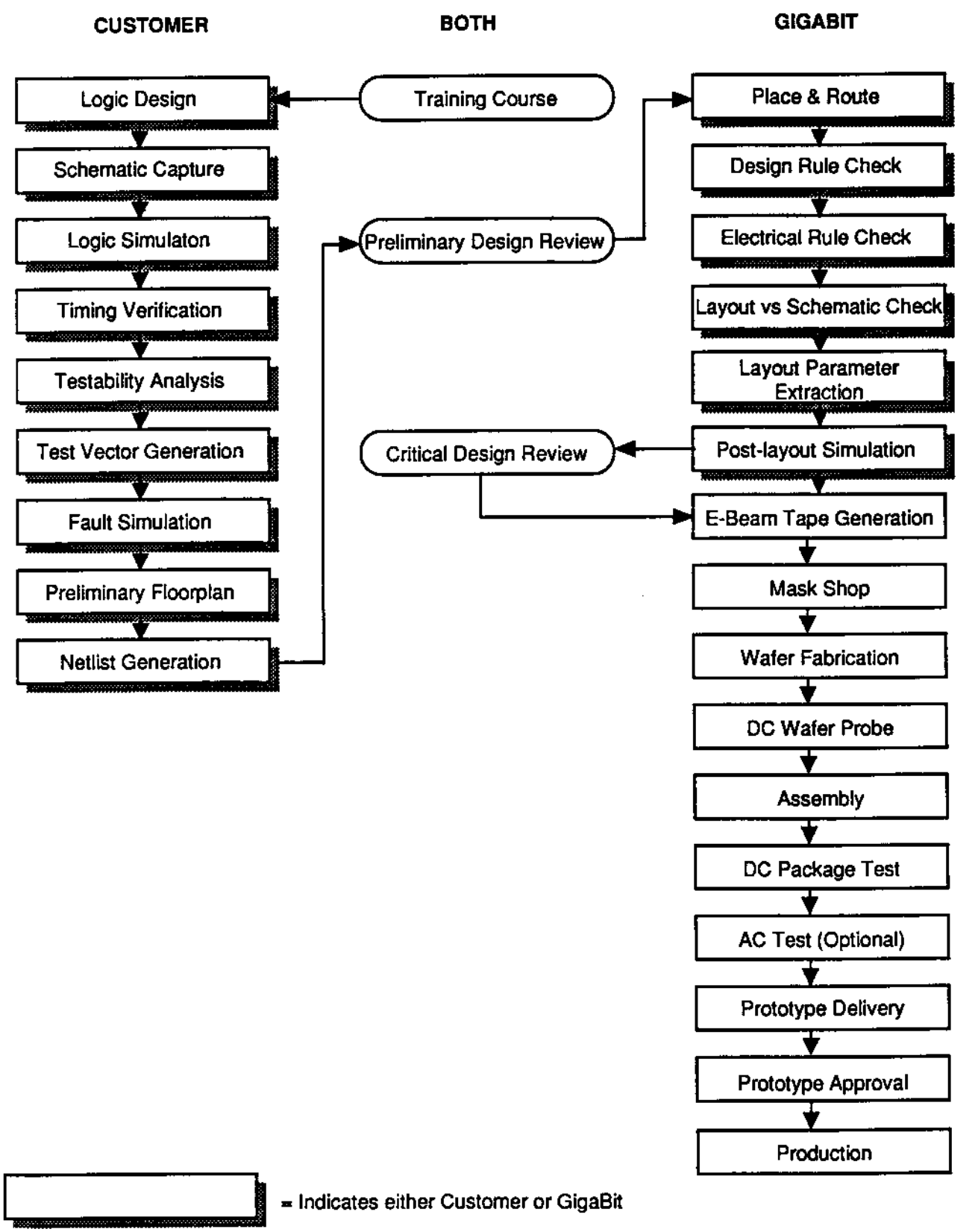
Figure 3.1 shows the typical design path for an ASIC. The diagram shown is from GigaBit Logic, but is quite similar for most vendors. The left column shows tasks typically performed by the customer, namely us. A CAE (Computer-Aided Engineering) system, running on a fairly high-powered workstation, is required to perform most of the steps. An IBM-PC based system would not be appropriate.

Software required is as follows:

- **Schematic Editor** (required) for capture and editing of schematic diagram
- **Logic Simulator** (required) for simulation and timing verification
- **Test Vector Generator** (optional) helps generate test vectors to verify correct operation of the simulation and actual ICs.
- **Fault Simulator** (optional) simulates failure of each logic element in the IC to test coverage of test vectors

After the design simulation is correct and the test vectors are prepared, a tape containing the design files is delivered to the IC vendor. They then produce a physical layout of the logic elements in the IC, and produce a back-annotation file. This allows a detailed simulation, taking into account the actual time delays produced by the interconnections on the IC itself. After this simulation, the ICs are fabricated by the vendor.

DESIGN & DEVELOPMENT FLOW



3.4 Capabilities at B.U.

The EDF at Boston University is equipped to handle most of the engineering required to produce an ASIC. We have a Mentor Graphics IDEA system, running on Apollo workstations. It would be advisable to purchase test vector generation and fault simulator software from Mentor prior to beginning the design work.

3.4.1 Consulting Recommendations

We suggest that a consultant be hired to perform at least one, and preferably two design reviews. The IC vendor will provide a lot of engineering support during the design process, but it is useful to have the design evaluated by an experienced third party periodically.

3.5 Engineering Labor Estimate

We estimate that the design and production of the ASIC will take approximately 1 man-year of engineering. This breaks down as shown in the table below. This includes all work required after a final choice of vendor is made.

In addition, a test board will be required to test the ASICs once they are delivered. Probably the PCB will be usable in the SBC itself with some modifications. We do not have enough detailed information on the overall SBC design to accurately estimate the cost of the final PCB design.

Task	Time (man-weeks)
ASIC Engineering	
basic (paper) design	14
schematic editing	8
simulation	12
add features for testability	7
generate test vectors	5
Test PCB Engineering	7
Prototype Testing	5
TOTAL	58

Chapter 4

Conclusions

In summary, we believe that the design of the DUMAND SBC digitizer is relatively straightforward with today's fast ASIC technologies. We see two possible options for the actual digitizer:

- A single-chip design using 0.8μm Silicon ECL technology. This would probably be the most reliable.
- A two-chip design using GaAs. The fast SCFL logic family would be used for the digitizer itself, and the slower DCFL family for the memory buffer. This would consume about half the power of the ECL design, and would cost somewhat less.

Appendix A

Detailed Description of Proposed Design

A.1 Front-End (edge detector)

The first task of the digitizer is to synchronize the 27 inputs (24 OMs + 3 CMs) with the 1 GHz clock, and to detect rising and falling edges. This is accomplished with several latches and an exclusive-or (XOR) gate on each input channel. Edge detection is done by XORing two successive samples of an input. The XOR output is high when the two samples differ, indicating that the input has changed state. A 27-input OR gate senses when an edge is present on any of the 27 input channels, producing the TRIGGER signal. The XOR outputs are used only to generate the trigger signal. The output from this stage is 28 bits:

1	TRIGGER
27	OM data

A.2 Time Stamp

The arrival time of each hit (TRIGGER) is recorded to 1nS accuracy. A 14-bit synchronous counter runs continuously at 1GHz, and the low 10 bits are latched on each TRIGGER. When a carry occurs from the 10th bit (every 1uS), a word is latched with a flag set to indicate roll-over. If a trigger is present when roll-over occurs, OM data is recorded as usual.

A.3 Roll-Over Words

When a clock roll-over occurs (every 1μS), 6 external inputs are latched, along with the upper 4 bits of the clock synchronous counter. These 10 bits replace the 10 bit time word data.

The data stream at this point consists of:

1	TRIGGER
27	OM data
10	time word (or auxiliary input data)
1	roll-over flag

If there are changes on any of the OM inputs, the data is recorded as usual in the "OM data" portion of the word.

A.4 FIFO buffer #1

The first FIFO buffers the raw OM data (one bit per OM input). This buffer is required to handle hits on more than one OM input at a time.

A 39 (1+27+10+1) bit word is written into the FIFO on each TRIGGER or roll-over. The FIFO may be full when data is to be written. If so, no data is written, but a LOST DATA flag is set in the top word on the FIFO. In addition, a single free location is always reserved for roll-over words at the input to the FIFO, guaranteeing that no roll-over words will be lost.

The depth of this fifo can be quite small, probably 5 or 10 words.

A.5 Change Register

Each output word from FIFO #1 is clocked into two latches in series. An XOR gate on each bit identifies which bits (each corresponding to an OM input) have changed. The output from this stage is two 27 bit words; the first identifies which inputs have changed state, the second records the direction of the change.

A.6 Channel Number Encoder

The Change Register output feeds an encoder, which scans the change register for 1 bits. Each time one is found, an output word is built, with the

current time stamp. A priority encoder converts the 1-of-27 input from the change register into a 5-bit binary channel number. The channel number is used to select the appropriate bit from the direction register for output.

When the roll-over flag is set, a word is built with channel number 0, and auxiliary data in the clock field. If any bits are set in the change register, normal data words are also built, with the clock field set to 0.

A.7 FIFO #2

The output from the channel encoder is stored in FIFO #2, which is 17 bits wide by about 100 words deep. Hits are transferred in every 2nS from the channel number encoder. Hits are removed from FIFO #2 and transmitted (in pairs) to the Hot-Rod encoder every 80nS (per pair).

A.8 Output Data Format

The Hot-Rod chip transmits fixed length 40-bit words. A 40-bit word is built from two 17 bit data words, a flag bit to indicate a Null Word (see Section A.9) below, four parity bits, and a spare bit. The output words are formatted as follows:

Data or Roll-Over Words

bit	Description
0-16	data field #1 (earlier in time)
17-33	data field #2
34	spare (not used)
35	1=null word 0=data word
36	parity for bits 0,4,8...
37	parity for bits 1,5,9...
38	parity for bits 2,6,10...
39	parity for bits 3,7,11...

Data Field Details

bit	Data	Roll-Over
0–4	channel	zeroes
5	up/down	-not used-
6–15	t_0–t_9	t_{10}–t_{13}, aux_0–5
16	overflow	overflow

Null Words

bit	Description
0–4	t_{10}–t_{14}
5	-not used-
6–15	t_0–t_9

The bit names in the above tables are defined as follows:

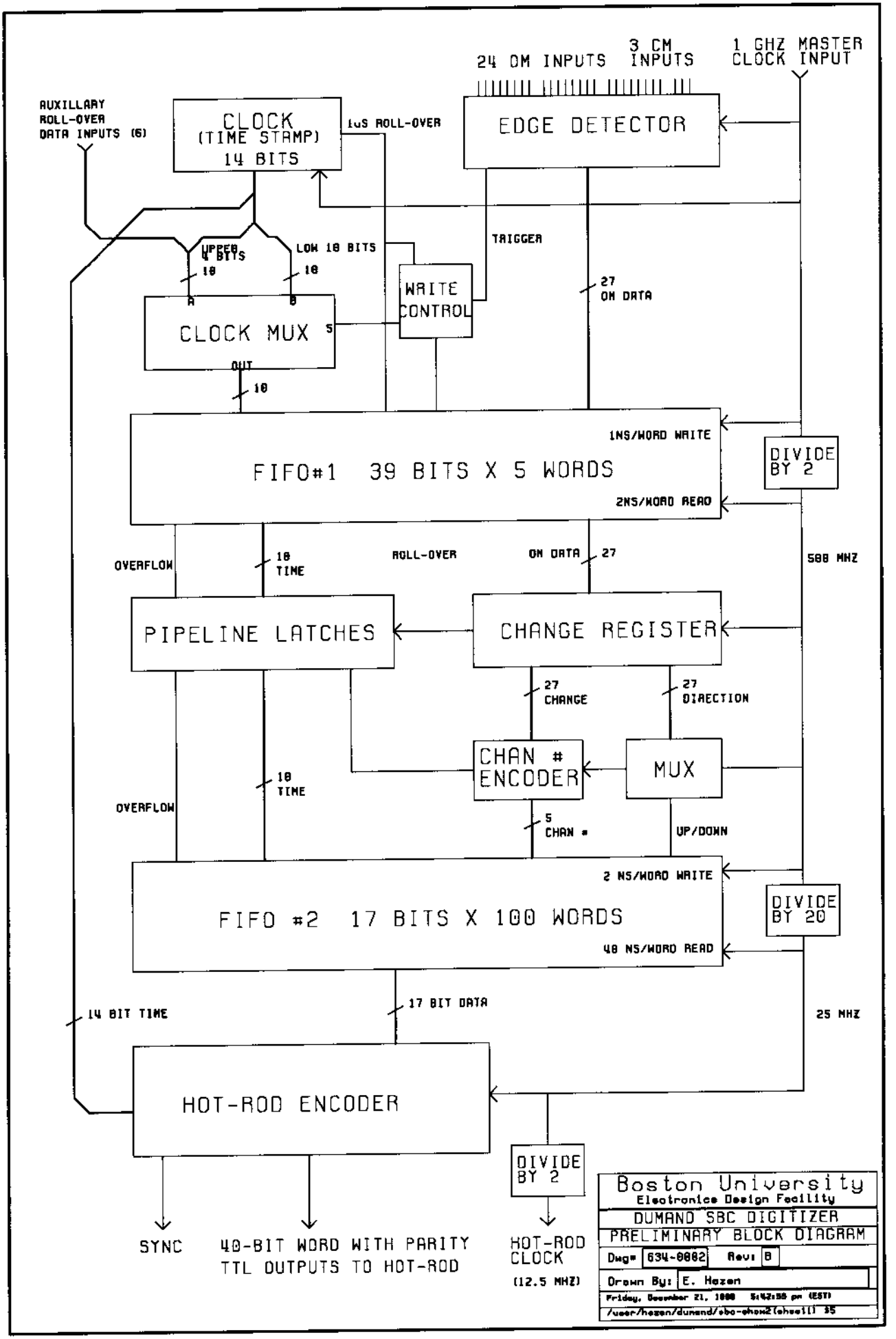
bit	description
t_n	clock time to 1nS
aux_{0-4}	hydrophone data
aux_5	SBC computer data to shore

A.9 Null Words

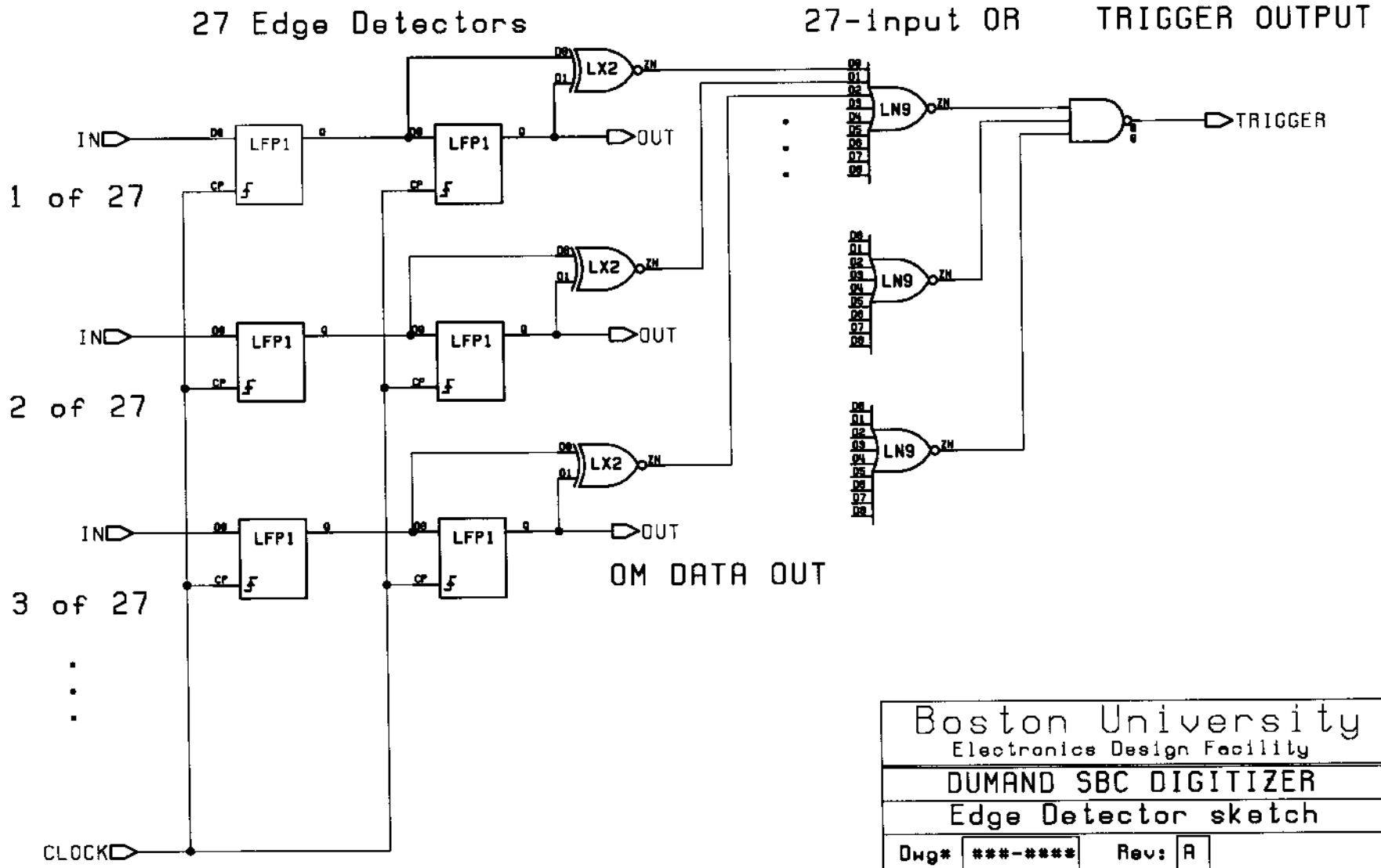
Whenever FIFO #2 is empty, a null word is transmitted, containing 14 bits of time. A bit is set to flag null words. The null word replaces the low 17 bits of the 40-bit word. Bits 17-33 are set to zeroes.

Appendix B

Drawings of a Possible Implementation

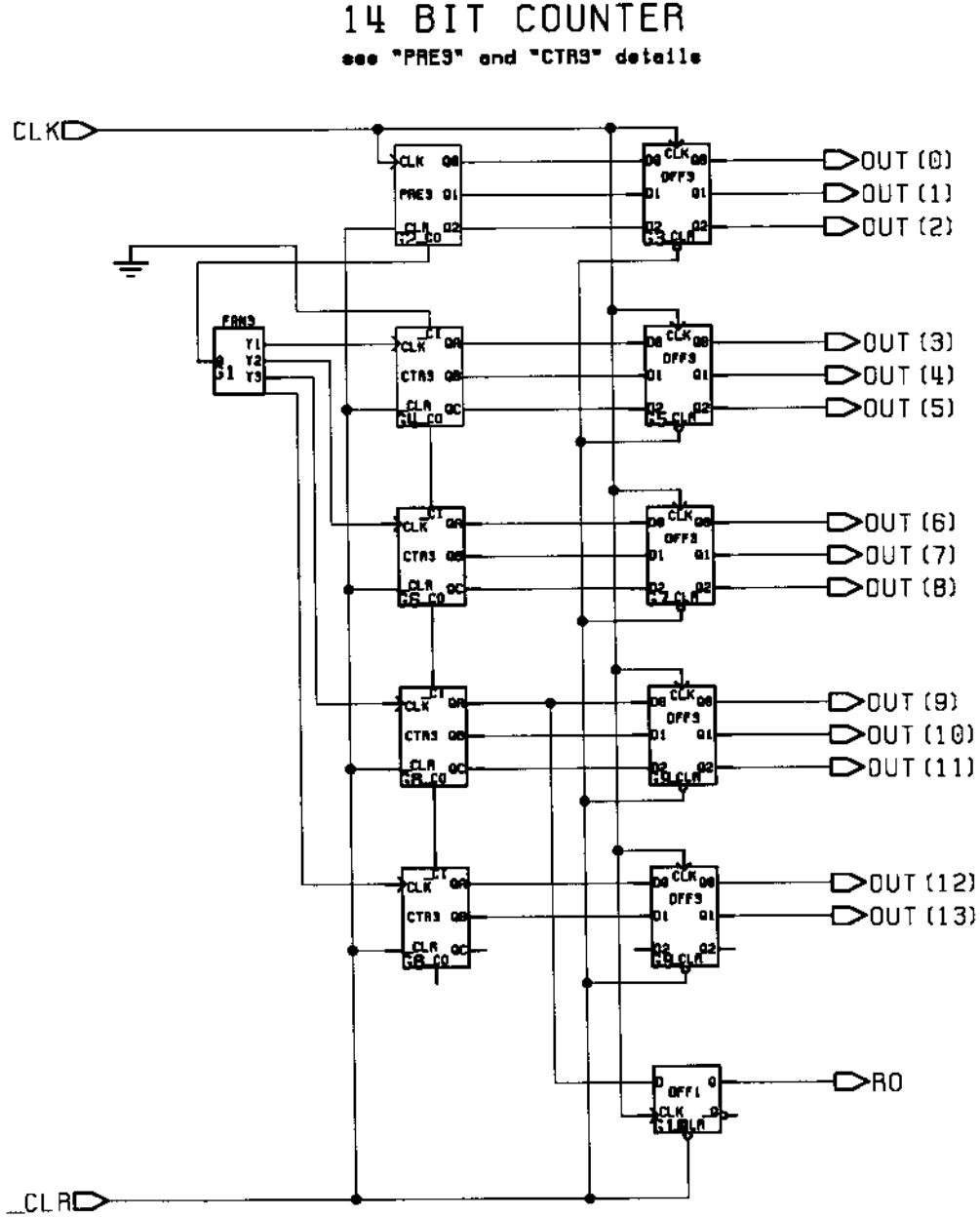

24 OM INPUTS
3 CM INPUTS
1 GHZ MASTER CLOCK INPUT
AUXILLARY ROLL-OVER DATA INPUTS (6)
CLOCK (TIME STAMP) 14 BITS
1uS ROLL-OVER
EDGE DETECTOR
TRIGGER
UPPER 4 BITS
LOW 18 BITS
18
18
A
B
WRITE CONTROL
27 OM DATA
CLOCK MUX
5
OUT
18
1NS/WORD WRITE
FIFO#1 39 BITS X 5 WORDS
2NS/WORD READ
DIVIDE BY 2
OVERFLOW
18 TIME
ROLL-OVER
OM DATA
27
500 MHZ
PIPELINE LATCHES
CHANGE REGISTER
27 CHANGE
27 DIRECTION
CHAN # ENCODER
MUX
OVERFLOW
18 TIME
5 CHAN #
UP/DOWN
2 NS/WORD WRITE
FIFO #2 17 BITS X 100 WORDS
48 NS/WORD READ
DIVIDE BY 20
14 BIT TIME
17 BIT DATA
25 MHZ
HOT-ROD ENCODER
DIVIDE BY 2
SYNC
40-BIT WORD WITH PARITY
TTL OUTPUTS TO HOT-ROD
HOT-ROD CLOCK
(12.5 MHZ)
Boston University
Electronics Design Facility
DUMAND SBC DIGITIZER
PRELIMINARY BLOCK DIAGRAM
Dwg# 634-0002 Rev: B
Drawn By: E. Hazen
Friday, December 21, 1990 5:42:55 pm (EST)
/user/hazen/dumand/sbc-ohsw2[sheet1] 35

Block: Edge Detector



Boston University Electronics Design Facility	
DUMAND SBC DIGITIZER	
Edge Detector sketch	
Dwg# ***-****	Rev: A
Drawn By: E. Hazen	
Thursday, December 6, 1990 12:04:46 pm (EST)	
//ginger/local_user/hazen/dumand/vitesse/notes/edge-sketch (sheet 1) $l	

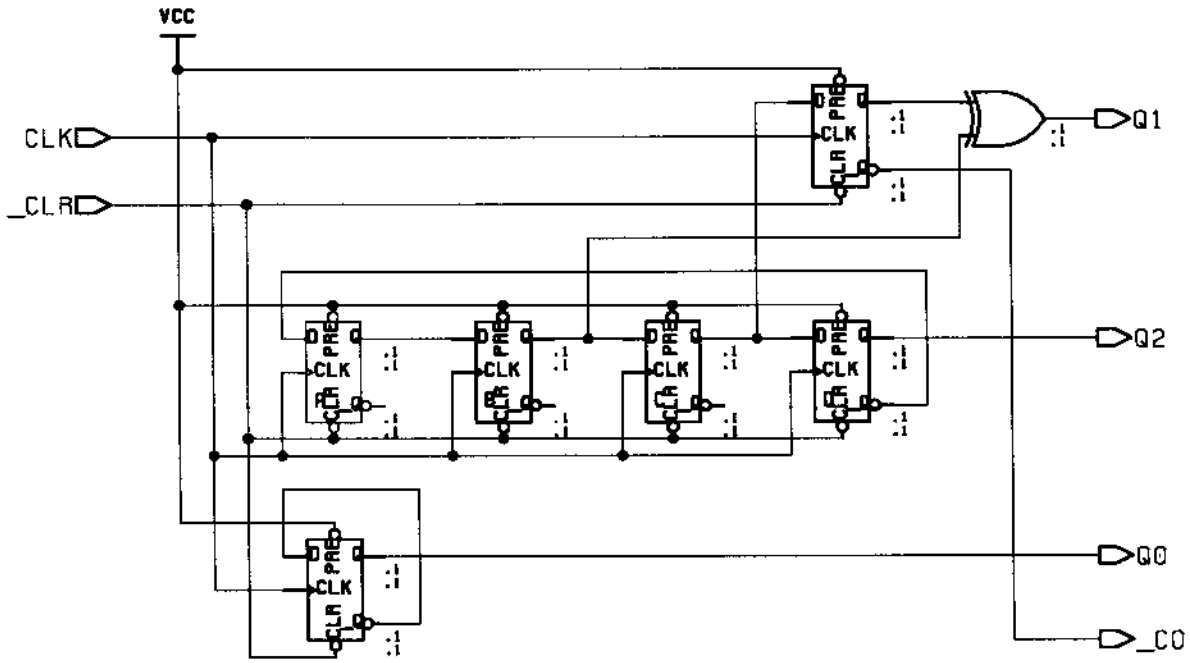
Block: Clock

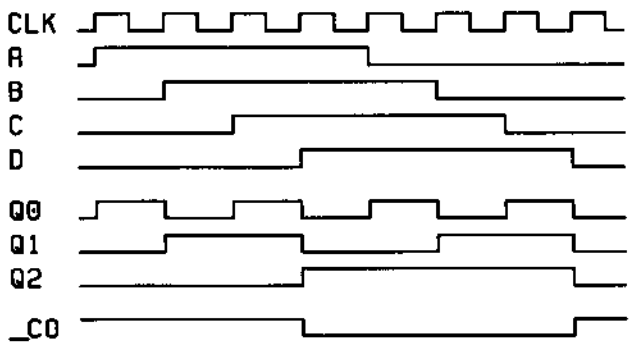


Boston University Electronics Design Facility
DUMAND SBC DIGITIZER
CLOCK DETAIL
Drawn By: E. Hazen
Thursday, December 6, 1990 2:06:43 pm (EST)
/user/hazen/dumand/sbc-generic(sheet1) $6

Block: Clock (detail)

3-BIT PRESCALER



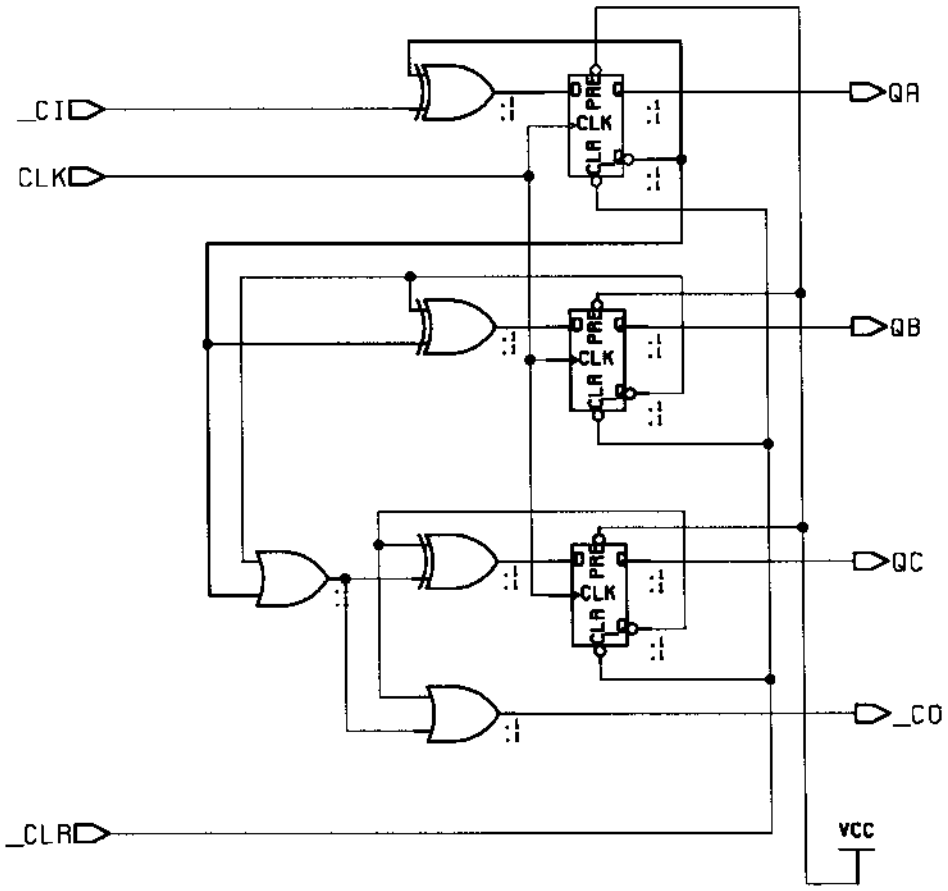


11/6/98, eeh - 100ps delays added on all outputs
_CO now in phase with Q2

Boston University Electronics Design Facility		
DUMAND SBC DIGITIZER		
Clock prescaler sketch		
Dwg# ***-****	Rev: A	
Drawn By: E. Hazen		
Thursday, December 6, 1998 2:11:46 pm (EST)		
/user/hazen/dumand/sbc-generic/design_lib/pre3(sheet1) #2		

Block: CLOCK (detail)

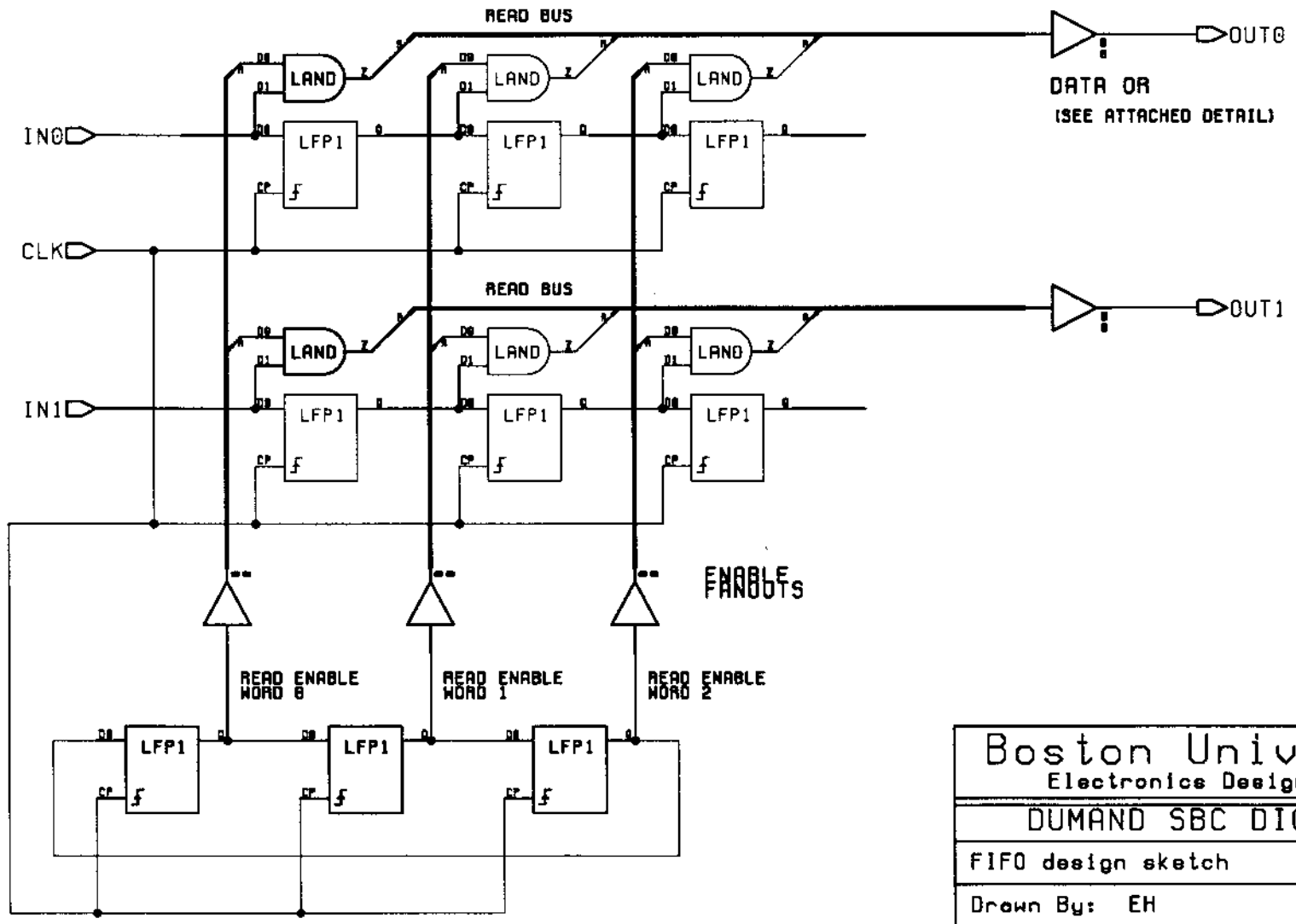
3-BIT SYNC CTR



11/6/98, esh -- added 100ps delays

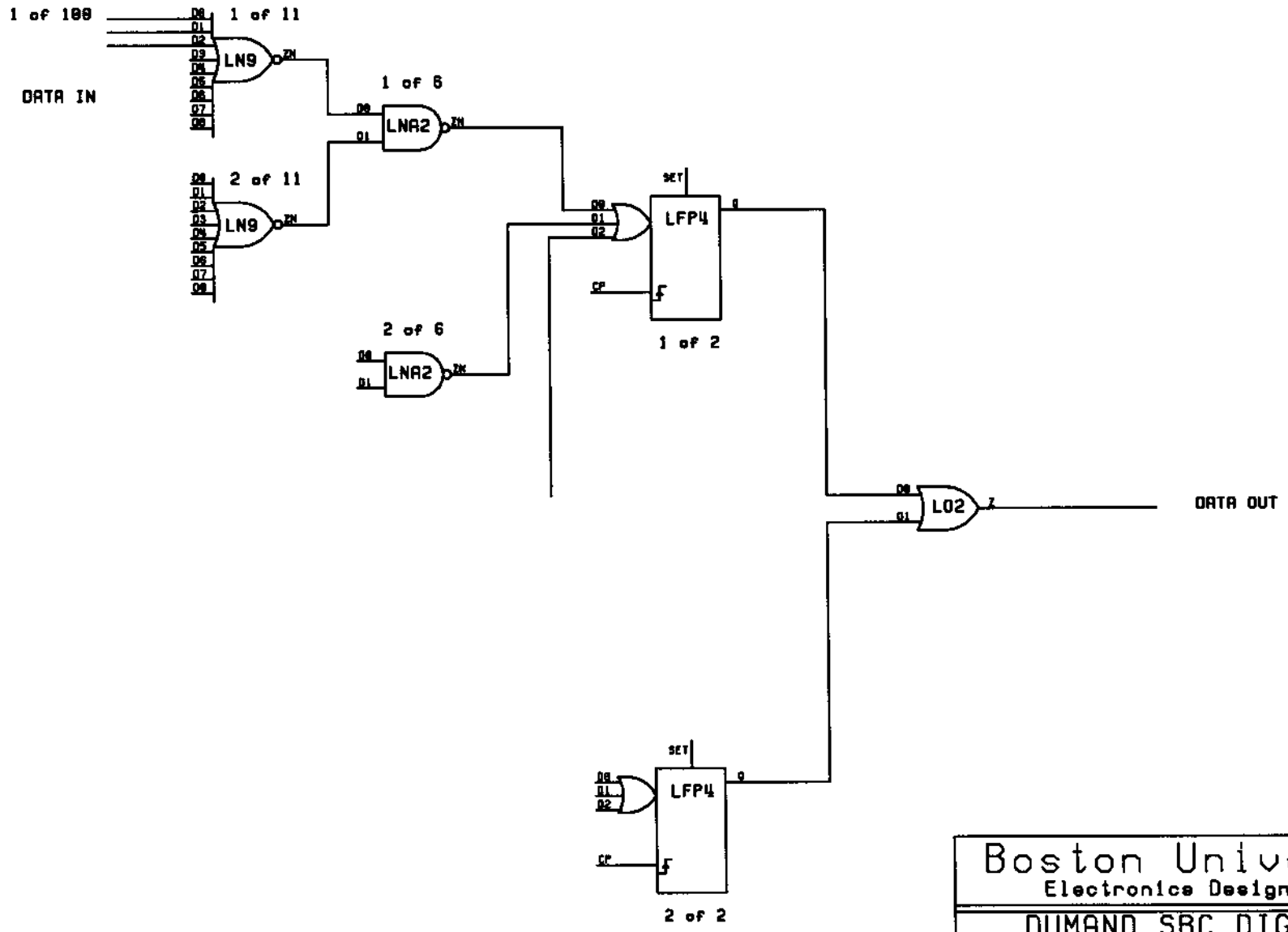
Boston University Electronics Design Facility	
DUMAND SBC DIGITIZER	
3 Bit ctr sketch	
Dwg# ***-****	Rev: A
Drawn By: E. Hazen	
Thursday, December 6, 1998 2:15:57 pm (EST)	
/user/hazen/dumand/sbc-generic/design_lib/ctr3(sheet1) #2	

Block : FIFO #1 and FIFO #2



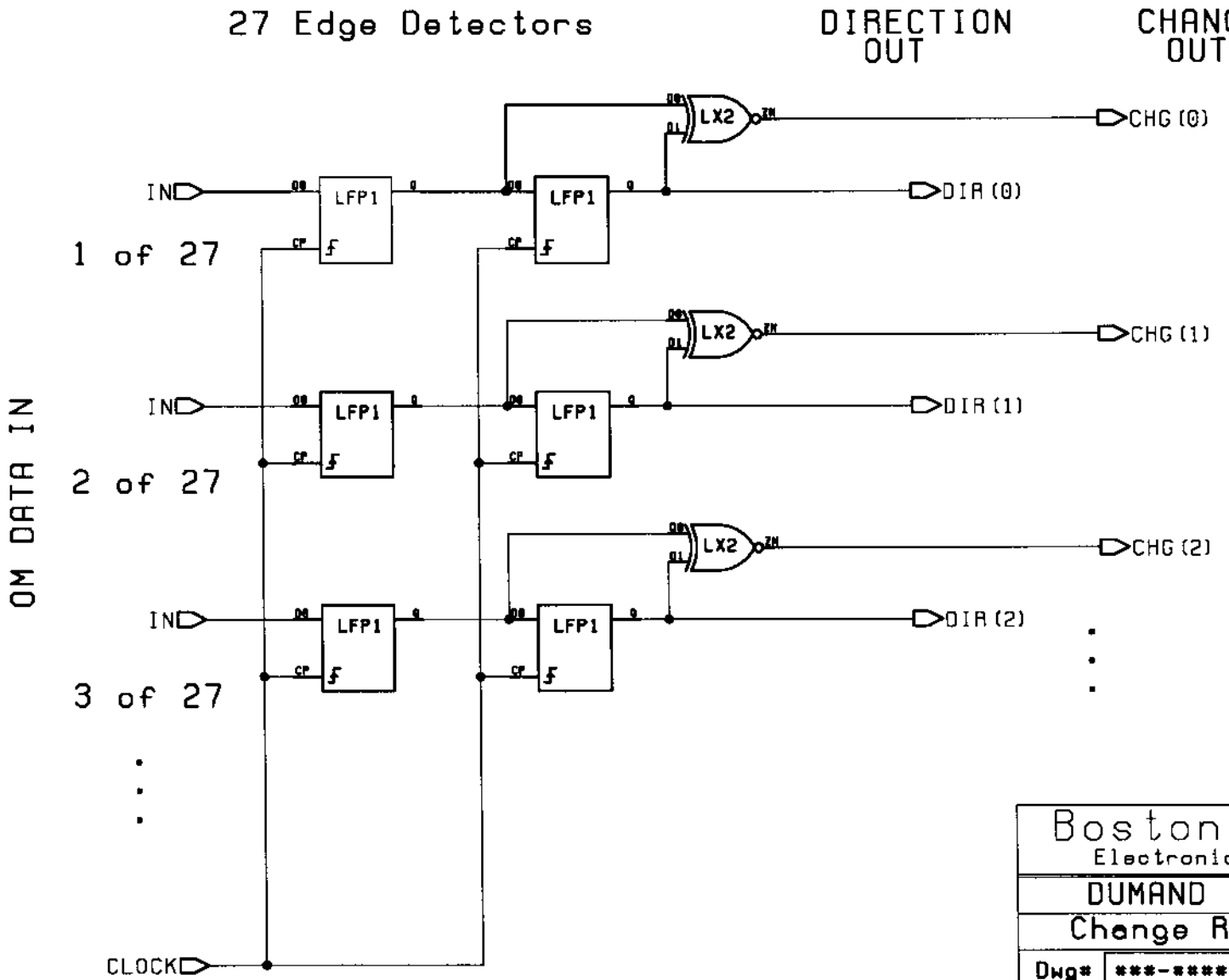
Boston University Electronics Design Facility
DUMAND SBC DIGITIZER
FIFO design sketch
Drawn By: EH
Monday, November 26, 1990 5:26:46 pm (EST)
/user/hazen/dumand/vitesse/notes/sr-sketch(sheet1) $2

Block: FIFO #2 (FIFO #1 Sim but 10 inputs)



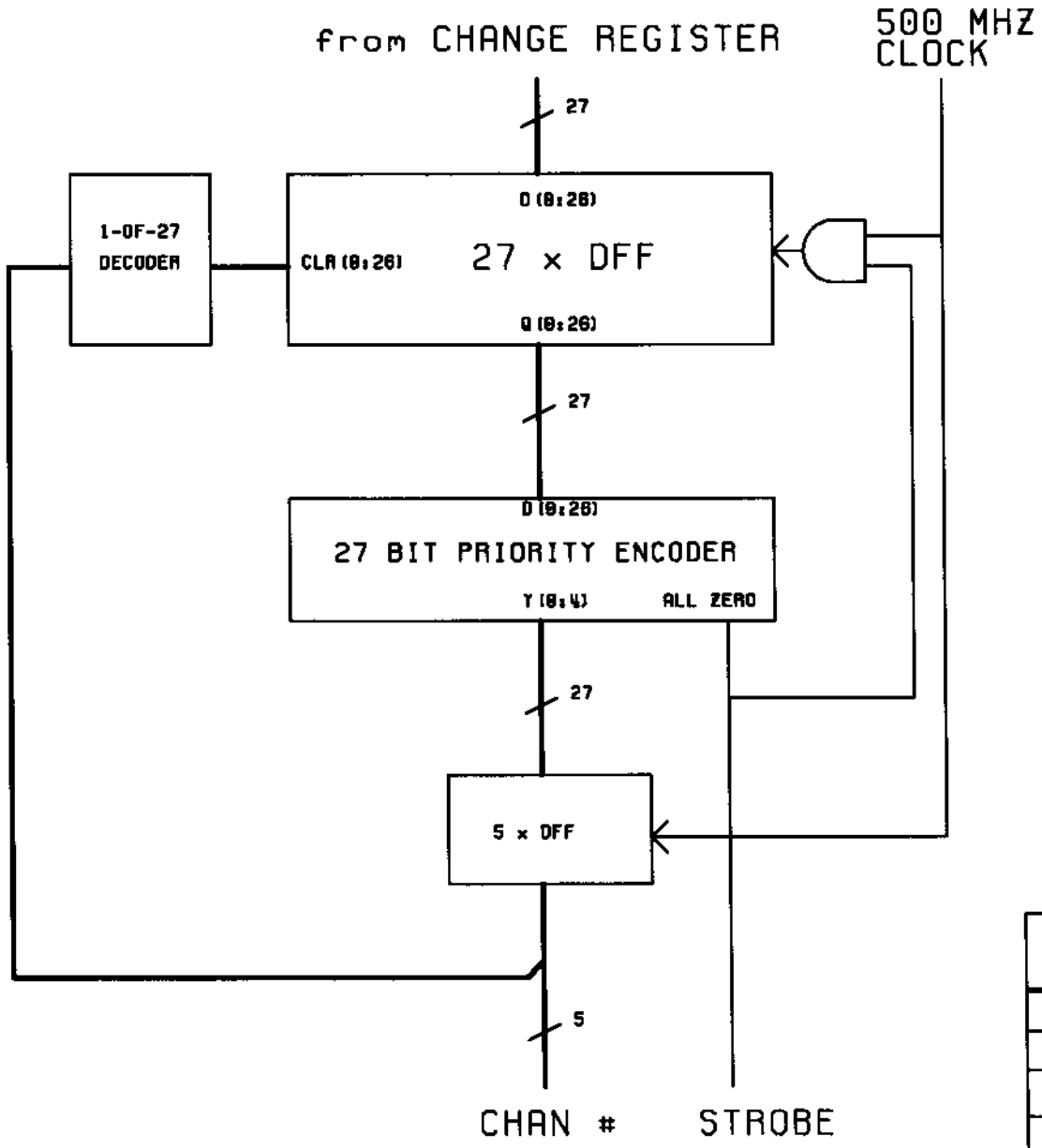
Boston University Electronics Design Facility
DUMAND SBC DIGITIZER
100:1 DATA OR sketch
Drawn By: E. Hazen
Monday, November 26, 1990 5:44:34 pm (EST)
//ginger/local_user/hazen/dumand/vitesse/notes/er100-sketch(sheet1) #1

Block: CHANGE REGISTER



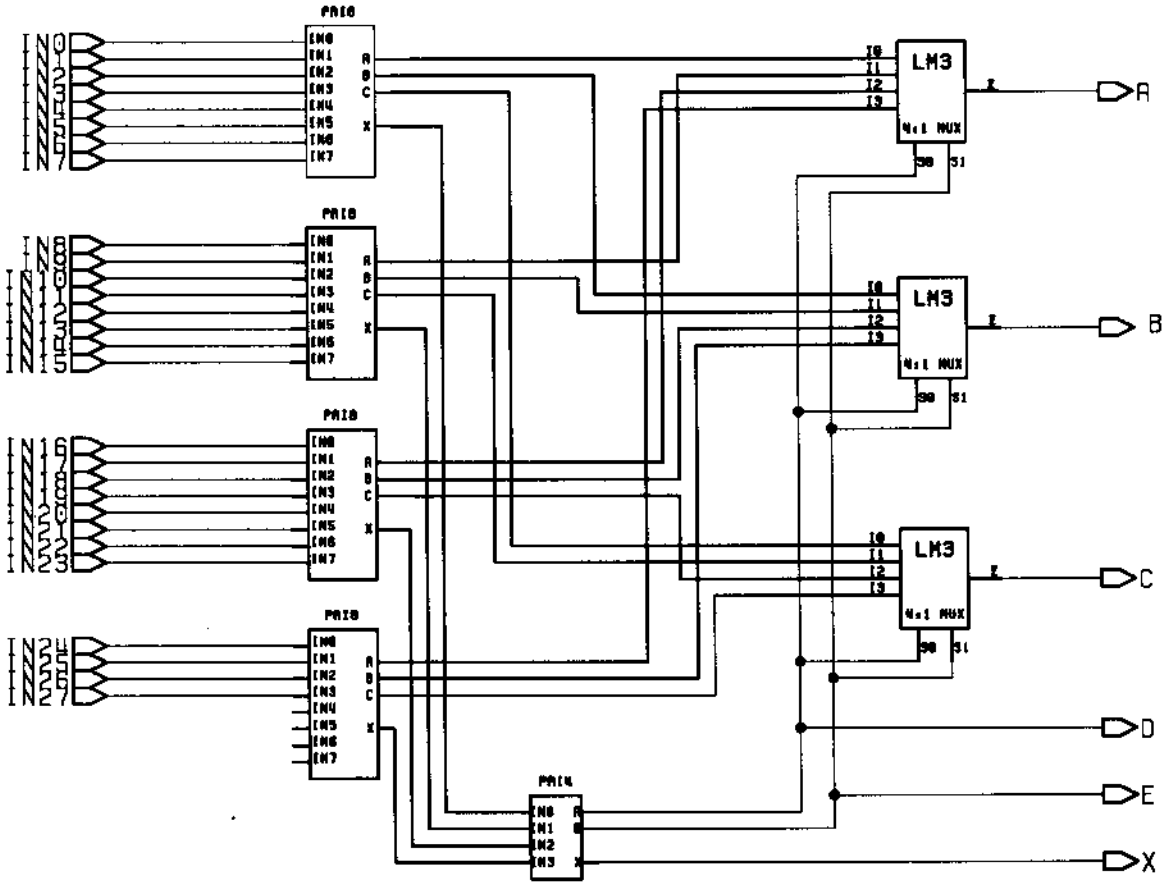
Boston University Electronics Design Facility	
DUMAND SBC DIGITIZER	
Change Register Sketch	
Dwg# ***-****	Rev: A
Drawn By: E. Hazen	
Monday, December 10, 1990 9:00:07 pm (EST)	
/user/hazen/dumend/vitesse/notes/chg-reg-sketch(sheet1) #2	

Block: CHAN # ENCODER



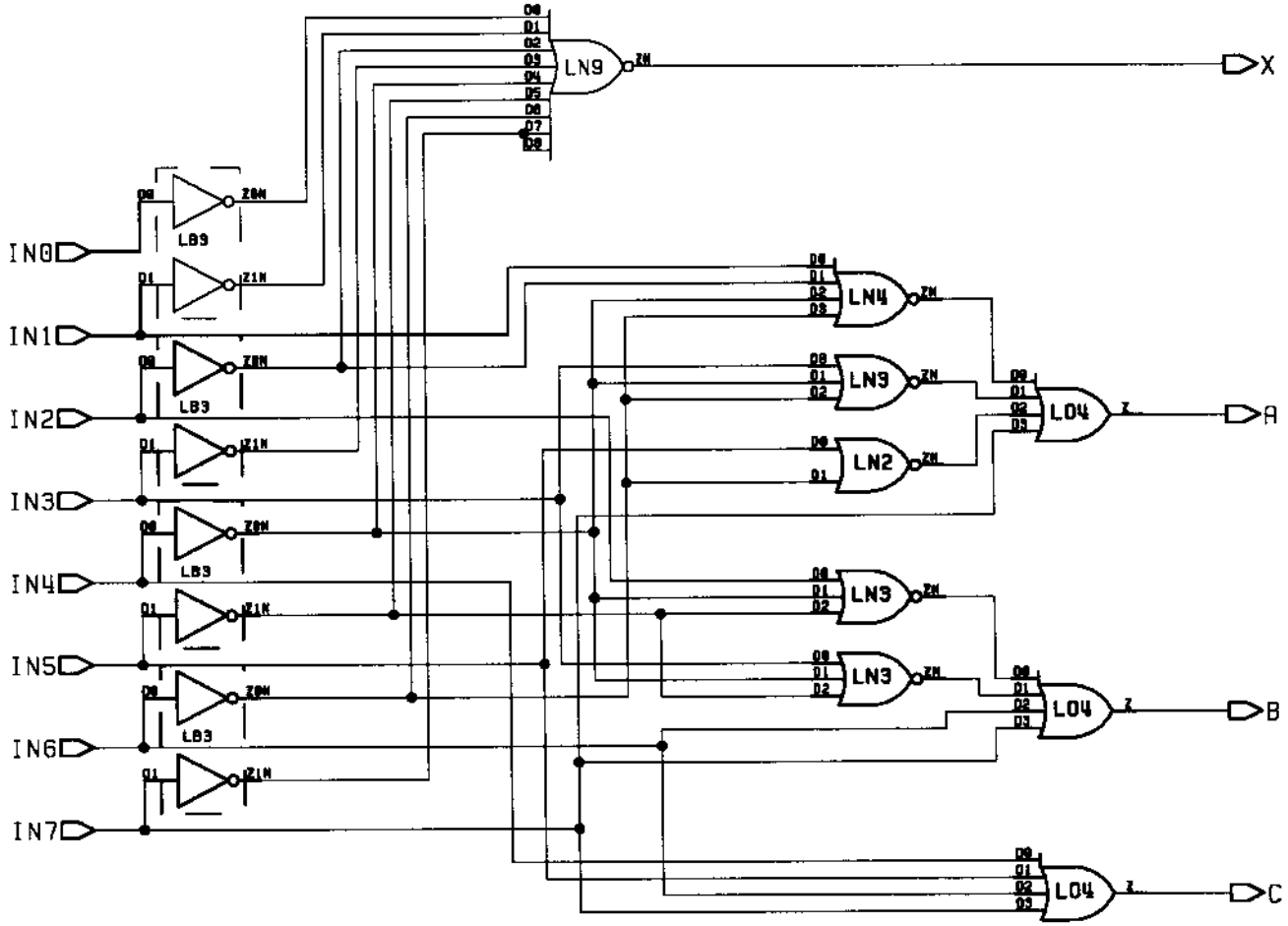
Boston University Electronics Design Facility	
DUMAND SBC DIGITIZER	
Chan # Encoder - Sketch	
Dwg# ***-****	Rev: A
Drawn By: E. Hazen	
Monday, December 10, 1990 8:48:00 pm (EST)	
//ginger/local_user/hazen/dumand/vitesse/notes/chan-enc-sketch (sheet1) #1	

BLOCK: CHAN # ENC. (Detail)



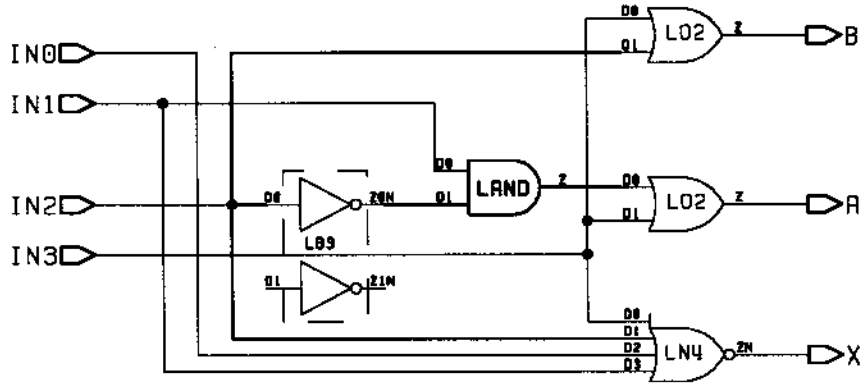
Boston University Electronics Design Facility			
DUMAND SBC DIGITIZER			
28-input priority encoder			
Dwg#	***-****	Rev:	A
Drawn By:	E. Hazen		
Sunday, December 9, 1990 6:17:18 pm (EST)			
//ginger/local_user/hazen/dumand/viteese/notes/pri28-sketch(sheet1) s1			

Block: CHAN # ENC. (Detail)



Boston University Electronics Design Facility	
DUMAND SBC DIGITIZER	
8-input priority encoder	
Dwg# ***-****	Rev: A
Drawn By: E. Hazen	
Sunday, December 9, 1990 4:30:47 pm (EST)	
//ginger/local_user/hazen/dumand/viteese/notes/pri8-sketch(sheet1) $L	

Block: CHAN # ENC. (Detail)



Boston University Electronics Design Facility	
DUMAND SBC DIGITIZER	
4-input priority encoder	
Dwg# ***-****	Rev: A
Drawn By: E. Hazen	
Sunday, December 9, 1990 6:08:39 pm (EST)	
//ginger/local_user/hazen/dumand/vitesse/notes/pri4-sketch(sheet1) $1	

Appendix C

ASIC Vendor Quotations

National Semiconductor

20 Blanchard Road
Suite 1
Burlington, Massachusetts 01803

Telephone: (617) 221-4500
Fax: (617) 272-6357

January 7, 1991

Mr. Eric Hazen
Boston University
590 Commonwealth Avenue
Boston, MA 02215

Re: DUMAND Project - SBC Fast Digitizer

Dear Eric,

Based on our conversations today and last December 19, National Semiconductor is pleased to provide the following quotation for your project, assuming that the entire design will fit into 1 Gate Array. National has not completed it's gate estimation, however based on a preliminary review, and Boston Universities inputs, it is anticipated that the design will occupy approximately 40 - 45k gates. National has proposed two gate arrays, the NGA049T, which contains 49,000 equivalent gates, features 256 ECL I/O's, and is packaged in a 323 CPGA, and the NGA052T which contains 52,000 equivalent gates, features 220 I/O's with mixed ECL/TTL interface capability, and is packaged in a 303 CPGA. It should be noted that National has only taken test data with the 323 CPGA at speeds over 1GHz, and additional testing would be required on the 303 CPGA package to determine if these speeds are possible. The pricing for these arrays is as follows:

Device	Package	NRE (Joint)	NRE (Turnkey)	50-100	100-500	500-1k	1k-5k
NGA049T	323 CPGA	$225K	$299K	$1499	$1428	$1295	$1234
NGA052T	303 CPGA	$225K	$299K	$1459	$1390	$1260	$1200

Note: NRE includes 10 Prototypes.
Joint NRE assumes BU supplies simulated NSC netlist.
Turnkey NRE assumes BU supplies generic schematics and test vectors.

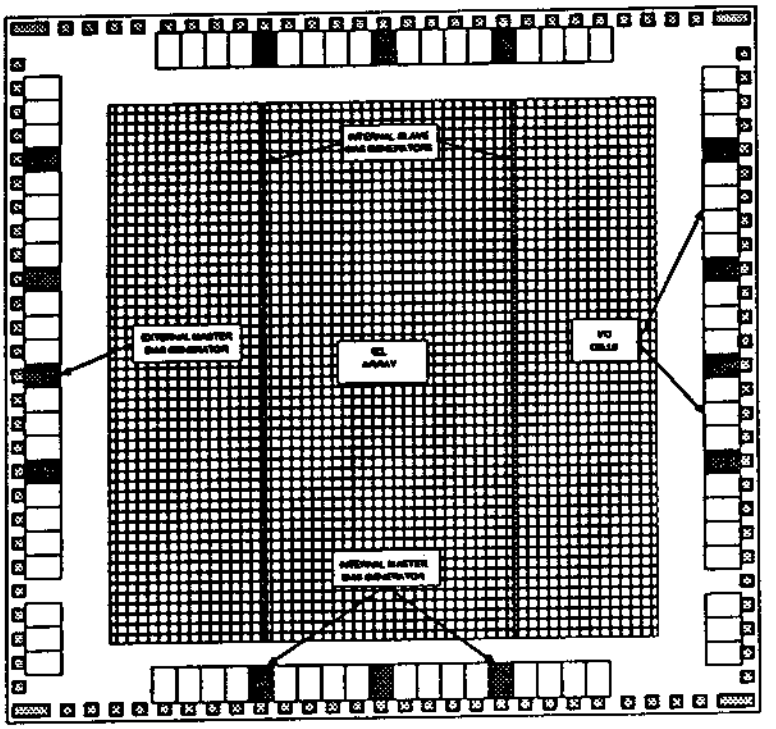
Design Automation support for the NGA series gate arrays currently is available with NSC's DA4 design automation system only. DA4 features either Cadence or Viewlogic schematic capture, with Verilog simulation. DA4 also provides several additional tools such as the NSC Electrical Design Rule Checker, and static timing analysis using CPA. DA4 currently is available on the SUN 4 platform, running 4.0.3 O.S. The cost for the Cadence or Viewlogic Schematic Capture, Verilog simulation, and DA4 specific tool packages is estimated to be $60k for your application. Yearly maintainence is also avaialable for 15% of the purchase price. DA4 may also be leased for $7k/month.

Please note that National has not completed the evaluation of a multichip solution to your project needs, and anticipates completeing this by Jan 11. Until then, if you have any other questions, please do not hesitate to contact me.

Regards,

Bill Carrigan
National Semiconductor
Boston ASIC Design Center

NGA SERIES - ECL Gate Arrays



PRODUCT FEATURES

5 REQ. WATTS/CAN 100 200

Description	NGA0500	NGA0900	NGA1600	NGA4800	NGA049T
Equivalent Gates	500	945	1610	4800	48700
# of Metal Layers	4	4	3	3	3
Typical Gate Delay (Note 1) Internal ECL (ps)	100-250	100-250	100-250	100-250	100-250
Speed/Power Option	YES	YES	YES	YES	YES
Typical Power (mW)	0.3-0.6	0.5-1.0	0.8-2.0	2.0-4.0	15-20
I/O (Note 2)					
ECL I/O	0	0	0	0	256
ECL/TTL I/O	13	25	48	72	0
Power/GND	3	3	12	40	56
Packages	16LDCC	16/24LDCC	44LDCC 75PGA	116LDCC 75/109PGA	323PGA
Availability (Calendar)	2Q91	4Q90	2Q91	2Q91	4Q90

Note 1: FO=2, L=1mm
Note 2: ECL I/O (100K/10K/10KH)

DATE: OCTOBER 1990

PRELIMINARY DATA SHEET

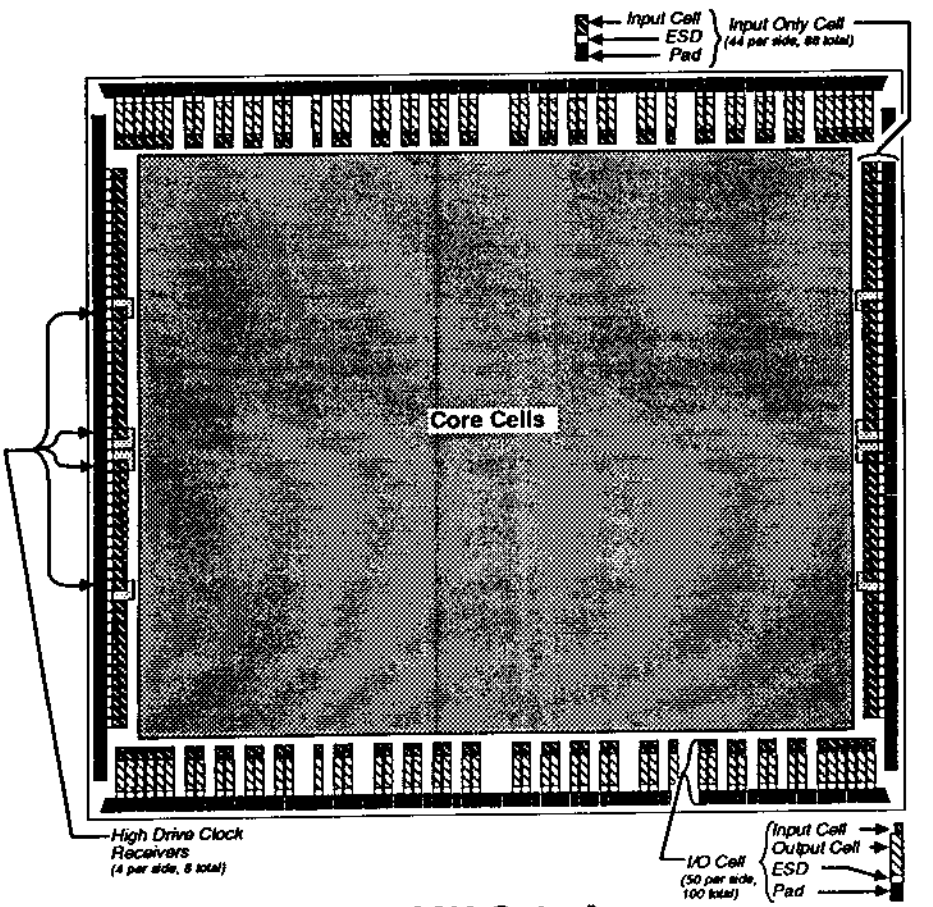
VITESSE SEMICONDUCTOR CORPORATION

VGFX100K/VGFX200K High Performance FX Series Gate Arrays

Features

- Superior Performance: High Speed and Low Power Dissipation
- Channelless Array Architecture for Ultra High Density
- Four Layer Metal for High Gate Utilization
- Proven GaAs Enhancement/Depletion MESFET Process
- Array Performance
  - D Flip-flop toggle rates: >1.6 GHz
  - Typical gate delay: 115 ps @ 0.15 mW (Unbuffered 2-input NOR, F.O. = 1, 0.21 mm wire)
  - Typical gate delay: 130 ps @ 0.6 mW (Buffered 2-input NOR, F.O. = 3, 0.63 mm wire)
  - ECL and GaAs inputs/outputs
  - TTL compatible inputs/outputs
- Choice of Sizes:
  - FX100K, 102K 2-Input NOR gates (raw), over 50,000 usable gates or 6,250 usable D flip-flops, 196 I/O
  - FX200K, 195K 2-Input NOR gates (raw), over 100,000 usable gates or 12,500 usable D flip flops, 256 I/O
- Multiple Buffering Options for Each Macro Function
- Embedded SRAM and Megacell Options Available
- Schematic Capture and Simulation Supported on MENTOR or VALID Platforms
- Behavioral and Mixed Mode Simulation Support for VERILOG XL
- Logic Synthesis Supported with Synopsys Design Compiler™

Architecture



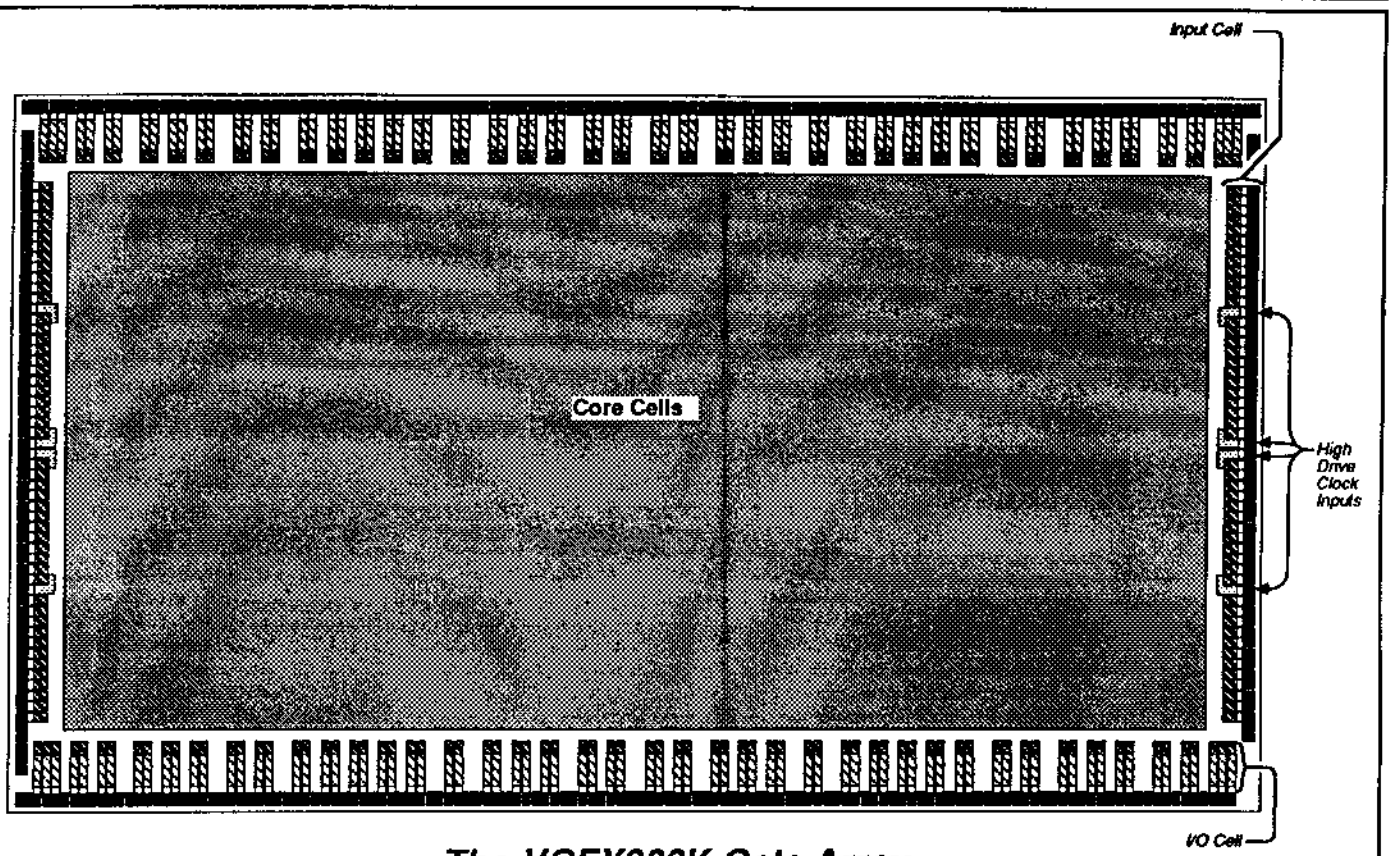
The VGFX100K Gate Array

741 Calle Plano, Camarillo, CA 93012 • (805) 388-3700 • FAX (805) 987-5896

VGFX100K/VGFX200K

High Performance FX Series Gate Arrays

VITESSE SEMICONDUCTOR CORPORATION



The VGFX200K Gate Array

Introduction

The FX Series offers the integration level of BiCMOS gate arrays at the speed performance of much smaller ECL devices. Implemented using Vitesse's proprietary H-GaAs process, the FX100K and FX200K are the first in a series of gate arrays that combine ultra high integration with leading edge performance.

The FX array family incorporates a channelless array architecture which allows metal routing on the first layer to be placed directly over unused cells. This approach avoids the need for pre-defined channels between columns of macros and therefore allows much greater density and flexibility than channelled gate array architectures. Due to an advanced four layer metal process, typical maximum array utilizations range from 50% to 70% of the total available gates. This yields over 50,000 and 100,000 utilizable gates (2-input NOR gates) for the FX100K and FX200K, respectively.

Capable of operating from 50 MHz to well over 500 MHz, the FX Series arrays have been designed to provide the best speed - power performance of any gate array technology. The speed of leading edge ECL technology is achieved at a fraction of ECL's power. In addition, because of the frequency independent power consumption of H-GaAs technology, power dissipation levels comparable to, or lower than, similar density BiCMOS arrays are a reality at frequencies above 50 MHz to 80 MHz. This power savings can add up to substantial cost savings to users in terms of overall cooling requirements.

As with all of Vitesse's ASIC products, the FX arrays interface with TTL, ECL and GaAs devices directly. The FX100K and FX200K use standard power supplies and are supported on the ASIC industry's most popular CAE platforms for schematic capture, behavioral modeling and logic synthesis. Vitesse also supports the custom implementation of embedded SRAM, multiport register files, and other megacell functions in the FX arrays.

VITESSE
SEMICONDUCTOR CORPORATION

VGFX100K/VGFX200K
High Performance
FX Series Gate Arrays

Technology

The FX Series arrays are implemented using Vitesse's proprietary H-GaAs III process. This process represents the third generation of the H-GaAs technology developed by Vitesse to manufacture high yielding, LSI and VLSI digital GaAs circuits. The H-GaAs III process features a 0.6 µm self-aligned gate MESFET and four levels of metal interconnect. The basic logic structure for the FX Series is a 2-input NOR gate implemented using direct coupled FET logic (DCFL). Millions of hours of life testing have proven the reliability of the H-GaAs process technology and the DCFL logic structure.

Applications

The FX Series of gate arrays can be used in a wide variety of applications including: mainframe computers, workstations and communications equipment. This family of high performance semi-custom products is ideally suited for systems requiring very high speed, low power digital logic at high levels of integration.

Computers

The ultra high integration that the FX arrays offer, combined with their high performance and low power consumption, makes them ideally suited for the implementation of high performance processors and processor support logic. Offering a big performance increase over BiCMOS technology and substantially lower power than ECL technology, the FX Series gate arrays are the perfect choice for systems with clock rates in excess of 50 MHz. Specific computer applications for FX arrays include integer arithmetic processing, floating-point processing, cache control, and bus interface functions.

Communications

Intelligent fiber optic communication links for voice and data transmission can be designed with the FX family. These applications can greatly benefit from the low power dissipation inherent in the FX arrays while allowing the user to implement the high speed VLSI and LSI circuits necessary to handle the new generation of high-bandwidth telecommunications standards. The implementation of large switching networks on a single chip is just one example of these applications.

Architecture

The FX arrays contain four cell types: internal logic cells, input only cells, input/output (I/O) cells and clock receivers. The layout of the VGFX100K is shown on page 1. Page 2 displays the layout of the VGFX200K. The table below is a summary of the internal cells, I/O and package options for both arrays in the FX family.

Internal Logic Cells

The internal logic cells comprise most of the area of the array. These cells use direct coupled FET logic (DCFL), which minimizes the number of elements needed for each logic function. The primitive element or building block is a cell which consists of a single depletion-mode transistor and two enhancement-mode transistors which can be connected to make a 2-input NOR gate.

Input Only Cells

Input only cells are located on two sides of the periphery of the array. Input cells are also located in Input/Output cells. Input cells can be personalized as latches, registers, or buffers, and are compatible with TTL, ECL or 'native' GaAs signals. All three signal levels can be used in one chip design to optimize overall system performance. Input cells can provide 1x

***Table 1:** Array Cell Summary*

Array Name	# of Internal Gates		# of Input Cells			# of I/O Cells		Total Signal Pins	Package Options
	Total Raw Cells	2-in* NOR / D F-F*	TTL	ECL GaAs	Hi-Drive	TTL	ECL GaAs		
VGFX100K	102K	51K / 6K	88	88	8	100	100	196	211 pin PGA** 256 pin LDCC
VGFX200K	195K	98K / 12K	92	92	8	156	156	256	344 pin LDCC

** based on 50% utilization ** 172 total signal pins supported in this package*

or 2x drive on either the true or complement signal. The input cells translate off-chip logic levels to internal GaAs logic levels for efficient internal operation. These cells also provide ESD input protection.

Each input only cell has enough resources, and can be personalized through macro selection, to form a JTAG-compatible boundary scan flip-flop. In this way boundary scan can be accomodated without using core cells.

A number of input cells in each array are configured as high-drive receivers intended for use as clock buffers. These special input cells can support up to 6x the drive capability of a standard input cell.

Input/Output (I/O) Cells

Input/Output cells are located on the top and bottom of the array. I/O cells can be configured as output drivers, input receivers, or bidirectional transceivers. TTL, ECL, and GaAs I/O signal levels are supported with no restrictions on mixing different I/O types. The output portion of the I/O cell can be configured as a latch, flip-flop, 2-input or 3-input OR or NOR, or as an inverting or non-inverting buffer. In addition, boundary scan can be easily accomodated since each I/O cell can be configured as a scan flip-flop. When configured as an ECL driver, the output cell can interface with ECL 10KH or 100K receivers while driving a 50Ω load. Two output cells may be paralleled to drive a double-terminated ECL bus (25Ω DC load).

Macro Library

The FX Macro Library contains information to fully evaluate the function and performance of logic blocks (macrocells). The FX library includes functional equivalents for all FURY Series macros as well as optimized megacell functions. The following is a representative list of the macrocells which are available for the FX arrays. Performance characteristics for selected macros are given on page 4. For a complete set of specifications, refer to the FX Design Guide.

- BIE - Bidirectional ECL input/output buffer
- CLK1 - Clock buffer
- CLK1G - Clock buffer with GaAs input
- IED1FF - Differential ECL Input
- IE1T - ECL input buffer (1x drive)
- IECK3 - ECL input buffer (3x drive)
- IG - Buffered GaAs input
- LA1 - Half adder
- LA1U - Half adder, unbuffered
- LA2 - Full adder
- LAND - 2-input AND
- LANDU - 2-input AND, unbuffered
- LB1UG - Unbuffered GaAs input
- LB3UG - Unbuffered inverting GaAs input
- LDR1 - Line driver/Inverting clock buffer, 1x drive
- LDR3 - Line driver/Inverting clock buffer, 3x drive
- LFP1 - Positive edge triggered D flip-flop
- LFP3 - Positive edge triggered D flip-flop with asynchronous set & clear
- LFP4 - Positive edge triggered D flip-flop with 3-input OR and asynchronous set
- LFP5 - Positive edge triggered D flip-flop with 4-input OR
- LLP1 - High transparent D latch
- LLP2 - High transparent D latch with 2-input OR
- LLP3 - Muxed positive transparent D latch
- LM1 - 2:1 multiplexer
- LM1U - 2:1 multiplexer, unbuffered
- LM3 - 4:1 multiplexer
- LN2 - 2-input NOR
- LN2B - 2-input NOR with 2x buffer
- LN2U - Dual 2-input NOR, unbuffered
- LN4 - 4-input NOR
- LN4U - 4-input NOR, unbuffered
- LN9 - 9-input NOR
- LN9U - 9-input NOR, unbuffered
- LNA2 - 2-input NAND
- LNA2U - 2-input NAND, unbuffered
- LO2 - 2-input OR
- LO4 - 4-input OR
- LSP1 - Positive edge triggered D flip-flop with 2:1 mux input
- LX1 - 2-input exclusive OR
- LX2 - 2-input exclusive NOR
- OE - ECL output buffer
- OE25 - ECL 25Ω cut-off output driver
- OG - GaAs output buffer
- PD - Pull-down

VITESSE SEMICONDUCTOR CORPORATION

VGFX100K/VGFX200K

High Performance FX Series Gate Arrays

Absolute Maximum Ratings (1)

Power Supply Voltage (ECL), V_{TT} potential to GND .....-2.5V to +0.5V
Power Supply Voltage (TTL), V_{TTL} potential to GND .....+4.3V to -0.5V
ECL Input Voltage Applied, ($V_{IN\ ECL}$) .....+0.5V to V_{TT}
TTL Input Voltage Applied, ($V_{IN\ TTL}$) .....-0.5V to V_{TTL}
ECL or TTL Output Current, I_{OUT}, (DC, output HI) .....50 mA
Maximum Junction Temperature, (T_J) .....150°C
Case Temperature Under Bias, (T_C) (2) .....-55° to +125°C
Storage Temperature, (T_{STG} (2)) .....-65°C to +150°C

Recommended Operating Conditions

ECL Supply Voltage, (V_{TT}) .....-2.0V ± 5%
TTL Supply Voltage, (V_{TTL}) .....+3.3V ± 5%
Commercial Operating Temperature Range, (T) (2). .....0° to 70°C
Industrial Operating Temperature Range, (T) (2). .....-40° to 85°C

Notes:
(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) Lower limit is ambient temperature and upper limit is case temperature.

DC Characteristics

TTL Inputs/Outputs: *(Over recommended commercial operating conditions, TTLGND = GND)*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	—	—	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage		—	0.5	V	I_{OL} = 16 mA
V_{IH}	Input HIGH voltage	2.0	—	—	V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage		—	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	50	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current	-500	—	—	µA	V_{IN} = 0.5 V
I_{OZH}	3-state output OFF current HIGH	—	—	100	µA	V_{OUT} = 2.4 V
I_{OZL}	3-state output OFF current LOW	-100	—	—	µA	V_{OUT} = 0.5 V
I_{OCZ}	Open collector output leakage current	—	—	100	µA	V_{OUT} = 2.4 V

ECL Inputs/Outputs: *(Over recommended commercial operating conditions with internal V_{REF}. $V_{CC} = V_{CCA}$ = GND, Output load 50Ω to V_{TT})*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-850	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH voltage	-1100	—	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1540	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	200	µA	$V_{IN} = V_{IH}$ max
I_{IL}	Input LOW current	-50	—	—	µA	$V_{IN} = V_{IL}$ min

Note: 1) Differential ECL output pins must be terminated identically.

GaAs Inputs/Outputs: *(Over recommended commercial operating conditions, $V_{CC} = V_{CCA}$ = GND, Output load 50Ω to V_{TT})*

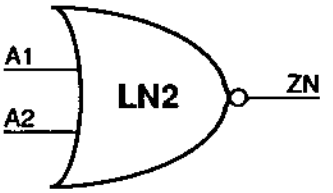
Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	V_{TT}+700	—	V_{TT}+1100	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	—	V_{TT}+100	mV	
V_{IH}	Input HIGH voltage	V_{TT}+600	—	V_{TT}+1200	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	V_{TT}-400	—	V_{TT}+200	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	200	µA	$V_{IN} = V_{IH}$ max
I_{IL}	Input LOW current	-100	—	—	µA	$V_{IN} = V_{IL}$ min

Note: 1) Differential GaAs output pins must be terminated identically.
2) If only GaAs I/Os are used, V_{TT} = 0V, V_{CC} = +2.0V, and all I/O levels are still referenced to V_{TT}.

Selected Macrocell AC Performance (Commercial temp. arrays)

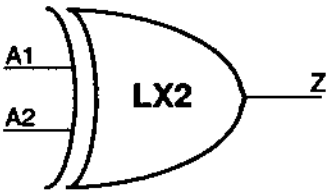
LN2: Buffered 2-input NOR

Parameter		Min	Typ	Max	Units
Propagation Delay					
A1, A2 to ZN	*Rising Signal*	50	—	80	ps
	Falling Signal	40	—	50	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	5	—	8	ps
	Falling Signal	7	—	8	ps
Delay/mm wire	*Rising Signal*	92	—	150	ps
	Falling Signal	76	—	95	ps
Power Dissipation		—	0.50	0.79	mW



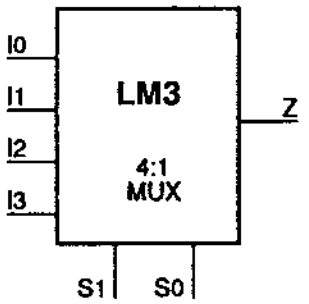
LX2: 2-Input XNOR

Parameter		Min	Typ	Max	Units
Propagation Delay					
A1, A2 to Z	*Rising Signal*	120	—	320	ps
	Falling Signal	150	—	290	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	5	—	8	ps
	Falling Signal	9	—	11	ps
Delay/mm wire	*Rising Signal*	92	—	150	ps
	Falling Signal	97	—	121	ps
Power Dissipation		—	0.99	1.53	mW



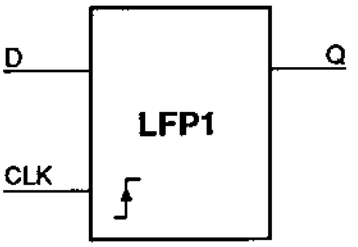
LM3: 4:1 Multiplexer

Parameter		Min	Typ	Max	Units
Propagation Delay					
S0, S1 to Z	*Rising Signal*	170	—	350	ps
	Falling Signal	170	—	320	ps
I0 - I3 to Z	*Rising Signal*	170	—	210	ps
	Falling Signal	170	—	260	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	6	—	9	ps
	Falling Signal	9	—	11	ps
Delay/mm wire	*Rising Signal*	103	—	167	ps
	Falling Signal	97	—	121	ps
Power Dissipation		—	1.40	2.28	mW



LFP1: Positive Edge Triggered D Flip-flop

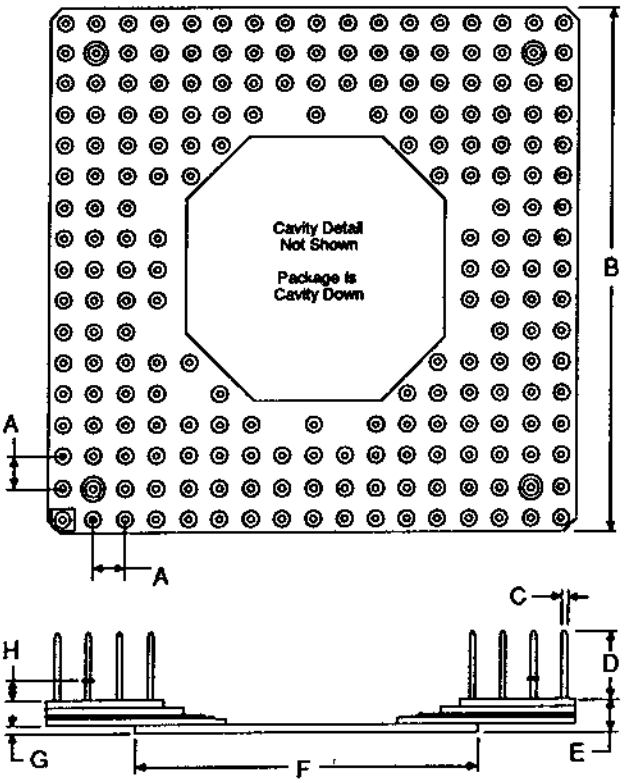
Parameter		Min	Typ	Max	Units
Propagation Delay					
CLK to Q	*Rising Signal*	110	—	180	ps
	Falling Signal	240	—	300	ps
t_{SET-UP}		61	—	102	ps
t_{HOLD}		43	—	73	ps
Toggle freq. (based on min. pulse width)		1620	—	2710	MHz
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	5	—	8	ps
	Falling Signal	8	—	10	ps
Delay/mm wire	*Rising Signal*	92	—	150	ps
	Falling Signal	92	—	115	ps
Power Dissipation		—	1.76	2.77	mW



VITESSE SEMICONDUCTOR CORPORATION

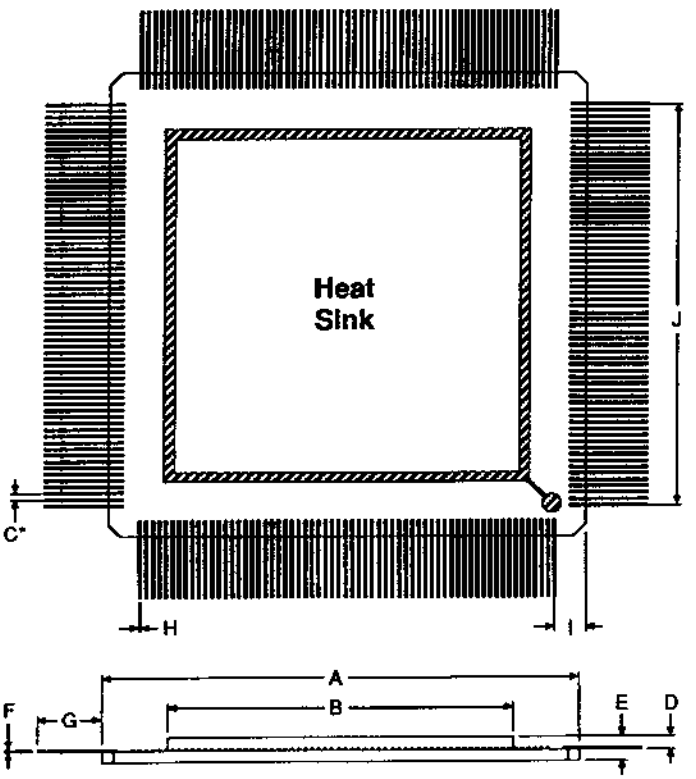
VGFX100K/VGFX200K
High Performance
FX Series Gate Arrays

211 Pin Grid Array (PGA)



Item	mm (Min/Max)	In (Min/Max)
A	2.41/2.67 (typ)	0.095/0.105 (typ)
B	41.91/44.45 (sq)	1.650/1.750 (sq)
C	0.41/0.51 (typ)	0.016/0.020 (typ)
D	4.45/4.95 (typ)	0.175/0.195 (typ)
E	2.0/3.0	0.08/0.12
F	27.4 (sq) Ref	1.08 (sq) Ref
G	0.38/0.64	0.015/0.025
H	1.02/1.52 (typ)	0.040/0.060 (typ)

256 Pin Leaded Flatpack (LDCC)



Item	mm (Min/Max)	In (Min/Max)
A	34.29/39.37 (sq)	1.350/1.550 (sq)
B	Ref 28 (sq)	Ref 1.1 (sq)
C*	0.51 (typ)	0.020 (typ)
D	0.38/0.64	0.015/0.025
E	2.03/3.05	0.08/0.12
F	0.0889/0.2159 (typ)	0.0035/0.0085 (typ)
G	6.1/7.6 (typ)	0.20/0.30 (typ)
H	0.15/0.26 (typ)	0.006/0.010 (typ)
I	Ref 2.54 (typ)	Ref 0.100 (typ)
J	32.0 (typ)	1.26 (typ)

* At package body

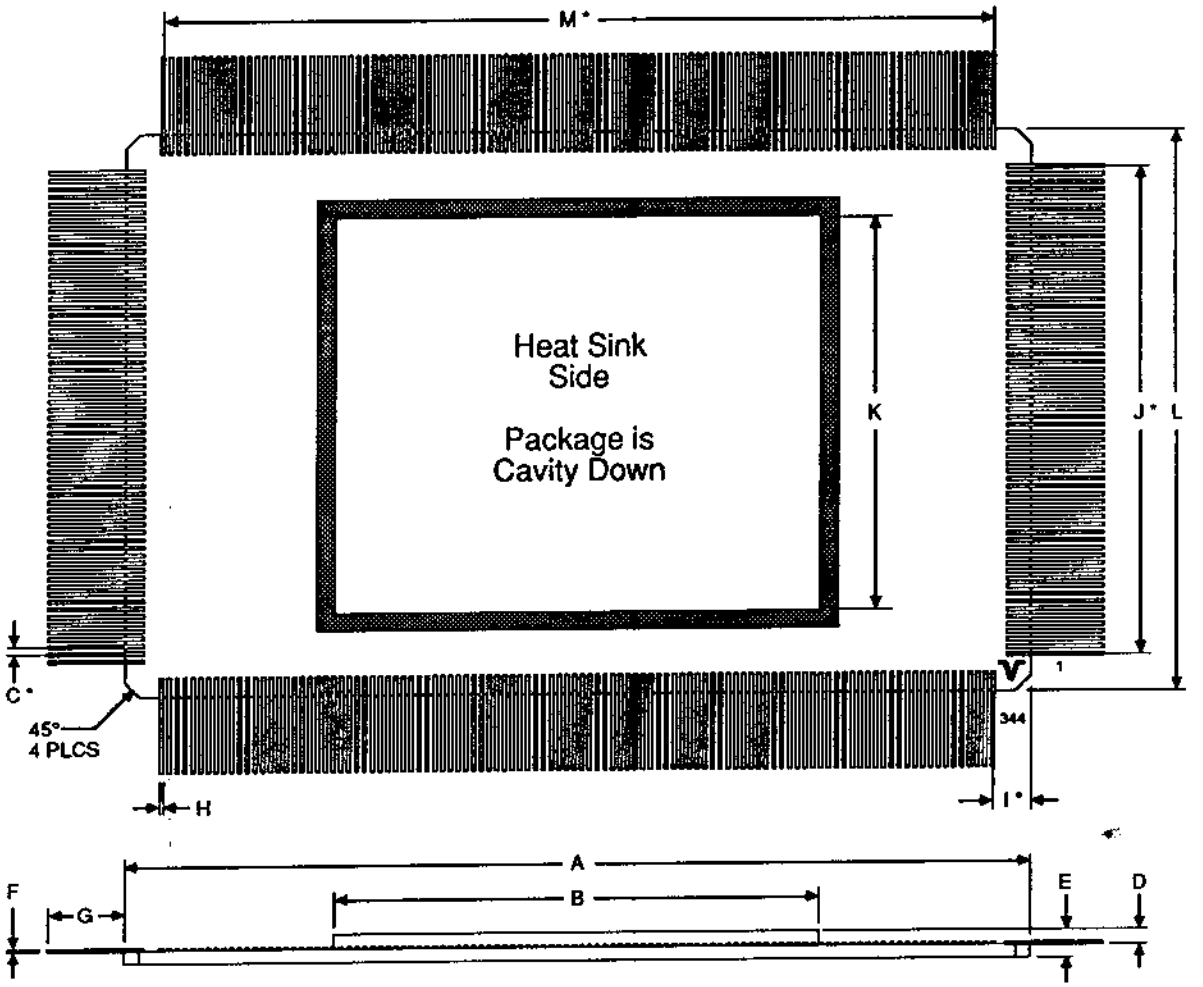
VGFX100K/VGFX200K

High Performance FX Series Gate Arrays

VITESSE SEMICONDUCTOR CORPORATION

Packaging

344 Leaded Ceramic Chip Carrier (LDCC)



Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	58.93/59.94	2.320/2.360	H	0.15/0.25	0.006/0.010
B	35.54 TYP	1.36 TYP	I*	REF 2.54 TYP	REF 0.100 TYP
C*	0.51 TYP	0.020 TYP	J*	32.00 TYP	1.26 TYP
D	0.38/0.63	0.015/0.025	K	39.46 TYP	1.16 TYP
E	2.16/2.92	0.085/0.115	L	36.57/37.59 SQ	1.440/1.480
F	0.09/0.216	0.004/0.008	M*	54.36 TYP	2.140 TYP
G	5.08/7.62	0.200/0.300			

* At package body

VITESSE SEMICONDUCTOR CORPORATION

Option Development Procedure

Vitesse Semiconductor offers its customers the option of fully designing their own gate array, or having Vitesse perform a turn-key implementation of their design based on mutually agreed specifications. Regardless of the interface, a Vitesse implementation engineer is assigned to the customer to answer questions and track the progress of the design from start to finish. The following steps are normally performed by a Vitesse implementation engineer.

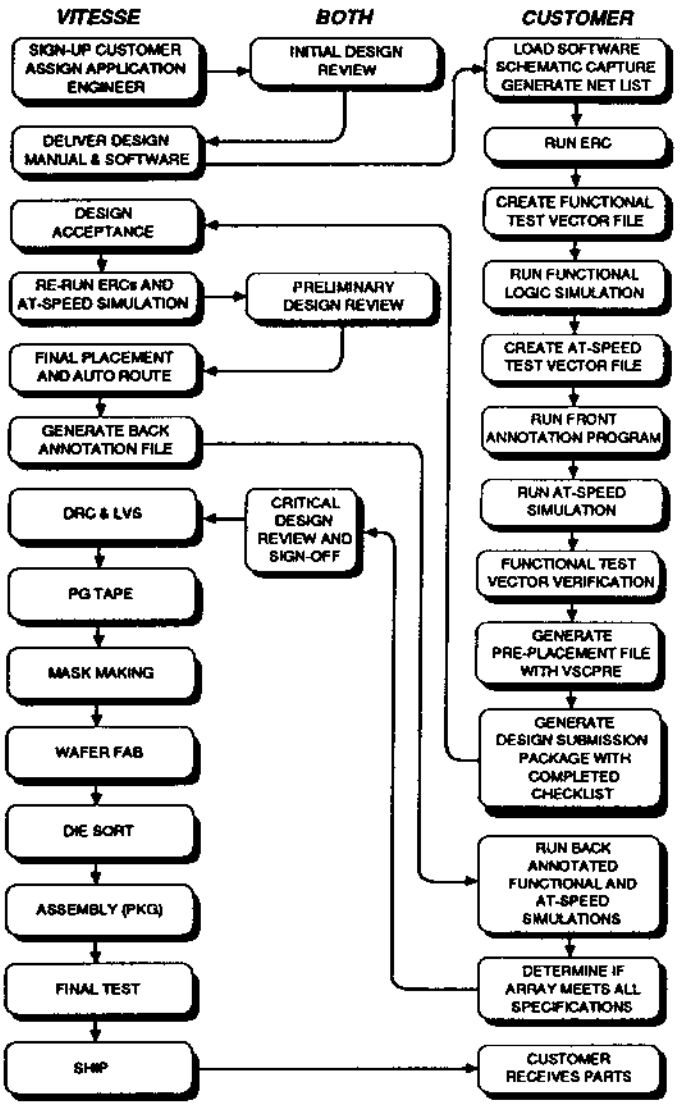
- *Final placement and routing of the design*
- *Net-length extraction*
- *Fan-out and metal delay calculation*
- *Design rule checking and layout vs schematic*

Through experience with many gate array designs, Vitesse has created a design automation framework and a well defined flow for smooth implementation of customer designs. The flowchart at right summarizes the typical gate array project flow and the various tasks delegated to the customer or to Vitesse.

CAD Tools/Support

FX designs are supported on MENTOR, VALID, SYNOPSYS, and VERILOG platforms. LASAR simulation software is used to verify the AC performance of the design by taking into account on-chip timing variations. Simulation libraries for VERILOG XL™ are also supported. The Vitesse Design Kit includes documentation and software which allow the customer to perform schematic capture, functional simulation, front-annotated timing simulation, electrical rule checks, and back-annotated simulation upon completion of placement and routing. To facilitate floorplanning and block pre-placement, Vitesse has an interactive graphical placement program that the customer may choose to use for their design. This program is supported in the X Windows™ environment. Cadence placement and routing tools are used for physical implementation.

Gate Array Design Flow



Training

Design classes are provided to help the customer understand the design methodology and tools utilized in the gate array design process. These classes are recommended for all customers planning to implement a design in a Vitesse gate array. Training can be provided at the Vitesse facility or at the customer's site.

VGFX100K/VGFX200K
High Performance
FX Series Gate Arrays

VITESSE SEMICONDUCTOR CORPORATION

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VITESSE

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Fax (805) 987-5896

12/3/90
Mr. Eric Hazen
Boston University
Department of Physics
590 Commonwealth Avenue
Boston, Massachusetts 02115

Dear Eric,

Attached please find a budgetary quotation for the VGFX100K High Performance Channelless Gate Array. We believe it is the optimum solution to your DUMAND SBC Fast Digitizer requirements. Please note that a firm fixed pricing quotation will be furnished upon final review of the gate level design requirements.

Additionally, I have included in this package a copy of the Preliminary Technical Analysis of the Digitizer block diagram you provided. Allow me to make a few comments regarding the TA:

1. It was authored by Steve Dias who can be reached at (617) 239-8075.
2. The gate count and power dissipation seem to be very close to earlier estimates and well within both your budgets and the performance of the VGFX100K.
3. The maximum speed estimates of the design are completely a function of the 211 PGA package limitations. Using techniques such as impedance matching and source termination, other Vitesse customers have been able to exceed these limits. Steve and the Vitesse experts on printed circuit board layout will be in touch with you to discuss these methods of performance enhancement.

Regarding the development of this ASIC device, please be aware that as of January 1, 1991, Vitesse will support Mentor designs running under version 7.0 of the IDEA Series Workstation. This week you will be receiving Vitesse Release 3.2 of the FURY Design Kit, which is version 7.0 compatible.

Finally, the other items I've included in this package include the VGFX100K Preliminary Data Sheet and the Quality Assurance and Reliability Report you requested. I hope this information proves useful in your consideration of Vitesse as a supplier in your program. We look forward to working with you.

Regards,

Tony McManus
District Sales Manager

12/3/90
Quotation No.: EBN/PG-1457
Boston University

VGFX100K High Performance FX Series Gate Array in a 211PGA ceramic package; 102K 2-input NOR equivalents (raw); approx 50K usable gates.

Non-Recurring Engineering (NRE), including:
- Mentor 7.0 Library and Utlities
- Implementation engineer assignment
- Netlist level interface
- Preliminary and Critical Design Reviews
- Mask generation
- Fabrication, Assembly and Test of five (5) prototypes.....$152,000

Production of the DUMAND SBC Digitizer ASIC

40 pieces.....$925 ea

Leadtimes

Design submission to prototype delivery.....12 weeks
Production delivery ARO.....12 weeks

VITESSE TECHNICAL ANALYSIS 30-Nov-90

CUSTOMER: Boston University
KEY CONTACT: Eric Hazen
PHONE: 617 353-4117
CIRCUIT: DUMAND SBC Digitizer

The following document contains a summary of the technical analysis done by Vitesse applications engineering. All estimates are based on specified worst-case performance unless otherwise indicated. Please contact Vitesse Applications if you have any questions.

ANALYSIS SUMMARY

Recommended Product: VGFX100K
Gate count: 41824
Total Power: 19.7 W

Critical Path Timing: Due primarily to package and clock distribution limitations the maximum operating frequency is limited to 578 Mhz.

Package: 211 PGA

	ECL	TTL	CMOS	GaAs
Inputs:	62	0	0	0
Outputs:	0	40	0	0

Required Supplies: 5V, -2V

Special Macros: No special macros are required.
Notes: The two FIFOs assume the implementation suggested by Eric Hazen as a shift register based design.

GATE COUNT AND POWER DISSIPATION SUMMARY

29-11-90

COMPANY: Boston University
CIRCUIT: DUMAND SBC Digitizer
NOTE: VGFX100K implementation

TOTAL CELLS: 41824 cells
TOTAL POWER: 19719.7 mW

Macro	Function	Count	Macro Cells	Macro Power	Total Cells	Total Power
	INPUTS					
IEDIF3	ECL diff in 3x	1	2	23.1	2	23.1
IEDIF2	ECL diff in 2x	27	2	8.8	54	237.6
IE1T	ECL input	6	1	5.61	6	33.66
	OUTPUTS					
OT	TTL output	40	1	16.39	40	655.6
	TIME STAMP					
LFP3	DFF set/rst	12	14	6.16	168	73.92
LX1	XOR2	12	8	3.85	96	46.2
LN4	NOR4	9	8	1.76	72	15.84
LN2	NOR2	3	4	1.76	12	5.28
	EDGE DETECTOR					
LFP3	DFF set/rst	54	14	6.16	756	332.64
LX1	XOR2	27	8	3.85	216	103.95
	CLOCK MUX					
LM1	2:1 mux	10	8	3.41	80	34.1
	WRITE CONTROL					
LN2	NOR2	50	4	1.76	200	88
	FIFO #1 39 X 5 WORDS					
LFP3	DFF set/rst	195	14	6.16	2730	1201.2
LAND	AND2	195	6	2.86	1170	557.7
	PIPELINE LATCHES					
LFP3	DFF set/rst	12	14	6.16	168	73.92

VITESSE Gate Count and Power Analysis

	CHANGE REGISTER					
LFP3	DFF set/rst	27	14	6.16	378	166.32
LFP3	DFF set/rst	5	14	6.16	70	30.8
LN4	NOR4	3	8	1.76	24	5.28
LX1	XOR2	4	8	3.85	32	15.4
LN2	NOR2	1	4	1.76	4	1.76
	MUX					
LM3	4:1 mux	9	14	5.06	126	45.54
LM1	2:1 mux	1	8	3.41	8	3.41
	FIFO #2 17 X 100 WORDS					
LFP3	DFF set/rst	1700	14	6.16	23800	10472
LAND	AND2	1700	6	2.86	10200	4862
LFP1	DFF	3	12	6.16	36	18.48
	HOT ROD INTERFACE					
LFP3	DFF set/rst	80	14	6.16	1120	492.8
LX1	XOR2	32	8	3.85	256	123.2

BUCLK 11/30/90 1:55:35 PM

FX	COM	NONE					
Macro	Path	Wire	Fan	Rise	Fall	Rise	Fall
IEDIF3	+-PAD->Z1+-	0.825	5.00,5.00	620	800	620	800
LDR3	+-A->ZN-+	0.825	5.00,5.00	170	140	970	760
Total						970	760

DUMAND TIME STAMP COUNTER

FX COM NONE

MACRO	PATH	WIRE	FAN	RISE	FALL	RISE	FALL
LFP3	++CP->Q+-	0.660	4.00,4.00	400	510	400	510
LN4B	+-D0->ZN-+	0.165	2.04,2.04	170	110	680	510
LX1	+-D0->Z-+	0.165	1.00,1.00	280	330	790	1010
SET UP						180	180
Total delay						970	1190

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SEMICONDUCTOR CORPORATION

QUALITY ASSURANCE AND RELIABILITY

QUALITY GOAL

- To achieve ≤ 100 DPM quality index on production parts

RELIABILITY GOAL

- To achieve ≤ 20 FITs at T_j = 100°C on all products

QUALITY PHILOSOPHY

- Quality must be built into the product
- Quality is customer satisfaction
- Quality is a team effort

QUALITY POLICY

Definition of Quality:	Customer satisfaction
System:	Prevention
Performance Standard:	Zero defects
Measurement:	Cost of quality

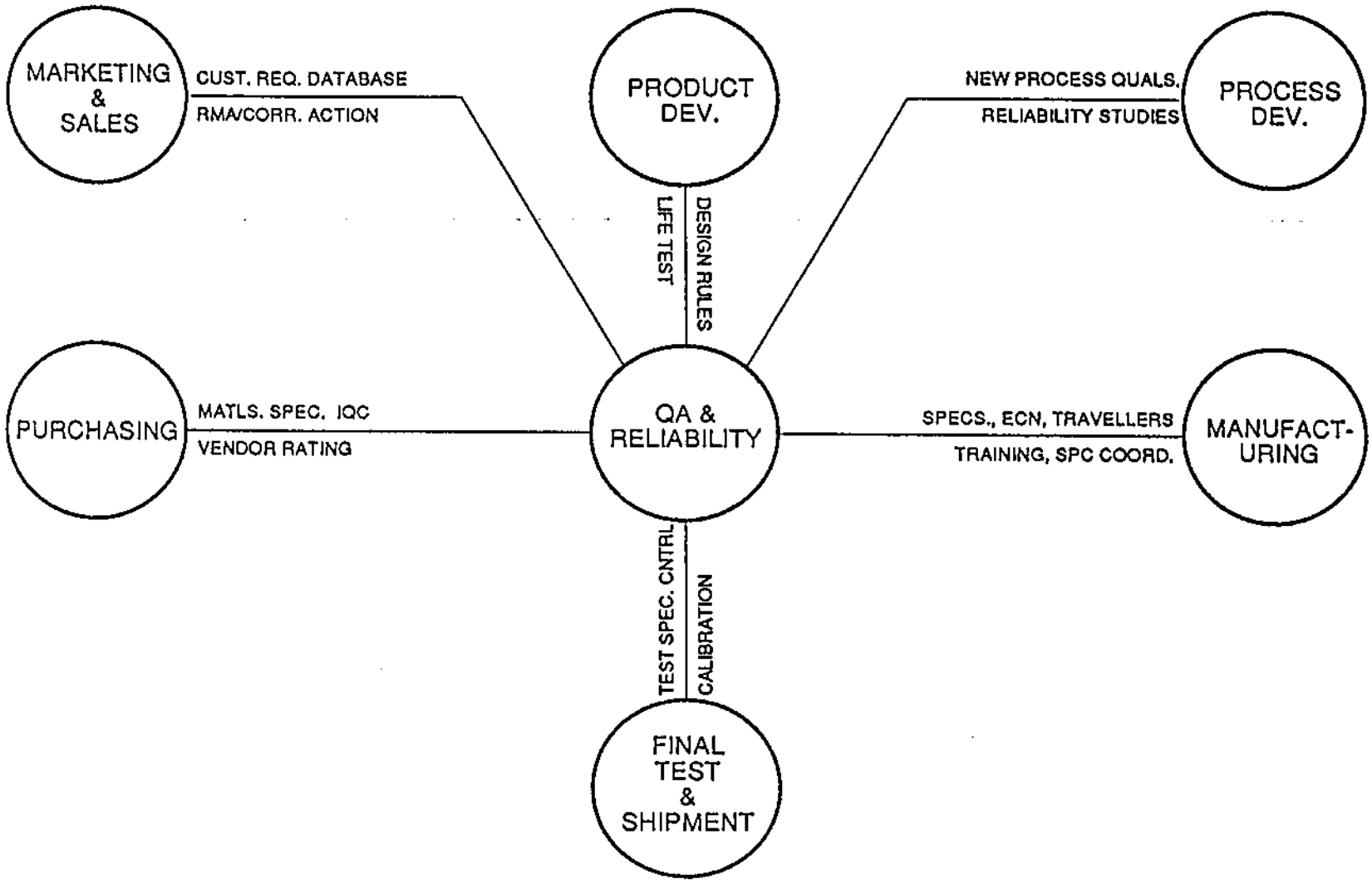
VITESSE

QUALITY SYSTEMS

- Overall system based on MIL-Q-9858A
- Inspection methods based on MIL-STD-883C
- Key Controls:
  - Environmental monitoring
  - Incoming material inspection
  - Document control (specs, ECN, travellers...)
  - SPC control of critical process steps
  - Calibration of equipment per MIL-STD-45662
  - Extensive PCM (process control monitor) testing
  - Full traceability (ingot to packaged part)

VITESSE

Vitesse Approach to TQC



VITESSE

RELIABILITY ADVANTAGES OF GaAs OVER SILICON

Characteristic	GaAs	Silicon	GaAs Advantage
Electric Field at peak electron velocity	7 kv/cm	30 kv/cm	- Lower power dissipation - Freedom from dielectric breakdown and field-induced electromigration
Energy Band Gap	1.4 ev	1.1 ev	- Potential high reliability - High temperature operation - Higher activation energy - Greater radiation tolerance
Device Structures	Schottky Barrier	MOS & Bipolar	- No known surface effects - Insensitive to ionic contamination - Stable at high temperature

VITESSE

RELIABILITY ADVANTAGES OF VITESSE PROCESS

	TRADITIONAL APPROACH	VITESSE APPROACH	VITESSE ADVANTAGE
Device Type	D-Mode and recessed E-Mode	Self-Aligned D- and E-Mode	- Greater repeatability
Gate Material	Au-Based (TiPtAu)	W-Based	- High temperature stability
n+ Alignment	Stepper Aligned	Self-Aligned	- Greater uniformity - Lower source resistance
Interconnect Material	Au-Based	Al-Based	- Proven VLSI interconnect - Silicon industry solutions
Interconnect Scheme	Lift off/Ion Mill or Airbridge	Etched	- Cleaner process - Proven equipment solutions

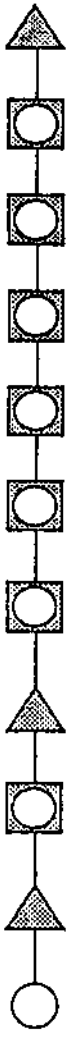
VITESSE

SILICON-LIKE FEATURES OF VITESSE PROCESS

- State-of-the-art silicon VLSI fab equipment
  - Precision implanters
  - 5x/10x DSW steppers
  - Metal sputtering systems
  - Plasma-enhanced CVD dielectric systems
  - Dry etchers
- N-MOS like process recipe
  - Implanted active layers
  - Sputtered metal films
  - Plasma-enhanced CVD low-stress dielectrics
  - All dry etch replication
  - Interconnects on field oxide

VITESSE

General Product Flow - Wafer Fabrication



INCOMING MATERIAL INSPECTION

CHANNEL INFORMATION

GATE METAL

CONTACTS

METALLIZATION / INTERCONNECTS

PASSIVATION

PARAMETRIC TEST

QC GATE - WAFER ACCEPTANCE

WAFER PROBE / SORT

QC MONITOR - WAFER PROBE

SHIP TO DIE BANK

KEY

- Production Process/ Test/Inspect Step
- QC Gates and Monitors
- Production Process

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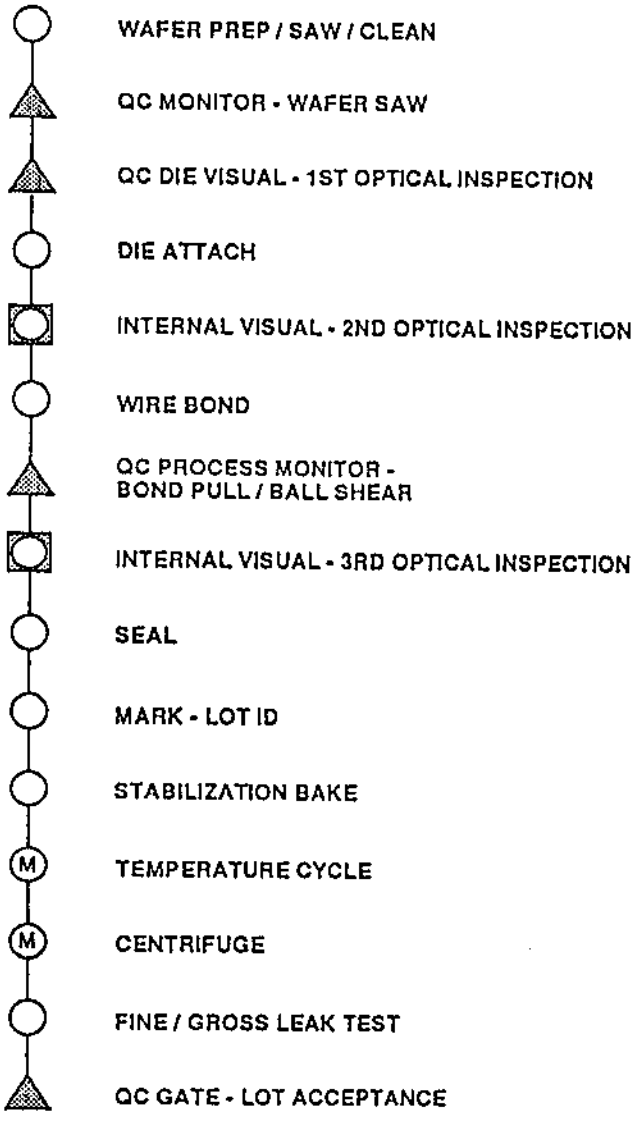
General Product Flow - Assembly

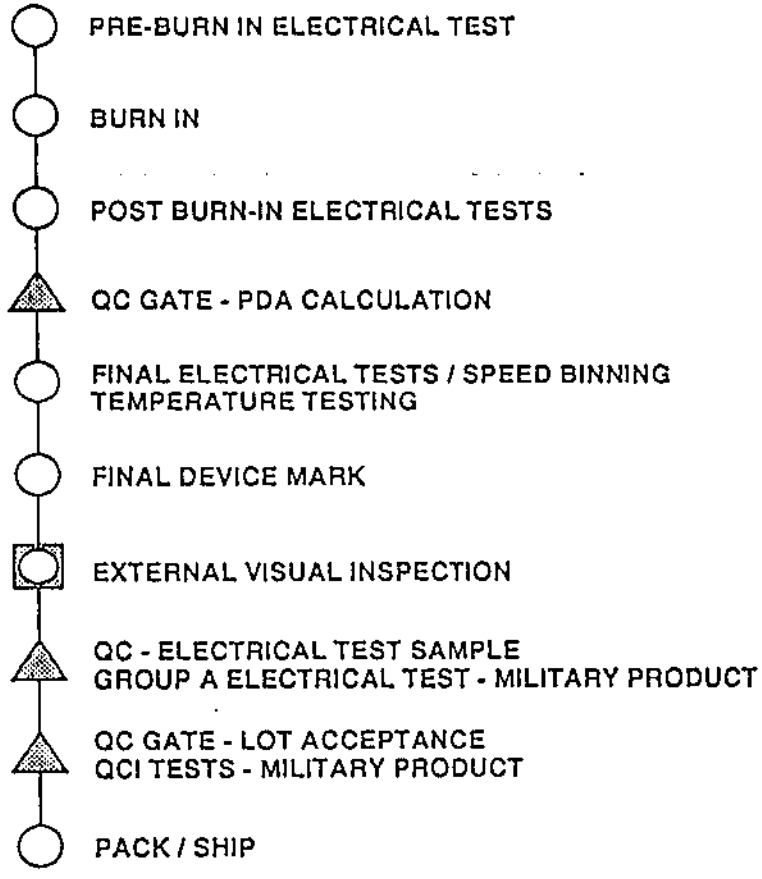


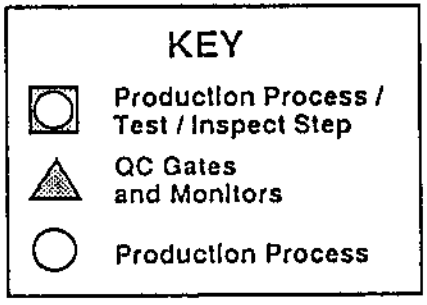
KEY

- Production Process/ Test/Inspect Step
- QC Gates and Monitors
- Production Process
- (M) Mil Flow Only

VITESSE

General Product Flow - Test





VITESSE

PACKAGE AND ASSEMBLY

- Gold-plated ceramic multilayer packages custom designed to insure high speed performance
- Silver glass die-attach
- Ultrasonic aluminum wedge bond
- Hermetic solder seal in nitrogen ambient
- Die visuals based on MIL-STD-883C, method 2010
- SPC charts for die shear and bond pull
- Gross and fine leak screening

VITESSE

Non-Hermetic MQUAD™ Package Option

Key Features:

- All Metal, 132 Lead, 25 mil Centers Construction
- Compatible with JEDEC PQFP Footprint, Socket and Carrier
- Built in Finned Heatsink, Handles up to 3 Watts with No Air Flow
- Epoxy Die Attach, 1.3 mil Gold Wire Thermosonic Ball Bond and B-Staged Epoxy Seal
- Meets Thermal Shock Per Mil-Std-883C, Method 1011, Cond. C
- Passes 1000 Hour Autoclave (121° C, 100% RH, 2 Atm) Test With Zero Failures

MQUAD is a Trademark of Olin Corporation

VITESSE

DC AND HIGH SPEED TEST

- 100% DC functional and parametric testing on Teradyne J953
- 40 MHz functional clock rate
- Timing edges 100 pS resolution, ± 250 pS accuracy
- Auto calibration under software control

VITESSE

RELIABILITY PROGRAM

- Four level reliability test strategy
  - Electromigration studies (200°C, high current density)
  - Process reliability test (250°C, storage test)
  - Package qualification (Thermal evaluation, 883C Group B & D screens)
  - Product life test (T_A = 125°C, ≥ 2000 hours)

VITESSE

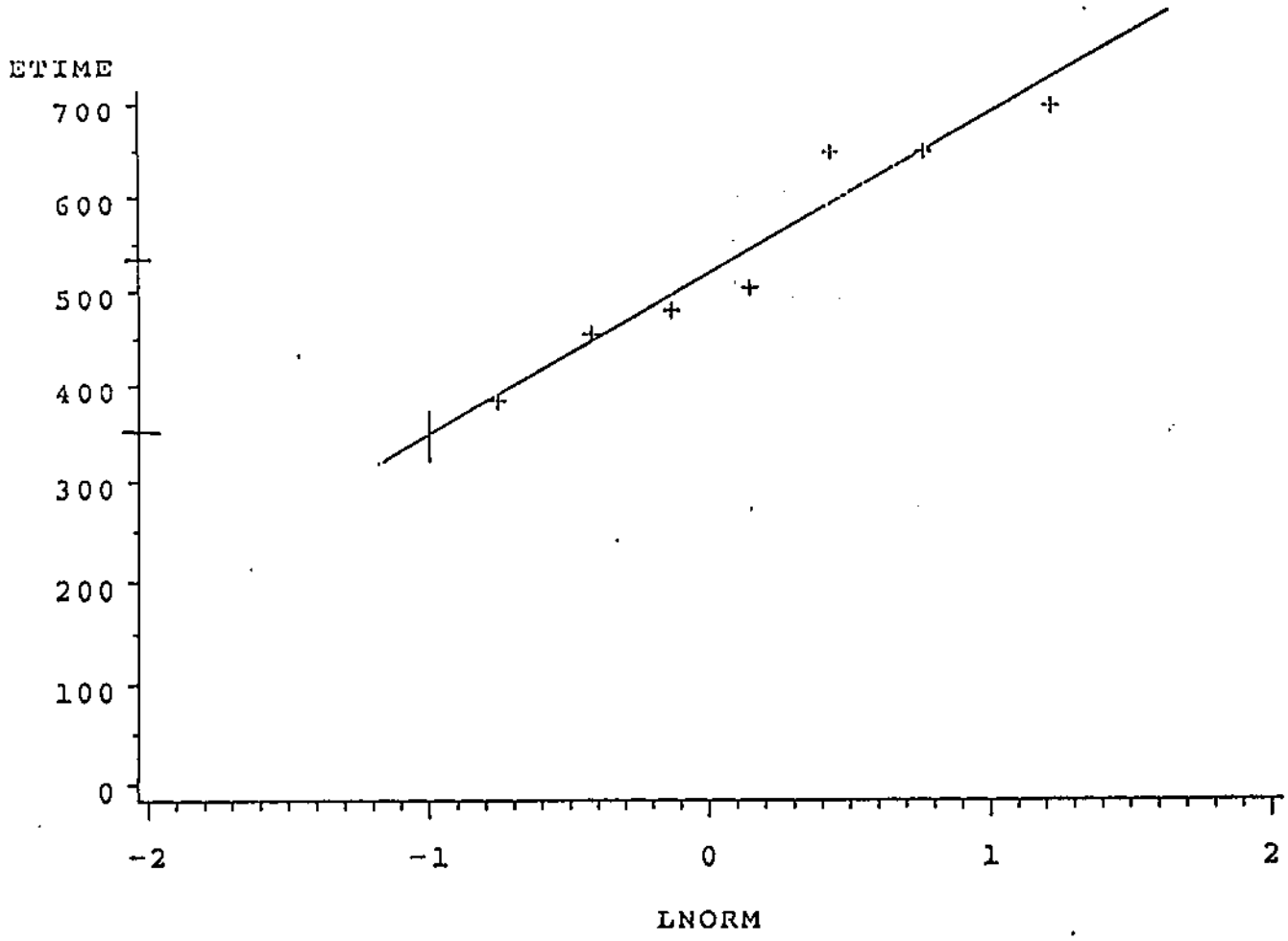
ELECTROMIGRATION TEST RESULTS

- Test conditions: 200°C, 1 x 10^6 A/cm^2
  EA = 0.6 ev (assumed)
- Failure criteria: 50% increase in resistance
- Sample size: 52,000 stripe hours
- Results: MTTF @ 100°C, 2 x 10^5 A/cm^2
  Metal 1: 0.47 Million hours
  Metal 2: 0.68 Million hours

VITESSE

EM FAILURE DISTRIBUTION

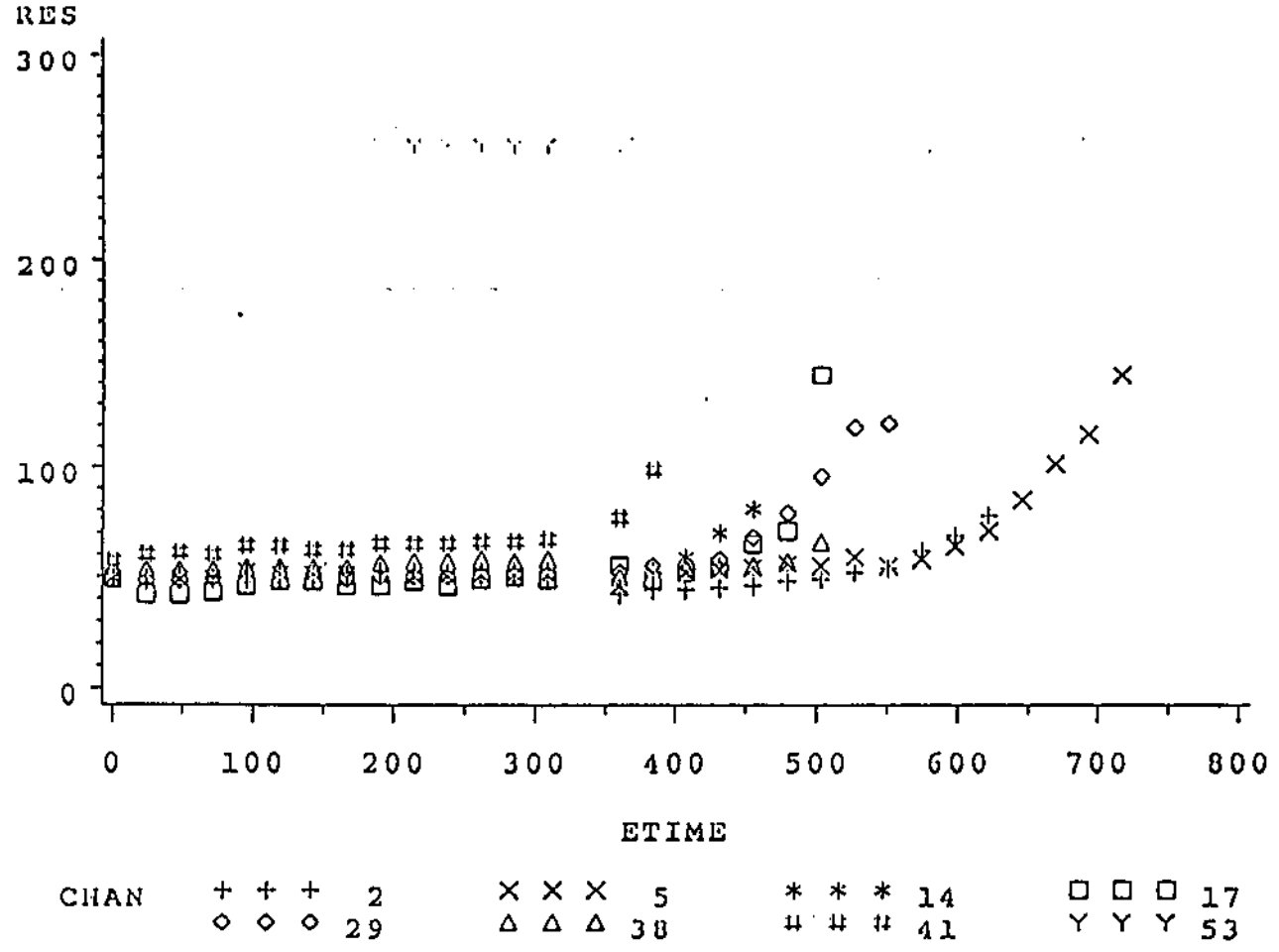
EMTEST .H
TYPE-m2expt IBIAS-1e6



VITESSE

RESISTANCE vs. TIME

emtest #25
TYPE-m2contro IBIAS-1e6



VITESSE

PROCESS RELIABILITY TEST DATA

- METHOD: 250°C storage bake in N_2 ambient at wafer level
- TEST VEHICLE: PCM FETs, Sheet resistance/Via/cross over structures
- TEST DURATION: 1000 hours
- SAMPLE SIZE: 21 wafers
- CUMULATIVE FET HOURS: 0.2 million
- CUMULATIVE STRUCTURE HOURS: 0.9 million
- RESULTS:
  - No catastrophic failures of FETs, Via strings,...
  - Parametric change in I_{DSS}, V_T, N^+ sheet ρ less than 10%
- CONCLUSION: Extremely stable schottky barriers

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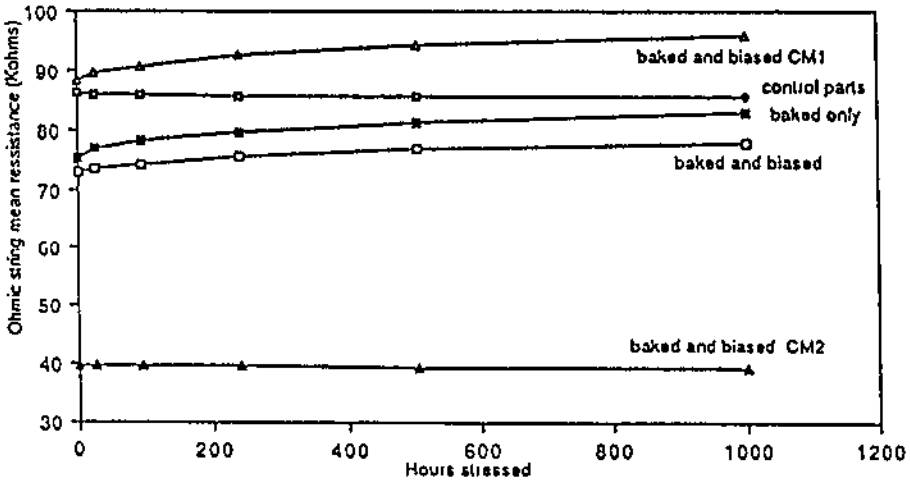
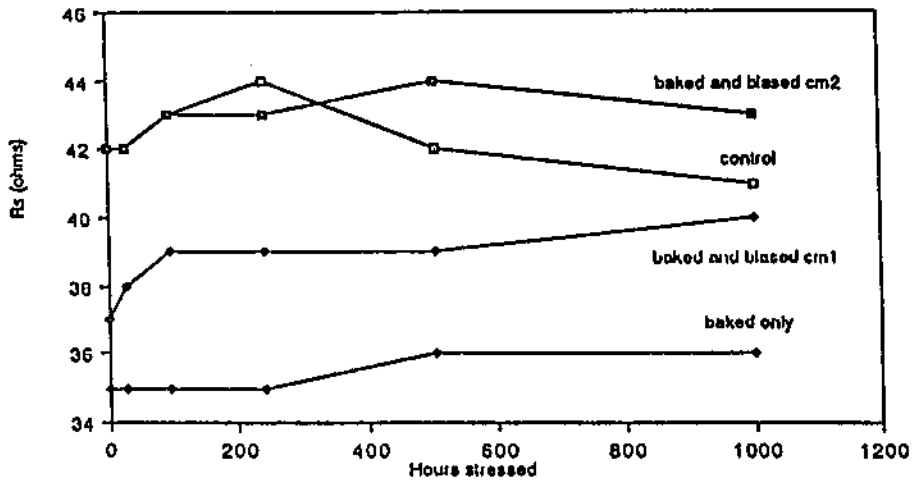
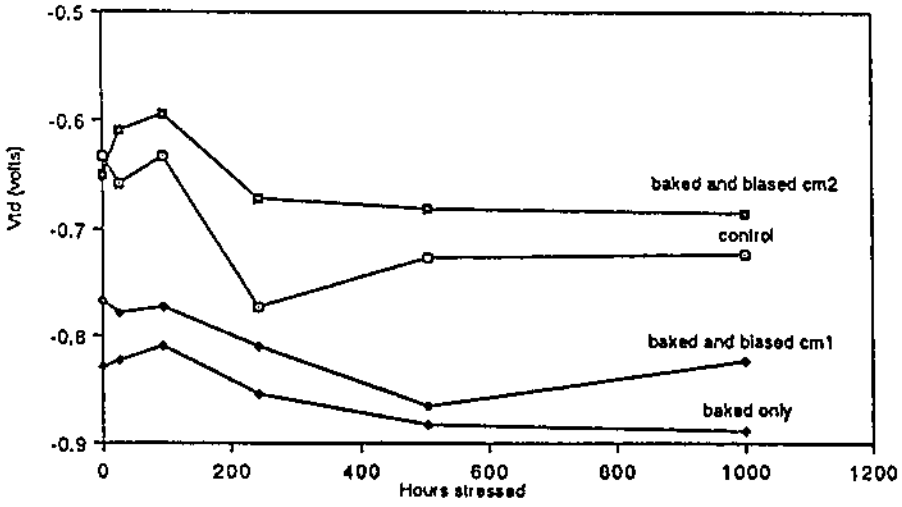
Ohmic string mean resistance vs stress time



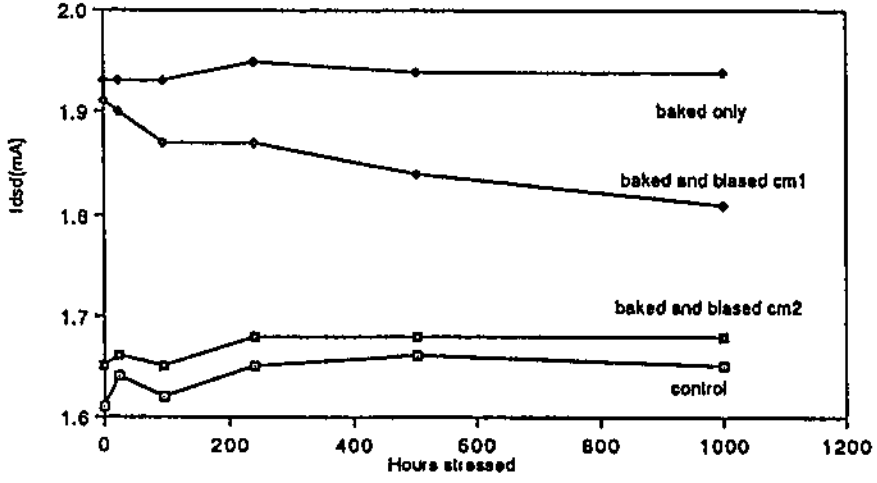
FET # 8 Rs vs stress time (packaged parts)



FET #16 Vt vs stress time (packaged parts)



FET #16 Ids vs stress time (packaged parts)



VITESSE

PACKAGE QUALIFICATION

MIL-STD-883C GROUP B & GROUP D GENERIC DATA

PRODUCT	PACKAGE	GROUP B		GROUP D	
		SAMPLES	REJECTS	SAMPLES	REJECTS
SPD 818	24DIP	83	0	124	1 *
SPD 818	28 LDCC	—	—	35	0
VSC1500	52LDCC	20	0	86	0
VSC4500	149 PGA	59	0	103	1 *

* *Fine leak rejects only. Lots met LTPD spec.*

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LIFE TEST APPROACH

- Static bias at nominal supply voltages
- Inputs returned to logic 'I' or 'O'
- TTL outputs terminated by 470 Ω to ground
- ECL/GaAs outputs terminated by 50 Ω to -2 Volts
- Ambient temperature set to 125°C
- Junction temperature evaluated from $\theta_{j\text{-}c}$ studies
- Failure criteria: Catastrophic/Spec. failures
- Interim test points: 168, 336, 504, 840, 1000 hours; thereafter every 500 hours

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LIFE TEST SUMMARY

PRODUCT	COMPLEXITY	PACKAGE	SAMPLE SIZE	LIFETEST HOURS T_A = 125 C	CUMULATIVE DEVICE HOURS
2900	< 500 gates	52 LDCC	293	1536	348,612
12G422T	1000 gates	22 DIP	45	1000	45,000
8001	1500 gates	52 LDCC	106	1000	106,000
4500	4500 gates	164 LDCC	40	1133	45,320
15K	15000 gates	211 PGA	60	1000	60,000
30K	30000 gates	344 LDCC	20	500	Continuing

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FAILURE RATE PREDICTION

FAMILY	SAMPLE SIZE	CUM. DEVICE HRS @ T_A = 125 C	REL REJECTS	FAILURE RATE (FITs) T_A = 70 C	T_A = 55 C
2900	293	348,612	1	29	6
422T	45	45,000	0	100	20
8001	106	106,000	1	92	18
4500	40	45,320	0	100	20
15000	60	60,000	0	75	15

NOTE: Failure rate is calculated for an upper confidence level of 60% using χ^2 distribution and activation energy of 1.2 ev.

VITESSE

MILITARY SCREENING PROGRAM

- Fab line not DESC certified, but meets most of the provisions of MIL-M-38510H
- Quality system based on MIL-Q-9858A
- Parts screened to MIL-STD-883C, Class-B level can be shipped against customer SCD or to Vitesse-certified non-Jan specifications
- In-House MIL screening facilities:
  - Burn-In/life test ovens
  - Fluoro carbon gross leak tester
  - Helium fine leak tester
  - Centrifuge
  - Die shear/bond pull

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PRODUCT SCREENING FLOWS

SCREEN	PROCEDURE PER METHOD 5004 OF MIL-STD-883C	COMMERCIAL / EXTENDED TEMP	MILITARY
VISUAL / MECHANICAL			
• Internal Visual	Method 2010	100%	100%
• Temperature Cycling	Method 1010, Cond C	—	100%
• Constant Acceleration	Method 2001, Cond B Y1 Orientation only	—	100%
• Hermeticity			
- Fine Leak	Method 1014	100%	100%
- Gross Leak	Method 1014	100%	100%
BURN-IN			
• Pre Burn-In Electrical	Per Applicable Device Specification	100%	100%
• Burn-In*	Method 1015, 125 C	100%	100%
• Post Burn-In Electrical	Per Applicable Device Specification	100%	100%
• Percent Defective Allowable (PDA)	Maximum PDA - 5%		

** Duration of burn-in for commercial products varies from 24 to 96 hours*

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PRODUCT SCREENING FLOWS (continued)

SCREEN	PROCEDURE PER METHOD 5004 OF MIL-STD-883C	COMMERCIAL / EXTENDED TEMP	MILITARY
FINAL ELECTRICAL TEST			
• Static, Dynamic, Switching and Functional Tests	Method 5004, Table 1, Per Applicable Device Specification	100%	100%
QUALITY CONFORMANCE			
• Group A	Method 5005	—	Sample
• Group B	(See Appropriate Tables	—	Sample
• Group C	for Level B Product)	—	Sample
• Group D		—	Sample
LOT ACCEPTANCE			
• External Visual	Method 2009	Sample	Sample
• Fine & Gross Leak	Method 1014	Sample	Sample
• QA Electrical	Per Applicable Device Specification	Sample	Covered by Group A Test

VITESSE

ESD PROGRAM

- GaAs devices are inherently ESD sensitive
- Vitesse ICs have built-in ESD protection
- Each new family of products undergoes extensive ESD testing per MIL-STD-883C, Method 3015.7

Summary Data:	Telecom Products :	1500 V
	LP Series Gate Arrays:	2000 V
	FURY Series Gate Arrays:	3000 V

- Vitesse manufacturing line has ESD precautions per applicable EIA specs
- Customers are requested to follow ESD precautions while handling and assembling the ICs

RADIATION HARDNESS

- GaAs devices are inherently more rad hard than silicon devices
- Typical levels are:
  - Total dose ≥ 10^8 rads
  - Neutron fluence > 10^{14} n/cm^2
  - Transient dose (upset) ≥ 10^8 rads/Sec
  - Transient dose (survival) ≥ 10^{11} rads/Sec
- Vitesse rad-hard features
  - Interconnects on field oxide reduces photo currents
  - Buried P-layer improves transient upset performance
  - Aluminum metallization provides lesser scatter cross-section
- Results of tests on devices
  - Total dose up to 100 Mrads, no degradation
  - Neutron fluences up to 2 x 10^{15} n/cm^2, practically no change in gate delay

VITESSE

Electronic Microtech Associates
319 Littleton Road
Westford, MA 01886
(508) 692-0070 FAX (508) 692-7484

URGENT 11.8.10 Memo

LETTER

Date 11/10/89

To Dr. Steven Dy[redacted]

Subject Triquint

STD → ESH

Page 1 of 10

Steve,

What follows is a 9 page quote response for your ASIC. It is addressed to you, but was faxed to "Professor John Learned" @ U of H. (808-941-1455) last night at 9:00 PM our time.

I'll be in the office most of the day as if you have any comments or questions, just give me a call.

Good luck on your funding.

SIGNED John Toohey

[ ] Please reply ☐ No reply necessary

power and functional density for designs requiring high speed multiplexing and registering functions.

I look forward to working with you on this quotation proposal and the development of the "DVMAND Digitizer". If you have any questions or need additional information, please contact me at phone (503) 644-3535 x4025 or FAX (503) 644-3198.

Best Regards,

David Drummond

David Drummond
Product Marketing
Digital/Linear Products

cc: John Toohey - EMA

TriQuint SEMICONDUCTOR

Group 700, P.O. Box 4935
Beaverton, Oregon 97076

Phone: (503) 644-3535
FAX: (503) 644-3198

November 9, 1989

Dr. Steve Dye
Boston University

Subject: TriQuint Quotation #9-11-C-0007
Reference: Your fax request dated 10-21-89

Dear Dr. Dye,

Thank you for the opportunity to respond to the ASIC development outlined in your fax dated 11-6-89. I believe TriQuint's technology and design experience are well suited to implement the circuitry requested and hope this is reflected in the pricing and technical sections of this quotation. This letter is intended to provide additional information and clarifications and is to be made a part of the TriQuint quotation #9-11-C-0007 which is attached. This quotation is valid for a period of 60 days.

The following quotation proposal is for the semicustom development by Boston University of the "DVMAND Digitizer" ASIC. The ASIC will developed using TriQuint's QLSI™ standard cells and manufactured using TriQuint's QED Enhancement/Depletion Gallium Arsenide (GaAs) process. The QLSI standard cell functions are implemented with a fully differential logic known as Source Coupled FET Logic (SCFL). SCFL offers excellent speed, power and functional density for designs requiring high speed multiplexing and registering functions.

I look forward to working with you on this quotation proposal and the development of the "DVMAND Digitizer". If you have any questions or need additional information, please contact me at phone (503) 644-3535 x4025 or FAX (503) 644-3198.

Best Regards,

David Drummond
Product Marketing
Digital/Linear Products

cc: John Toohey - EMA

TECHNICAL DISCUSSION

Based upon the functional block schematic supplied in your fax and your discussions with Don Larson of TriQuint, the following estimates are provided.

The design will require approximately 900 core cells and 78 I/O signals resulting in a die size of 230x230 mils. The die size is slightly larger than TriQuint's 84 signal MLC132/84 package will allow. Although TriQuint offers a larger MLC196/128 package, the most economical solution would be to reduce the die size to fit into the MLC132/84 package.

Included in the 900 cells is the FIFO register block which requires approximately 440 core cells. TriQuint will provide a custom routed FIFO block reducing the resultant die size to approximately 210x210 mils allowing the use of the MLC132/84 package. There will be no charge for the custom FIFO block.

The design is straight forward and within the capabilities of the QLSI Standard Cells product.

STATEMENT OF WORK
Semicustom Design Option

TriQuint's semicustom design option distributes the development responsibilities between the customer and TriQuint. The logic design including simulation is the responsibility of the customer. TriQuint is responsible for the manufacture of the ASIC to the functional performance evaluated by the customer supplied test vectors.

TriQuint guarantees the logic functions supplied by TriQuint will operate as specified in the simulation models. Appropriate design margin is required to ensure operation over worst case conditions. A comprehensive design manual is provided detailing the specific design rules and guidelines.

Using the supplied workstation library, Boston University will complete the following tasks:

(1) Partition the system to fit the physical and electrical capabilities of a QLSI Standard Cell design. Guidelines to partition the design are included in the QLSI Standard Cell Design Manual.

(2) Design, enter and simulate the logic circuit using supplied macro symbols and models. The QLSI library is supported on DAISY and MENTOR workstations. The Standard Cell library contains all logic symbols, simulation models and development utilities required to complete the design task.

A supplied utility calculates the estimated macro delay loading value based upon statistical wiring capacitance and actual device loading.

Simulations should evaluate the design for nominal and worst case delay timing.

(3) Generate the design database containing the circuit schematic, netlist, and simulation test vectors.

(4) Perform package pin to I/O signal assignment using supplied placement parameter utility.

(5) Assign routing priority to critical nets. TriQuint's routing software will optimize the layout for the maximum performance of these nets. A development utility is supplied to assign the net priority.

(6) Submit the items in (3), (4) and (5) above to TriQuint Semiconductor.

STATEMENT OF WORK
Semicustom Design Option
(continued)

TriQuint Semiconductor will perform the following tasks:

(7) Review the design, test vectors and simulation results for general design violations. Resimulate the circuit to verify the test vectors and circuit performance.

(8) Automatic place and route the submitted design database based upon customer specified I/O placement and critical net priority information.

(9) Extract the parasitic wiring capacitance from the layout and backannotate into the design database in place of the statistical capacitance values. Resimulate using the backannotated capacitance values to ensure desired circuit performance is maintained. TriQuint will adjust the net priorities and/or manually place and route critical nets until the desired performance is achieved.

(10) Deliver the extracted capacitance file to the customer for backannotation into their design database. The customer resimulates the design for final examination of the post-layout performance. Written acceptance of the design from the customer is required before TriQuint will begin task 11.

The time from TriQuint receipt of design to delivery of extracted capacitance file is 2-4 weeks depending on design size, complexity and performance required.

(11) Generate the customer specific mask set for the QLSI Standard Cell ASIC.

(12) Fabricate the circuit using TriQuint's QED 1um Enhancement/Depletion Gallium Arsenide process.

(13) Test the wafers to meet the DC parametric performance as well as the functional performance using the customer supplied test vectors.

(14) Package the die and re-test using the same criteria as defined in (13).

(15) Deliver functionally tested prototype parts and test fixture. The high speed evaluation board is provided by TriQuint for rapid and accurate prototype evaluation.

DELIVERABLES AND SCHEDULE

The following items are considered deliverables to Boston University and will be billed in accordance with the enclosed pricing summary.

Item 1: QLSI Standard Cell library for Mentor Graphics workstation.

Includes QLSI Standard Cell Library cartridge, installation/utility guide and design manual.

Delivery: 1 week ARO

Item 2: Extracted capacitance file.

Boston University to evaluate the performance of their design using the extracted capacitance values. Written approval of the layout is required before TriQuint will continue the manufacturing process.

Delivery: 2-4 weeks from receipt of design database.

Item 3: Prototype parts packaged in MLC132/84 multi-layer ceramic leaded carrier.

40 Prototype parts:

5 Commercial parts included in NRE
35 Commercial parts optionally ordered with NRE

Delivery:

14-16 weeks from receipt of written layout approval from Boston University.

Item 4: (1) ETF-MLC132/84 high-speed test fixture.

Delivery: At time of prototype part delivery.

PRICING SUMMARY

Semicustom QLSI ASIC Development NRE: Includes: 5 Packaged Prototypes 1 High Speed Test Fixture	$75,000.00
Additional Prototype Parts: 85 units ordered with development NRE	$8,750.00

NRE charges will be invoiced in two phases:
55% of NRE following final design review.
45% of NRE following prototype delivery.

QUOTATION

TriQuint SEMICONDUCTOR

9-11-C-0007

DATE: 11-09-89

YOUR REFERENCE: FAXED REQUEST DTD 11/6/89

PLEASE REFER TO THIS NUMBER IN ALL CORRESPONDENCE

TO: BOSTON UNIVERSITY
DR. STEVE DYE

PLEASE DIRECT ORDERS AND INQUIRIES TO:
TriQuint Semiconductor, Inc.
Tektronix Industrial Park
Group 700, P.O. Box 4928
Beaverton, Oregon 97075

TERMS ON REVERSE SIDE AND EXHIBITS DO APPLY.

PHONE: (503) 644-3535

THIS QUOTATION WILL BE VALID FOR 30 DAYS.

ESTIMATED SHIPPING CAPABILITY IN WEEKS AFTER RECEIPT OF ORDER OR SOONER

F.O.B. FACTORY, BEAVERTON, OREGON

ITEM	QTY.	TYPE/PART NO.	MOD	DESCRIPTION	APPROX. SHIPPING WGT/UNIT	UNIT PRICE (IN U.S. FUNDS)	TOTAL (IN U.S. FUNDS)
1.	1			SEMICUSTOM QLSI ASIC DEVELOPMENT NRE Includes: 5 Packaged Prototypes 1 High Speed Test Fixture		$75,000.	$75,000.
2.	1			ADDITIONAL PROTOTYPE PARTS 35 units ordered with development NRE		$ 8,750.	$8,750.
				NRE charges will be invoiced in two phases: 55% of NRE following final design review. 45% of NRE following prototype delivery. The attached letter by David Drummond is to be made a part of this TriQuint Quotation 9-11-C-0007.			

THESE COMMODITIES ARE SUBJECT TO U.S. EXPORT CONTROL REGULATIONS.

A-1 9-Rule

QLSI™ Standard Cells

QLSI Standard Cells offer designers state-of-the-art capability in digital/linear ASICs. Designs requiring high speed, low power and direct interfaces to ECL, TTL and CMOS circuitry are ideally suited for implementation with QLSI Standard Cells. TriQuint designed the standard cell function based upon a fully differential logic structure known as Source Coupled FET Logic (SCFL) for maximum performance and flexibility. Three speed/power families offer designers the ability to tailor their designs for optimum speed with minimum power dissipation. The fully compatible ECL, TTL and CMOS I/Os eliminate the system level problems associated with non-standard interface levels.

TriQuint's proven QED™ Enhancement/Depletion Gallium Arsenide (GaAs) process is used to manufacture the QLSI Standard Cells ensuring consistent product of exceptional quality. QLSI Standard Cells are backed by extensive quality and reliability testing and evaluation.

Design examples for use with TriQuint MLC packages

Equiv. Gates	375	1000	2000	4500	10000
Unit Cells	75	200	400	900	2000
# of D Flip-flops	36	100	200	450	1000
# of I/O Cells	24	40	84	84	128
MLC Package	MLC44	MLC68	MLC132/84	MLC132/84	MLC196

High Performance

- Fully differential Source Coupled FET Logic (SCFL)
  - Excellent noise margin
  - True/complement outputs
  - Maintains signal symmetry
- Typical delays (FO=1)
  - Inverter = 90ps
  - 2-input NOR = 95ps
  - Flip-flop = 170ps Clk-Q, 85ps setup, 50ps hold
- Airbridge routing metal provides ultra-low wiring capacitance (70fF/mm)

Low Power

- 3 speed/power families
  - 2mW, 4mW and 8mW per complex cell
- Improved speed / power product over ECL

Standard Interface Levels & Power Supplies

- ECL, TTL and CMOS I/Os
- -5V (+/-10%), GND, optional +5V for TTL/CMOS I/O

High Speed Packaging

- TriQuint designed 44, 68, 132 and 196 pin MLC packages
- Designed for reflow solder board mount
- 50 Ohm environment from bond pad to package lead
- High speed evaluation board with quick connect socket

Software / Design Support

- Workstation libraries for Daisy and Mentor Graphics
- Design manual with guidelines for logic circuit design
- Design reviews and consulting
- Extensive design verification

- Supports LSI Solutions Beyond 2GHz
- 10,000 Equivalent Gates
- 128 High Speed I/O
- Integrated ROM Cells
- Mixed Analog & Digital Circuitry
- Commercial & Military Temperature
- Mil-STD-883C Screening
  - Class B Package
  - Class S Die
- Directly Interfaces to ECL, TTL and CMOS Based Systems
- Optional Design by TriQuint to Customer Specifications

APPLICATIONS:

- High Speed Logic
- Digital Signal Processing
- Waveform Generation
- Crosspoint Switch Matrix
- Accumulators
- NCOs
- Direct Digital Synthesis (DDS)

Summary

QLSI Standard Cell Workstation Macro Library

Cell Function	Name	Cell Function	Name
Inverter	SX10	2-Bit Accumulator	SXACC_2
Clock Driver	SF10	Carry Generate	SXCG
		ROM	
2-Input OR/NOR	SX20		
3-Input OR/NOR	SX30	Master Latch	SXDDML
4-Input OR/NOR	SX40	Master w/ Reset	SXDDMLR
5-Input OR/NOR	SX50	Master w/ Set	SXDDMLS
6-Input OR/NOR	SX60		
		Master/Slave	SXDDFF
2-Input Exclusive OR/NOR	SX2XOR	Master/Slave w/ Reset	SMDDFFR
3-Input Exclusive OR/NOR	SX3XOR	Master/Slave w/ Set	SMDDFFS
		Master/Slave Reset/Set	SXDDFFRS
2-Input AND/NAND	SX01	Master/Slave w/2:1 Mux	SXMDDFF
3-Input AND/NAND	SX3AND		
		TTL Input	IMTS1
1 AND, 1 OR/INVERT	SX11	CMOS Input	IMCS1
1 by 2-Input O/A	SXOA12	TTL/CMOS Output	OXSO1
2-Input Multiplexer	SX2MUX	ECL Input (Single-ended)	IXES1
4-Input Multiplexer	SX4MUX	(Differential)	IXES2
8-Input Multiplexer	SX8MUX	ECL Output (Single-ended)	OXSE1
		(Differential)	OXSE2

Linear Function Blocks

TriQuint offers linear function blocks for integration into QLSI standard cell designs. Each functional block has been characterized and can be implemented as-is. Typically, each application will require modification to the functional block to meet the required specifications. TriQuint will work with each customer and modify the basic functional block to meet the design requirements. TriQuint will perform all design modification and layout tasks.

Amplifiers:	
Bias Amplifier	AA01
Operational Amplifier	AA02
High Speed Buffer	AA03
Laser Drivers:	
Single Stage	LD001
Multi-Stage	LD002
Multi-Stage w/ Output control	LD003

Transimpedance Amplifiers:	
Single Supply (+5V)	
Single Stage	TA01-1,2
Multi-stage	TA01-3
Dual Supply (+/-5V)	
Single Stage	TA02-1,2
Multi-stage	TA02-3
Misc. Functions:	
Comparators	
Digital to Analog Converters	
Analog to Digital Converters	
Voltage Controlled Oscillators	

Multilayer Ceramic Packages

The QLSI Standard Cells are packaged in TriQuint's MultiLayer Ceramic (MLC) packages. The MLC packages were developed at TriQuint to support the special requirements of very high performance ICs. The packages are designed to handle clock rates up to 3.5GHz and edge rates less than 125ps. Signals are carried on 50-Ohm controlled impedance transmission lines from the package leads to the bond pads. Excellent signal isolation is provided by the use of multiple ground pins. Power planes and decoupling capacitors minimize switching noise on the power supplies.

The packages are fabricated from cofired alumina ceramic. The ceramic packages easily handle power dissipation of 1.5 Watts and can handle 4-10 Watts circuits with the addition of a suitable heat sink. The packages support both epoxy and solder die attach and lid seal and are capable of hermetic operation.

For further information contact:

Sales Department
TriQuint Semiconductor, Inc.
Group 700, P.O. Box 4935
Beaverton, OR 97076
(503) 644-3535
FAX: (503) 644-3198

SHEET 1 of 3

Electronic Microtech Associates
319 Littleton Road
Westford, MA 01886
(508) 692-0070
FAX (508) 692-7484

Memo
LETTER

To Dr Steven [redacted]
B.U.

Date 11/10/89

Subject Triquint
STD → ESH

Steve,

What follows is a 2 page addendum to our quote response on your ASIC. It was faxed to Professor Leonard at U of Hawaii at about 4:00 PM our time today.

Again, any questions just give me a call.

John Toohey

☐ Please reply ☐ No reply necessary SIGNED

[redacted] the test vectors (low speed test). Additionally, [redacted] operate as specified in the QLSI Design Manual and the workstation library models.

TriQuint will work with Boston University during the entire development process to ensure a successful first time design.

Prototype Re-design Charges:

Design Layout:	$2,000-$6,000
Mask Charges :	$2,000 per layer
(4-11 layers)	
Wafer Fabrication:	$28,000 per run
Typical re-design charges:	$38,000 - $56,000

TriQuint SEMICONDUCTOR

Group 700, P.O. Box 4935
Beaverton, Oregon 97076

Phone: (503) 644-3535
FAX: (503) 644-3196

November 10, 1989

Dr. Steve Dye
Boston University

Subject: Quotation Addendum
Reference: TriQuint Quotation #9-11-C-0007

Dear Dr. Dye,

This quotation addendum is to be made a part of TriQuint quotation #9-11-C-0007. In reviewing the above referenced quotation, I realized I did not include the re-design pricing information requested.

Re-design charges will vary depending on the level of changes required. The variable charges are the design layout and mask charges. If the design change is due to a wiring error, only the two (2) logic cell interconnect layers will require changes. Cell interconncet changes will require four (4) new mask layers. If additional or different logic cells are used, the chip layout will change requiring all 11 mask layers and additional time for layout.

I want to stress that these re-design charges are only for design changes requested by Boston University. TriQuint guarantees the prototype parts will function as specified with the test vectors (low speed test). Additionally, TriQuint guarantees the logic cell macros to operate as specified in the QLSI Design Manual and the workstation library models.

TriQuint will work with Boston University during the entire development process to ensure a successful first time design.

Prototype Re-design Charges:

Design Layout:	$2,000-$6,000
Mask Charges :	$2,000 per layer
(4-11 layers)	
Wafer Fabrication:	$28,000 per run
Typical re-design charges:	$38,000 - $56,000

If you have any questions or need additional information, please contact John Toohey - EMA at (508) 692-0070 or myself at (508) 644-8585 x4025.

Best Regards,

David Drummond
Product Marketing
Digital/Linear Products Division

cc: John Toohey - EMA