DIR-21-90

Circuit with New Output Pulse Structure for JOM

by H. Kawamoto *)

Tohoku University

At the Sendai meeting (October , 1990) , we decided to try new JOM(Japanese Optical Module) output pulse structure which consists of pulse corresponding to the charge and notches obtained through clipping of PMT pulse .

In this report , we describe that it is possible to build the circuit for the new structure , and point out that there are still problems of the circuit . We consider how to solve the problems .

§ 1 SPS test and Old Specification

In SPS , the output pulses from PMT are amplified by a preamplifier (NE5539) and fed to a discriminator chip (MVL407) which converts the pulse to time-over-threshold signals. The width depends logarithmically on the amplitude of PMT pulse . In order to get adequate resolution when pulses are digitized with a 200 MHz clock in SBC , the time-over-threshold pulse width is stretched by a factor of ten .

---

*) The circuits presented here were studied and built by H.Kawamoto , keeping discussions with **A.Okada** (I.C.R.R.- Tokyo) and other DUMAND colleagues .

Before the U.Maryland meeting , the JOM output pulse structure was specified to have the time-over-threshold pulse width with notches . The width is digitized with 1 GHz clock (but now is digitized with 500 MHz clock in SBC) and not stretched .

§ 2 3 Type of pulse structure

First , the JOM pulse structure proposed by the Japanese group at the Maryland meeting (April , 1990) has information on both pulse width and charge shown in Fig.1-(b). The first pulse has a width of PMT output pulse over threshold . The second pulse is logarithmically propotional to the integrated charge (lnQ) and starts at 100 nsec after the beginning of the first pulse .(In the following , this structure is called " Type 1 ") .

At the Bern meeting (June , 1990) , the discussion seemed to reach another conclusion that the second pulse should start just 5 nsec after the end of the first pulse(Fig.1-(c)). (In the following , this structure is called " Type 2 " .)

However , at Trigger Workshop (Seattle , July,1990) , " Type 1 " was chosen as the JOM pulse structure .

After discussion about the pulse structure at Sendai meeting (October, 1990), we decided to take new pulse structure which is shown in Fig.1-(d). The new pulse structure has the charge (lnQ) with notches. When PMT outputs double-(multi-)pulse , notches are expected to show us rising-points .(In the following this structure is called " Type 3 ").

We describe and discuss the circuit for the structure " Type 1 " and " Type 2 " in Appendix .

§ 3 The new circuit for JOM

The outline of the circuit for the structure " Type 3 " is shown in Fig.2 which is based on the discussion at the Sendai meeting . This circuit consists of a Pre-Amp. , Notcher , integrator , and discriminators . As mensioned above , the width of the circuit outout pulse corresponds to the PMT output charge (lnQ) and notches in the pulse show rising-points of PMT double pulses .

3 - 1 Pre - Amp.

The Newest Hamamatsu 15 inch photomultiplier will be producted in Mid-December. We expect the PMT has a gain of 10^8 , but if it is only several times 10^7 , a pre-amp. must be needed . A pre-amp.(CLC400) test circuit is shown in Fig.3 . The test circuit has a gain of 5 . This chip has an ability of 1 to 8 closed-loop gain range and low power consumption (150 mW) . This chip was suggested by M.Jowarski (U. Winsconsin) . Pulse response of this circuit is shown in Fig.4 . Propagation delay time is about 2 nsec .

3 - 2 The notch circuit using a clipping line

The notch circuit using a clipping line was proposeed by M.Webster (Vanderbilt U.) at the Sendai meeting . The test circuit of the notch is shown in Fig.5 which consists of a OP-Amp.(NE5539) and a delay line . The delay line is used a FSL05-020A (Showa Electric Wire & Cable Co., Ltd) chip . Mechanical dimensions of the delay line chip are 26.5*11.0*2.54 mm^3 . PMT output pulses are amplified by the OP-Amp. and transmitted to the delay line . PMT output pulses are inverted at the end of the delay line and added to original pulses . We can possibly find rising-points of PMT output pulses using this circuit . Input pulses from a Pulse Generator and output pulses are shown in Fig.6 . It is possible to separate two pulses which come about 15 nsec interval , but the clipping circuit output width over threshold is not fixed because width depends on the form of PMT output pulses .

3 - 3 The charge circuit

The charge circuit is shown in Fig.7 which consists of integrator and a comparator (MVL407) . Integrator is made of a LM6365 chip. The output time-over-threshold pulse width of integrator output is propotional to lnQ . Fig.8 shows a relation of lnQ vs. time-over-threshold pulse width. Input pulse waveforms are rectangular . In Fig.8 , several kinds of marks point out different input pulse widthes . The threshold of the comparator is setted at 50 mV .

The increase of time-over-threshold pulse width is not linear above several thousand mV*nsec due to saturation of the integrator (Fig.9). But if we calibrate the circuit enough , we can estimate charge from the time-over-threshold pulse width though ,of course , the resorution is a little worse in the saturation region . In fig.2 , outline of the whole circuit is shown . A discriminator after the Pre-Amp. produces PMT output time-over-threshold pulses for finding accurately first rising points . The output width of the whole circuit is determined by the logical OR between PMT output widthes and integrator output widthes . A test circuit for generating total width is shown in Fig.10 . An obtained relation of lnQ vs. total width is shown in Fig.11 .

3 - 4 Selection of the parts

A plan of the new circuit is shown in Fig.12 . We have not made a decision yet about which chip we use for the notch circuit . A candidate is CLC400 or NE5539 . CLC400AJE is very small . Mechanical dimensions of this chip are 5.1*6.4 mm^2 . As the delay line for clipping we use FSL05-020A chip . Comparator chip is MVL407S . Its mechanical dimensions are 12.7*7.4 mm^2 . The power budget of the circuit is about 1.5 W .

§ 4 Consideration of the new circuit

As mentioned above , it is possible to build the new circuit for the structure " Type 3 " , but we think , in 2 bad cases , it could happen that the circuit output pulses does not satisfy structure " Type 3 " . The 2 cases are shown in Fig.13 .

In case of Fig.13-1 , the circuit can not point out the first rising-point of PMT output pulse , and we misidentify the delayed pulse from the integrator . We think that if the discriminator which detects the first rising-point does not change Low to High level , the time-over-threshold pulse of the integrator output should be suppressed using one shot gate .

In case of Fig.13-2 , output pulse structure looks satisfying with the structure " Type 3 " . However the PMT output is a single pulse , we misjudge it as double pulses . If the discriminator which detects a first rising-point changes Low to High level , the discriminator should keeps High level for several tens nsec and such " crack " should not be created .

Considering those cases above , we propose the circuit which is shown in Fig.14 . Since it is possible for the notch circuit to find a first rising-point of a PMT output pulse and we don't check the end of

" width " pulse , the discriminator after a Pre-Amp. may not be needed . If one shot multivibrator(50 nsec width output) is inserted after the discriminator in the notcher ,it is impossible to create a " crack " as in Fig.13-2 . When a first rising point is not detected (as shown in Fig.13-1) , integrator time-over-threshold pulse cannot be outputted because gate signal from one shot multivibrator (700 nsec width) is suppressed .

§ 5 conclusion

As we described in this report , we can build the circuit for the structure " Type 3 " , but there are still problems shown in Fig.13 . If we build the circuit shown in Fig.14 , the problems will be solved . The circuit shown in Fig.14 will consume about 2.4 W . However the circuit shown in Fig.14. has not been built nor tested yet . We must build and test it rapidly .

At the same time , the Monte Calro study of the DUMAND Array must be needed enough . Not only multi-muon events but also ν_e's charge current events should be studied . Is it helpful of the JOM circuit to estimate energies of ν_e events and hadronic cascades or not ? In order to study neutrino oscillations by detecting the 20 GeV neutrino beam from the Fermilab Main Ring Injector , is it helpful to separate ν_e events , ν_μ events and Neutral Current events or not ? Is it helpful and useful to detect multi-PE signals caused by Supernova Neutrinos ? We must solve these questions rapid soon !

Appendix A The circuit for the structure " Type 1 " and " Type 2 ".

We have considered and discussed the circuits for the structure " Type1 " and " Type 2 " . We describe these circuits in this section , since what we have considered and discussed for the circuit may be helpful in the future development of Optical Module .

§ A - 1 On the structure " Type 1 "

For the structure " Type 1 " , we first considered a circuit using a peak holder (Fig.A-1). PMT output pulse is integrated by a charge integrator . Integrator outout signal is hold by the peak holder. When the peak holder gets a reset signal , a cliff wave is transmitted to differentiator . Since a fast peak holder looks difficult to develope , we gave up to build this circuit .

Fig.A-2 shows a circuit using Logic Hold Comparators and Fig.A-3 shows the timing chart of this circuit . We presented this circuit at Sendai meeting , but it was rejected because it is needed many chips and has a heavy power consumption . There isn't time nor money to make the whole circuit into a new chip.

When PMT signal is fed to this circuit , discriminator outputs the time -over-threshold pulse width , and edge detector makes Start and Gate signals. On the other hand , PMT output pulse is integrated by integrator . Integrater output pulse is transmitted to many Logic Hold Comparators. A Logic Hold Comparater consists of MAX9687 comparator (with Latch) and OR gate (See Fig.A-4). When Logic Hold Comparators get start signal , the comparator functions nomally . If the comparator output logical level is High , the Logic Hold Comparator keeps High Level. When Gate signal comes , AND Gates send rectangular waves to delay lines which have time constants different from each others about 5 nsec.These rectangular waves are transmitted to OR Gate , which makes a charge signal. Finally the circuit outputs the width and charge signals.

If using this circuit , any output dependence on Q can be chosen (lnQ , linearQ , (linear + ln)Q ...) . Charge resolution depends on the number of comparators. If we produce a Gate signal after the end of " width " pulse , it is possible to output " Type 2 " structure , too .

§ A - 2 On the structure " Type 2 "

For the structure " Type 2 " , we considered a circuit to make the second pulse which last from the peak of integrator output pulse to its falling threshold . This circuit is shown in Fig.A-5 . Time-over-threshold pulse width of integrator output is proportional to lnQ . If we demand that integrator has lineality for about 100 nsec , integrator has a long tail (over 500 nsec) . If PMT outputs after-pulses which are caused by optical background , noise ,or something else during the time , we estimate charge too large .

List of Figures

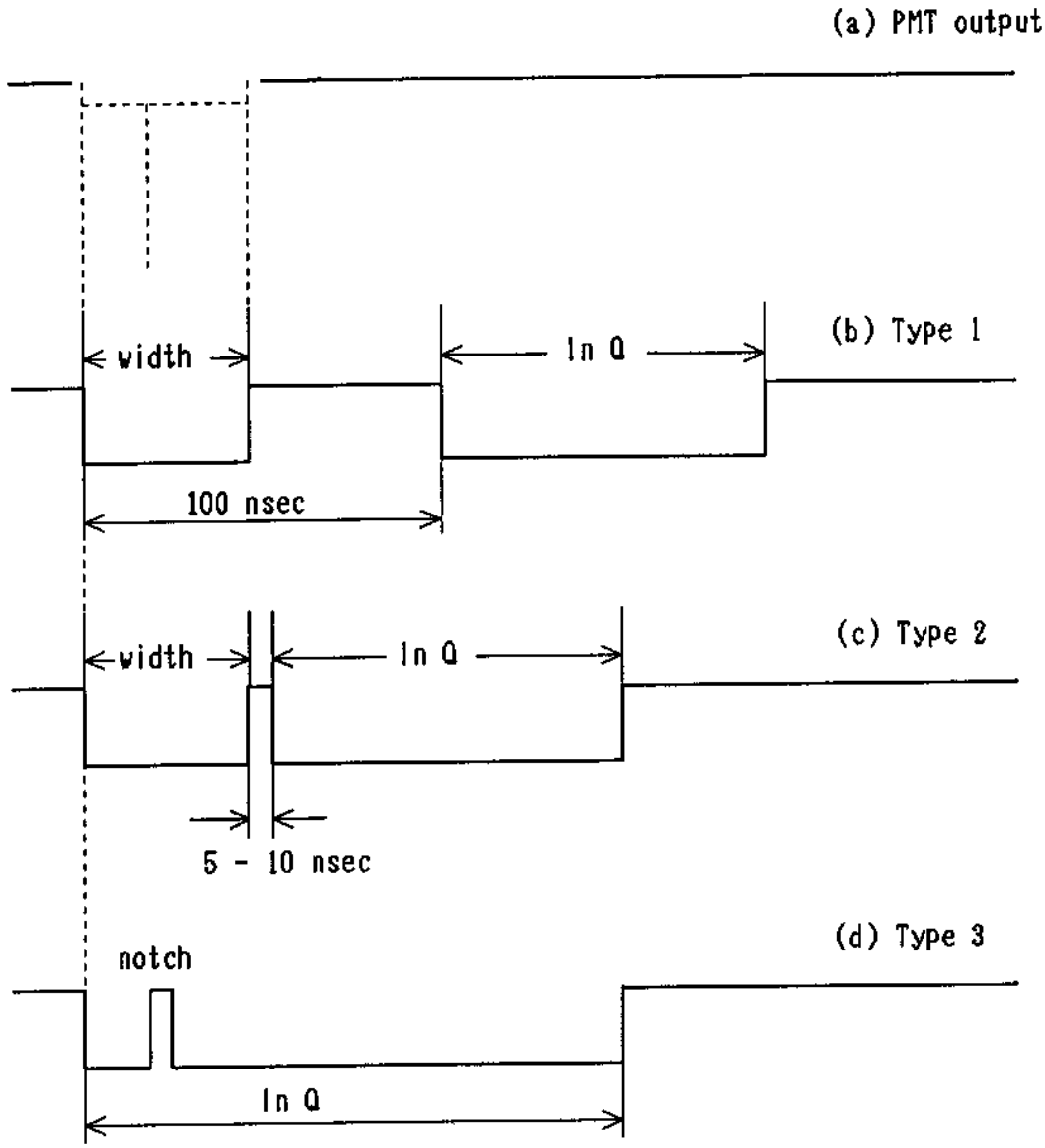


Fig. 1 three type output structure

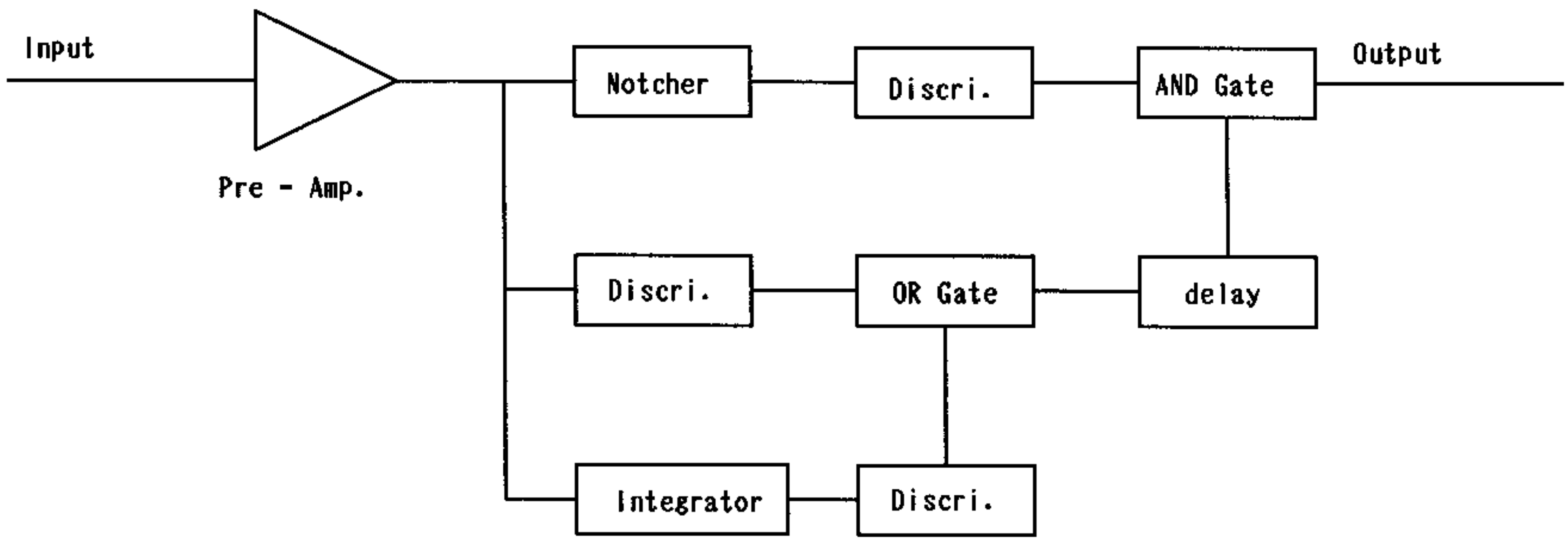


Fig.2 the circuit for " Type 3 " structure

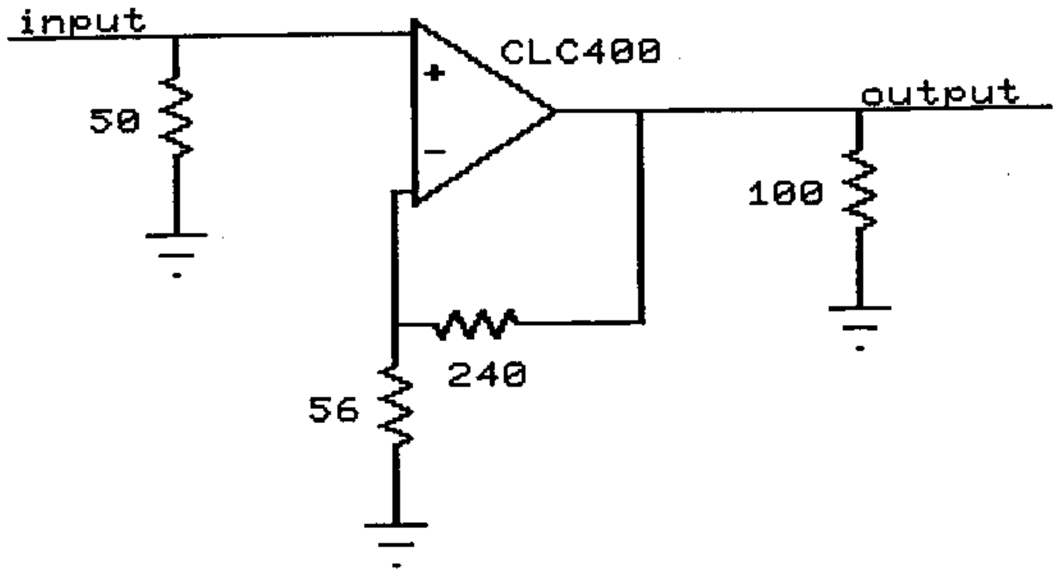


Fig.3 the test circuit of a Pre－Amp.

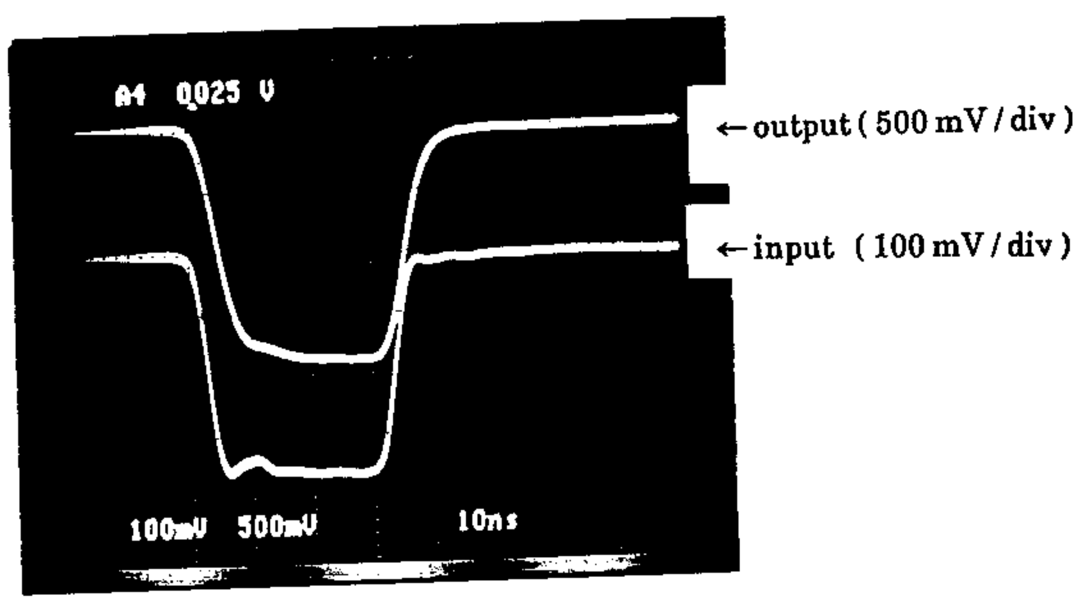


Fig.4 pulse response of a Pre－Amp.

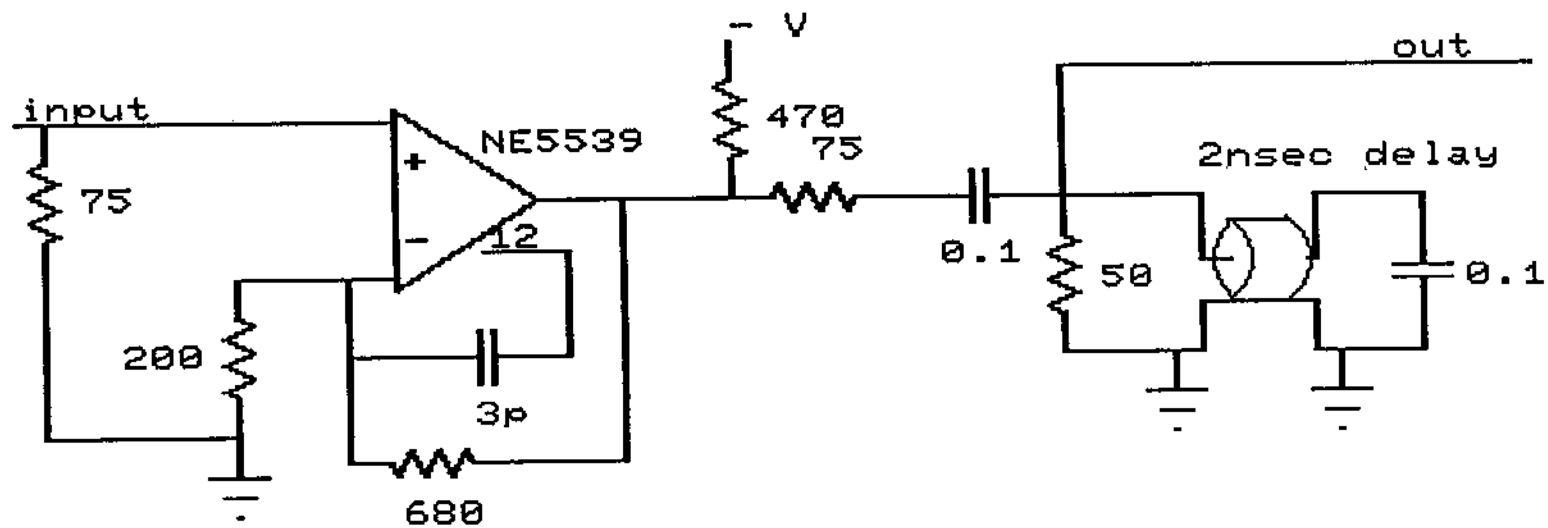
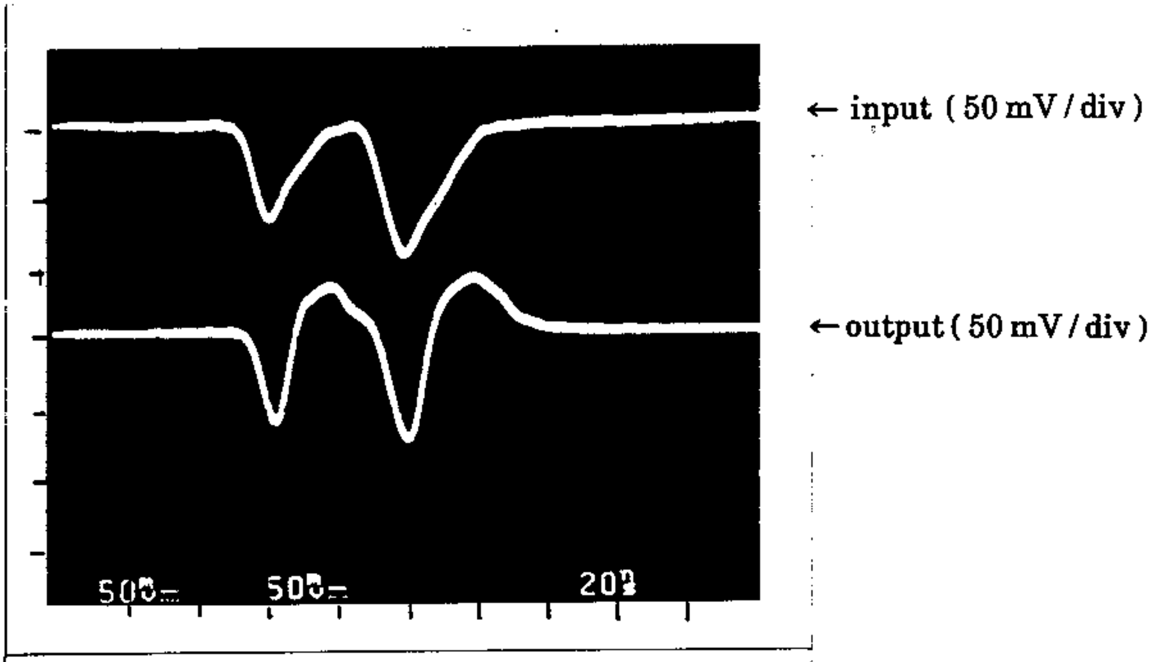
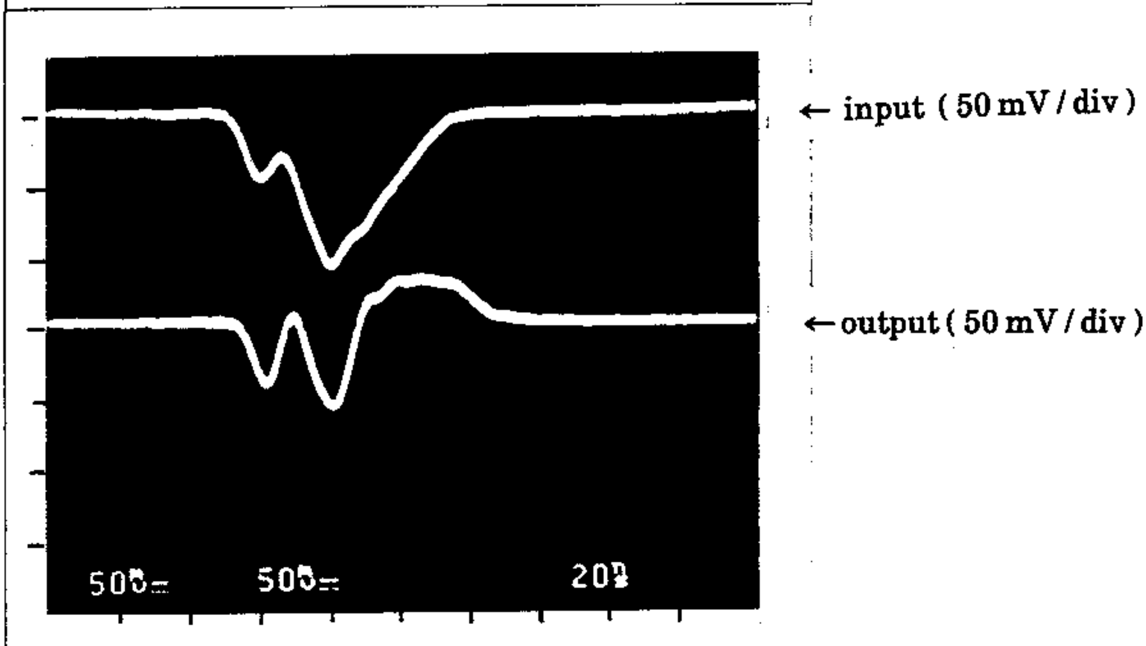
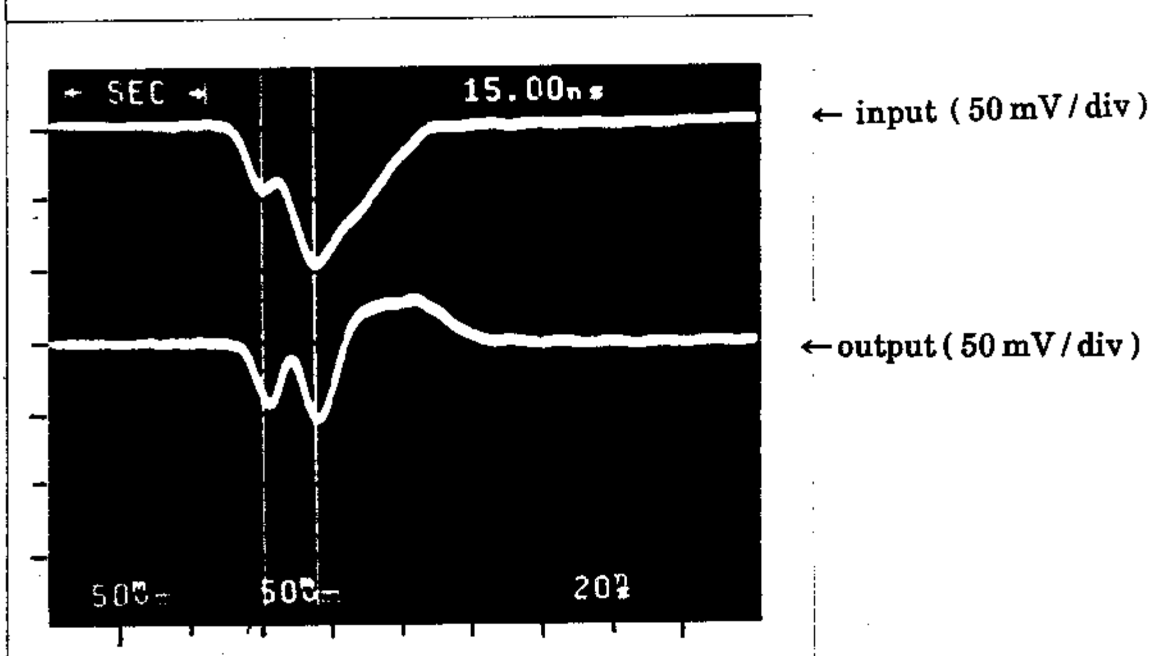


Fig.5 the notch circuit using a clipping line


← input (50 mV / div)
← output (50 mV / div)


← input (50 mV / div)
← output (50 mV / div)


SEC
15.00ns
← input (50 mV / div)
← output (50 mV / div)

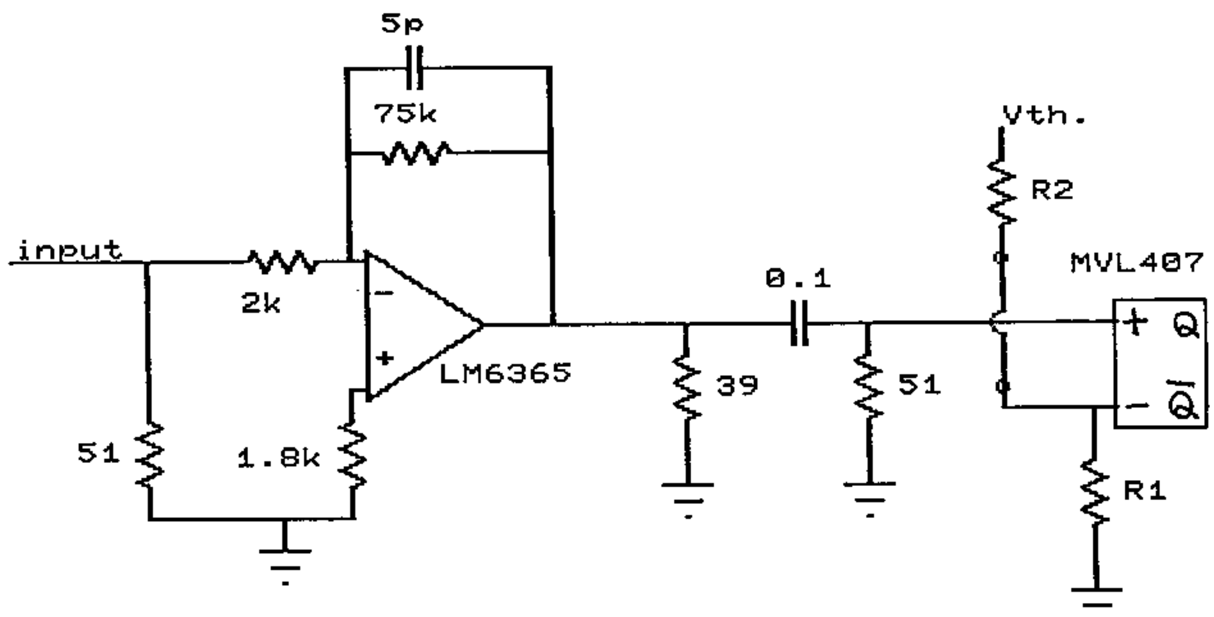


Fig.7 the charge circuit

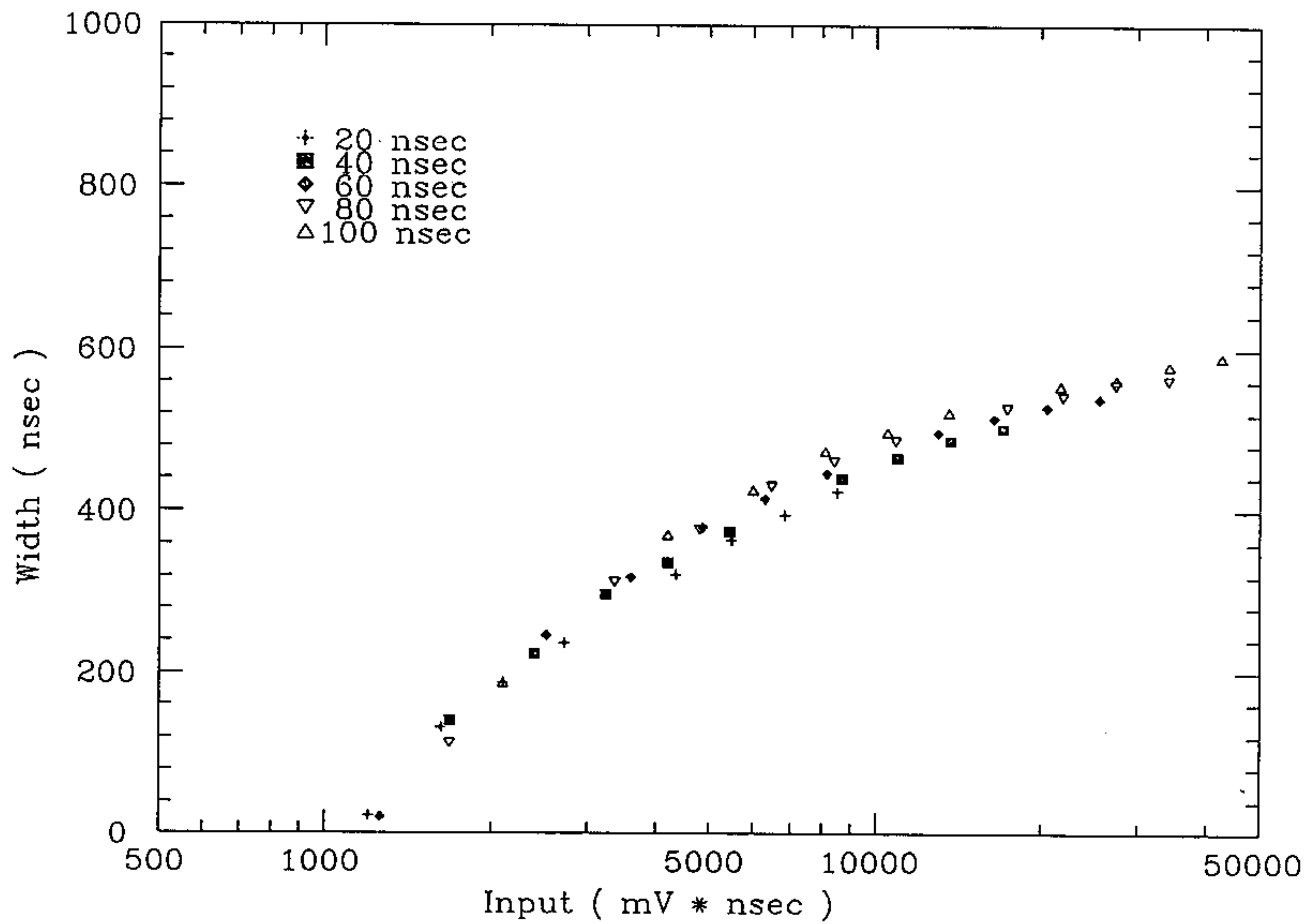


Fig.8 a relation of lnQ vs. integrator output time-over-threshold pulse width

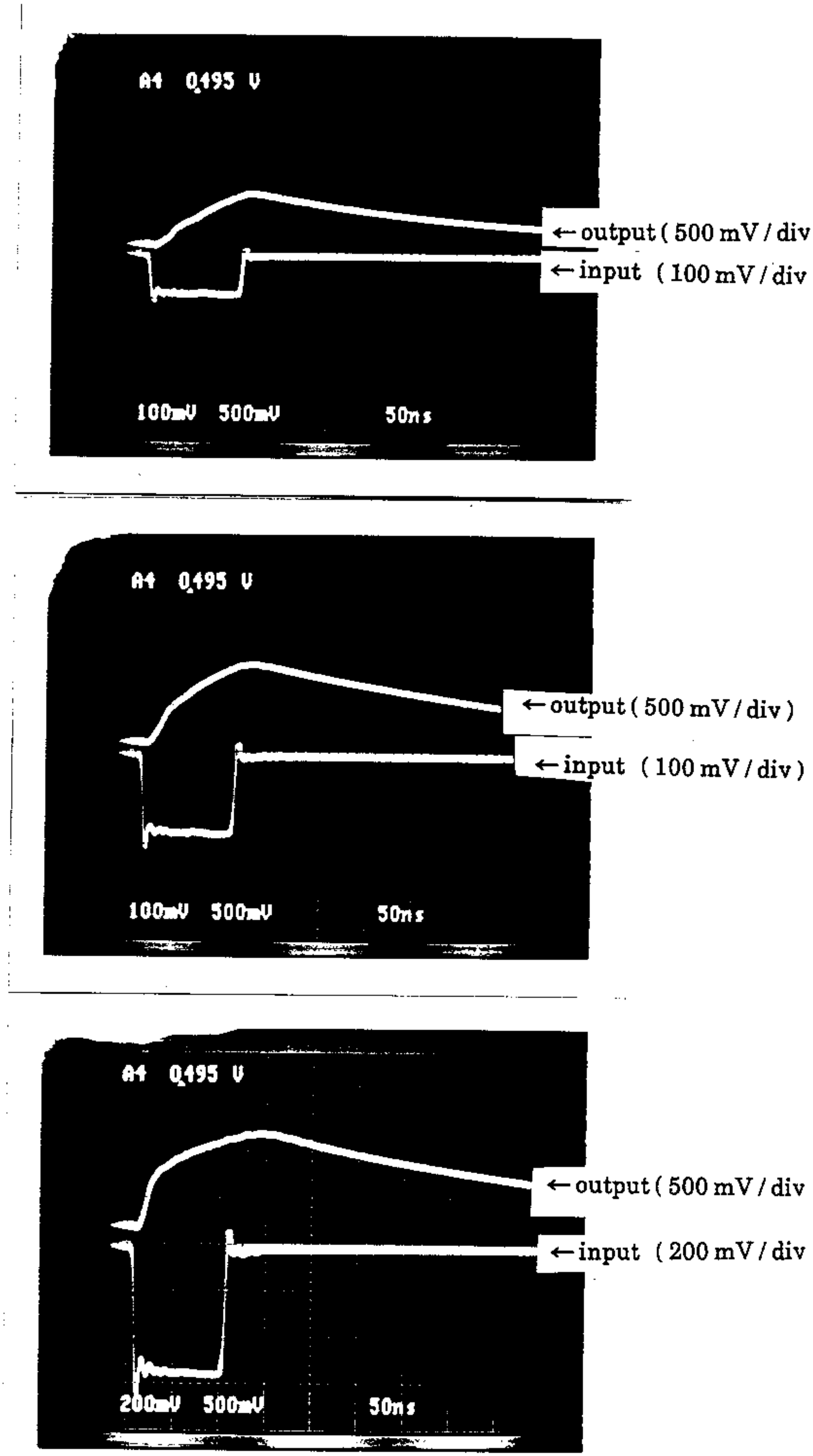


Fig.9 response of integrator

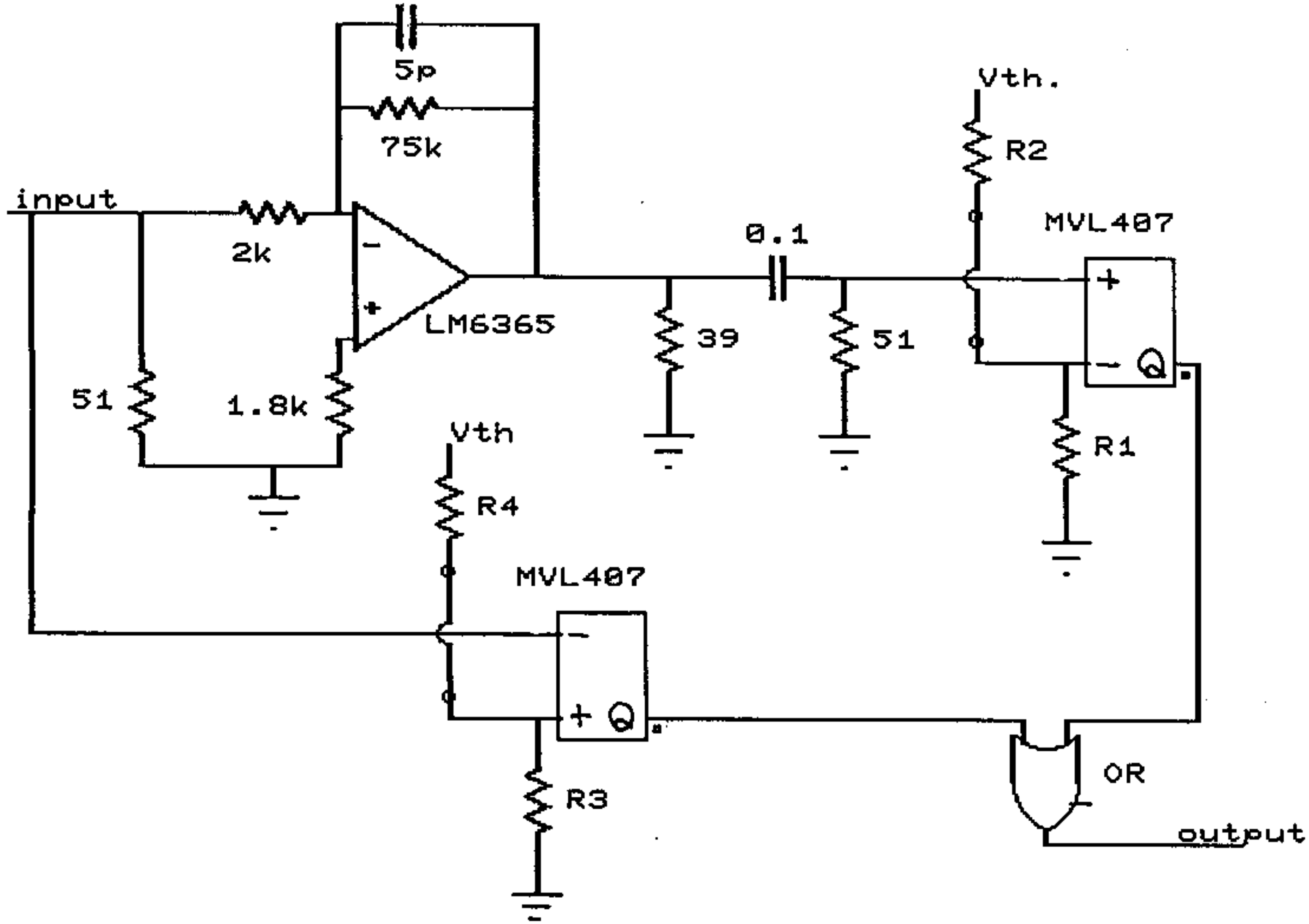


Fig.10 the test circuit generating total width pulse

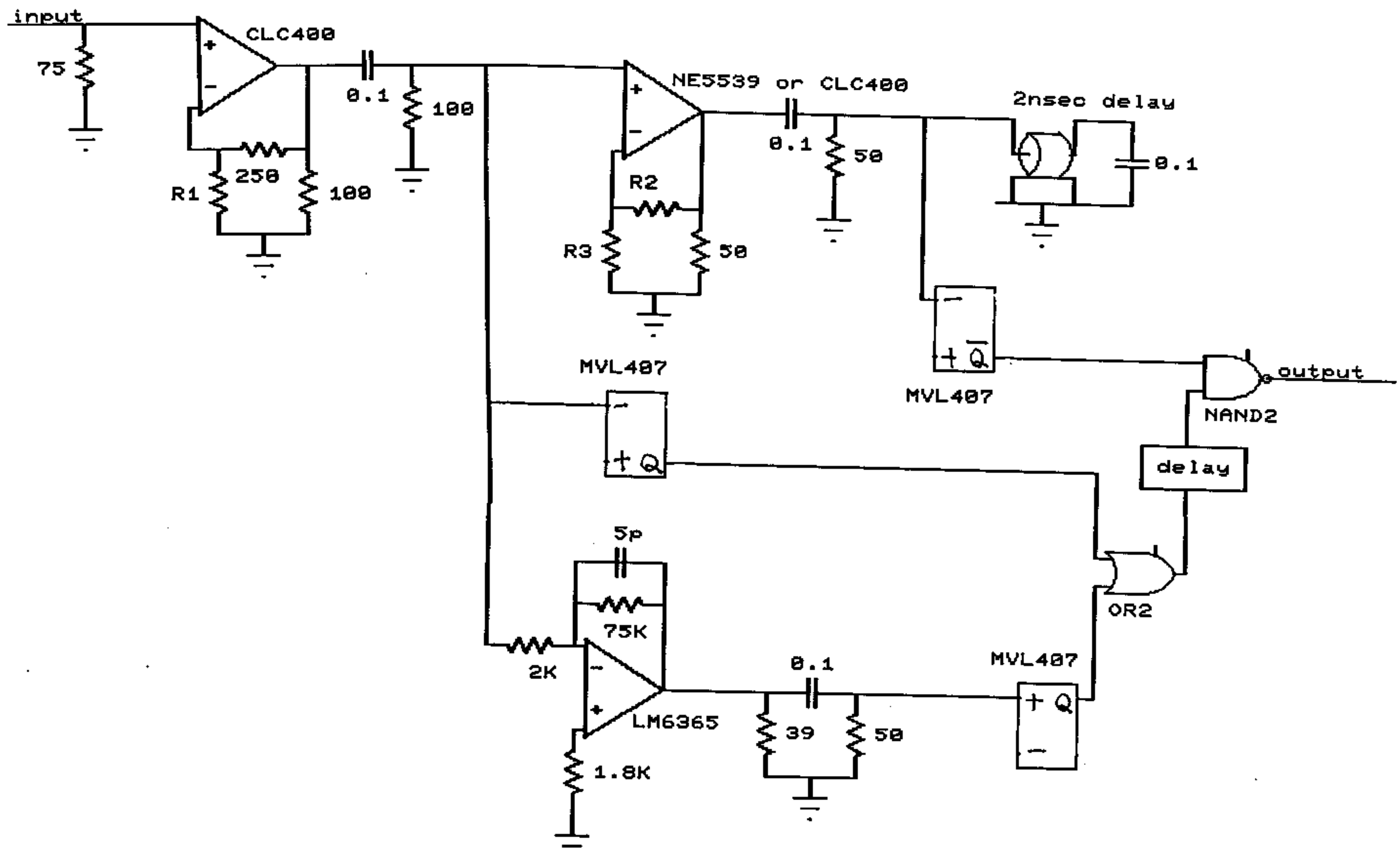


Fig.12 a plan of the whole circuit

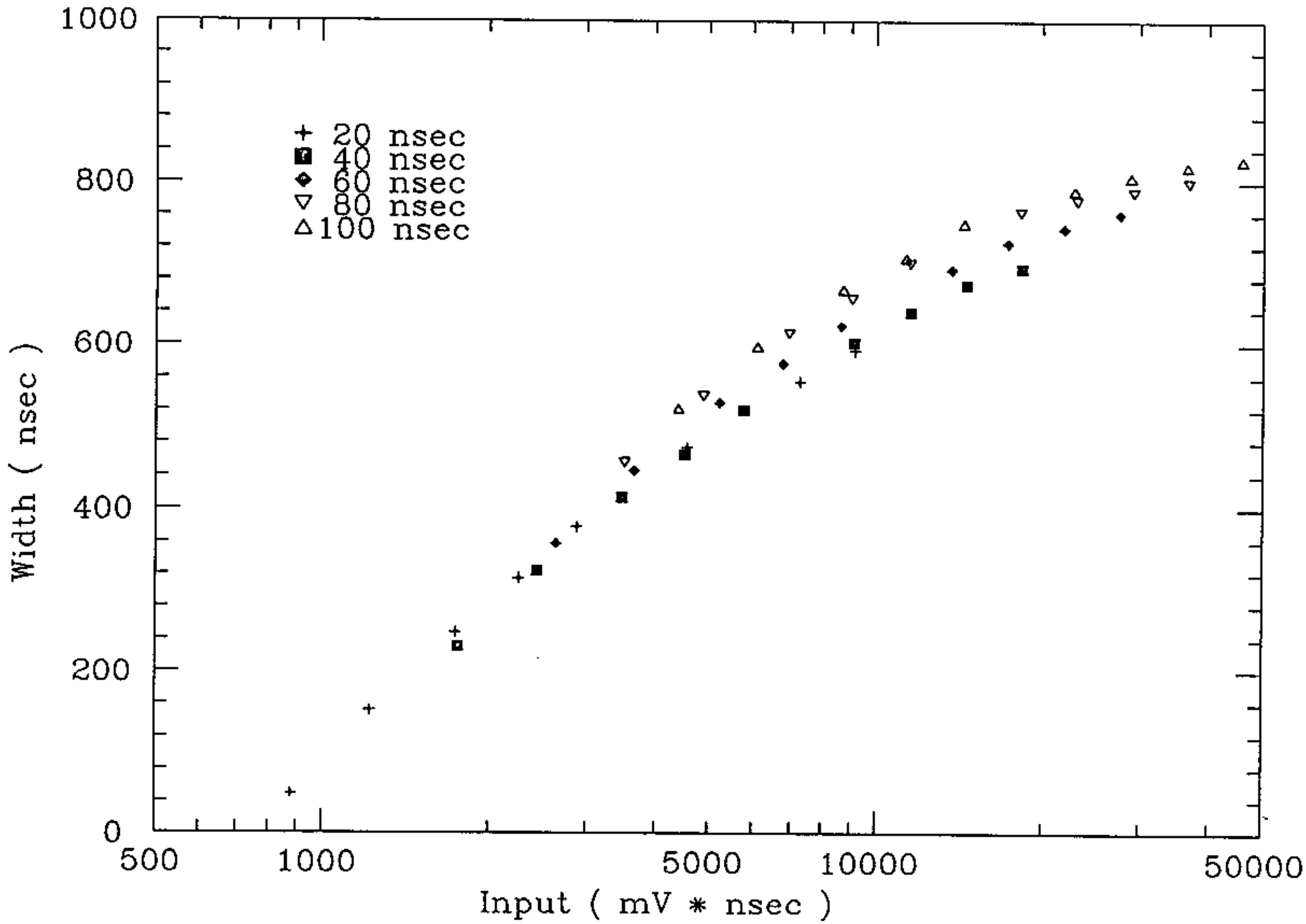


Fig.11 a relation of lnQ vs. total width

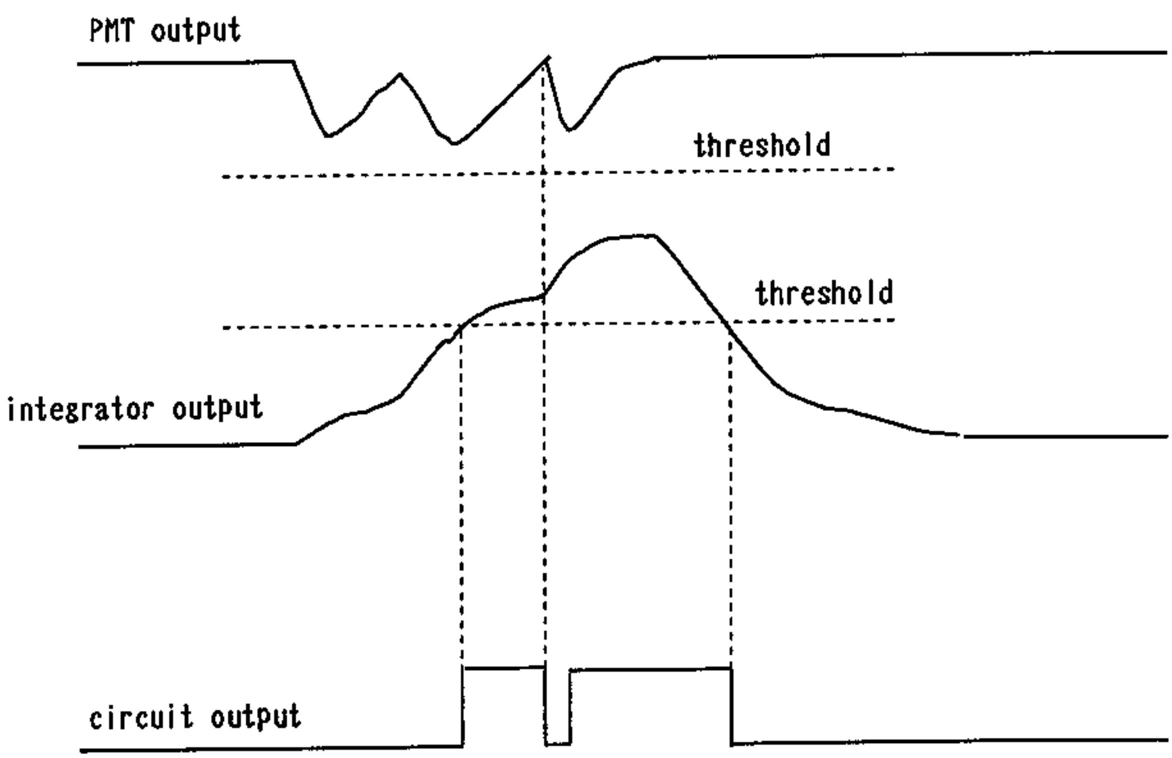


Fig.13-1 bad case 1

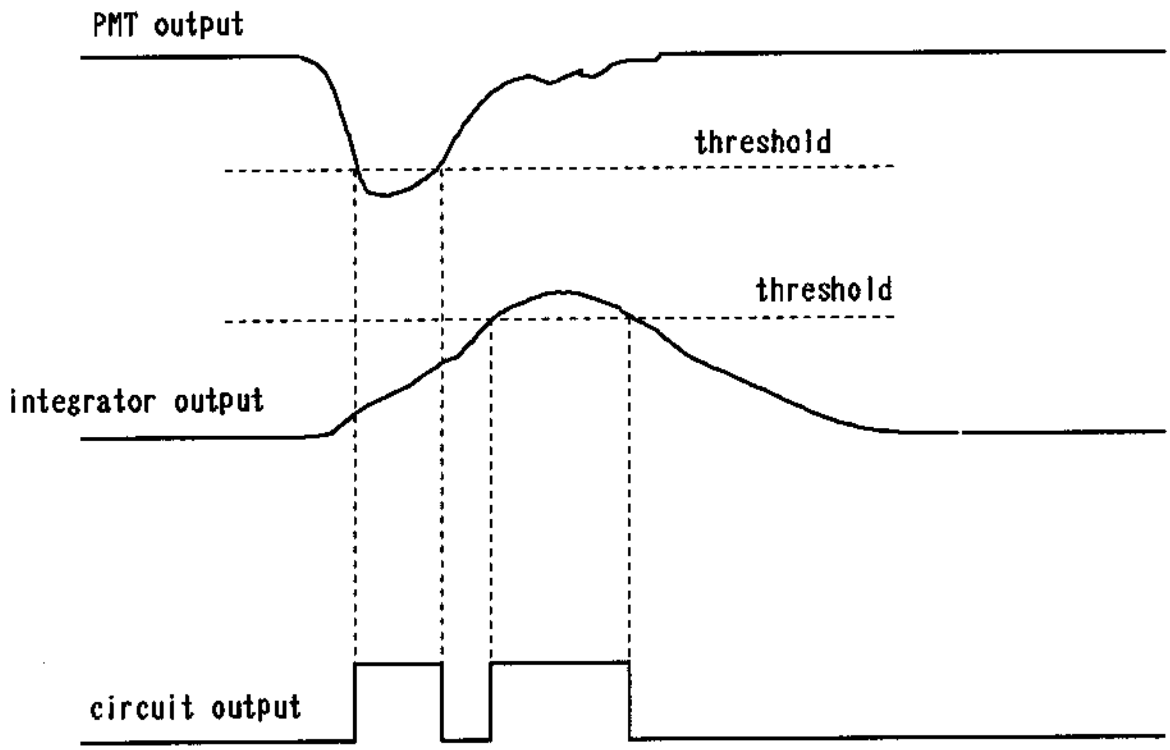


Fig.13-2 bad case 2

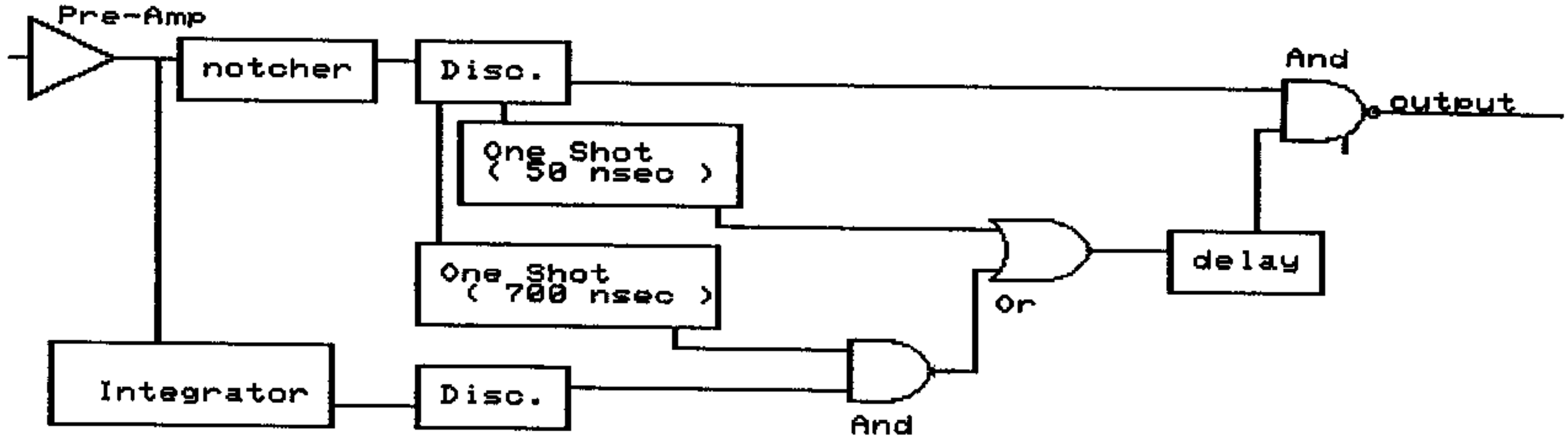


Fig. 14 a circuit using one shot gates

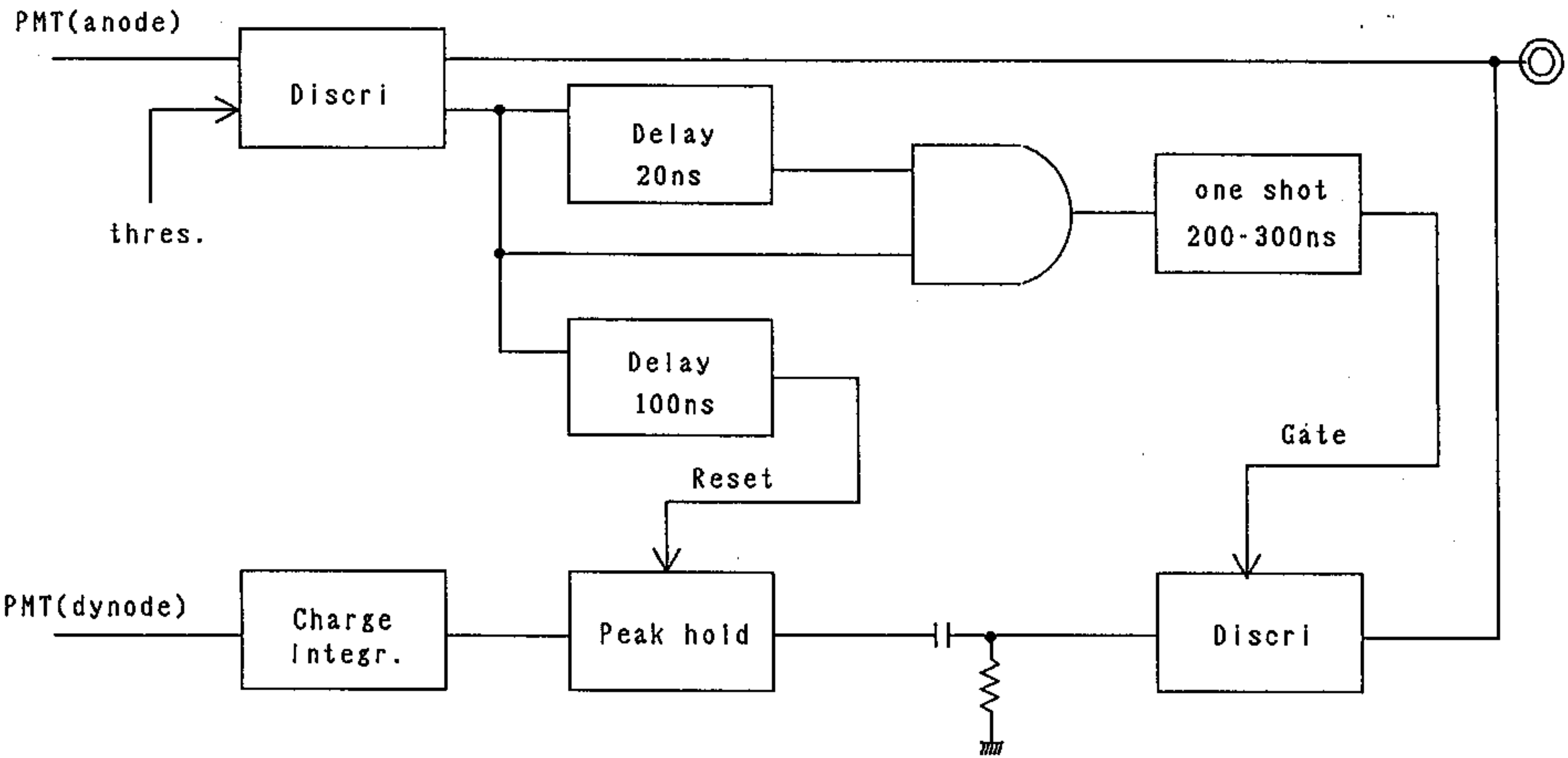


Fig. A - 1 a circuit using a peak holder for the structure “ Type 1 ”

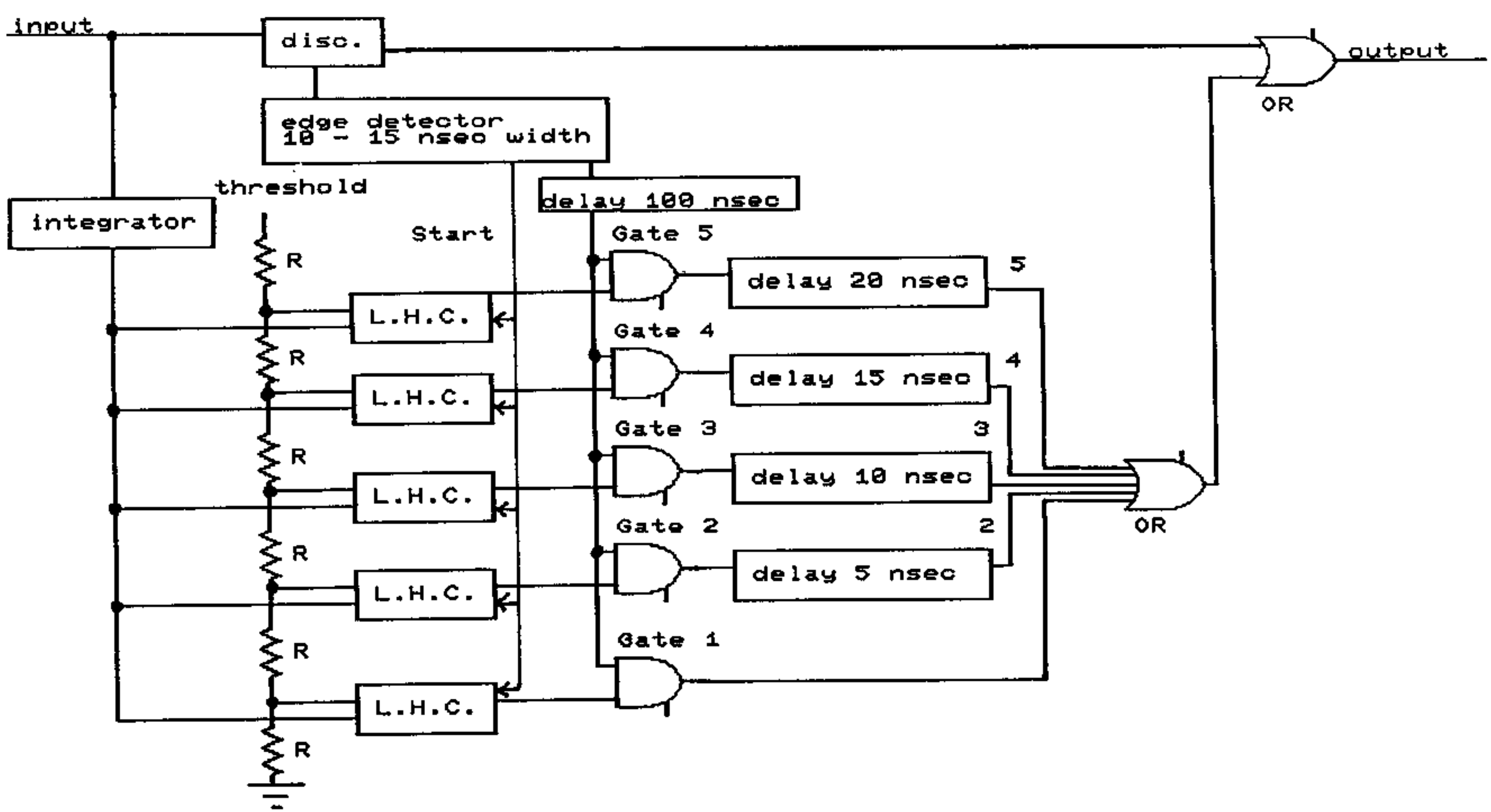


Fig. A - 2 a circuit using Logic Hold Comparators (L.H.C.)

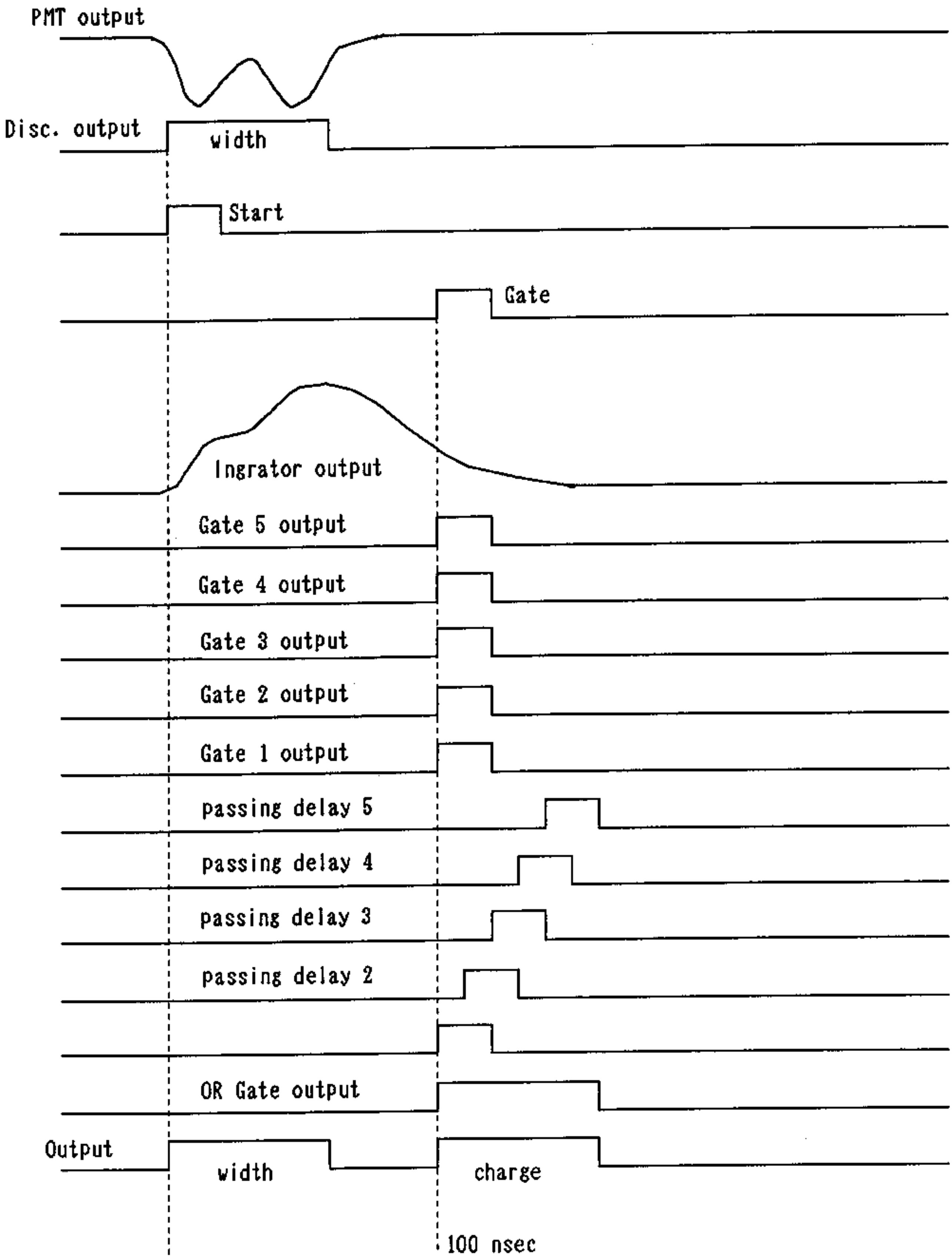


Fig.A-3 timing chart of a circuit using Logic Hold Comparator

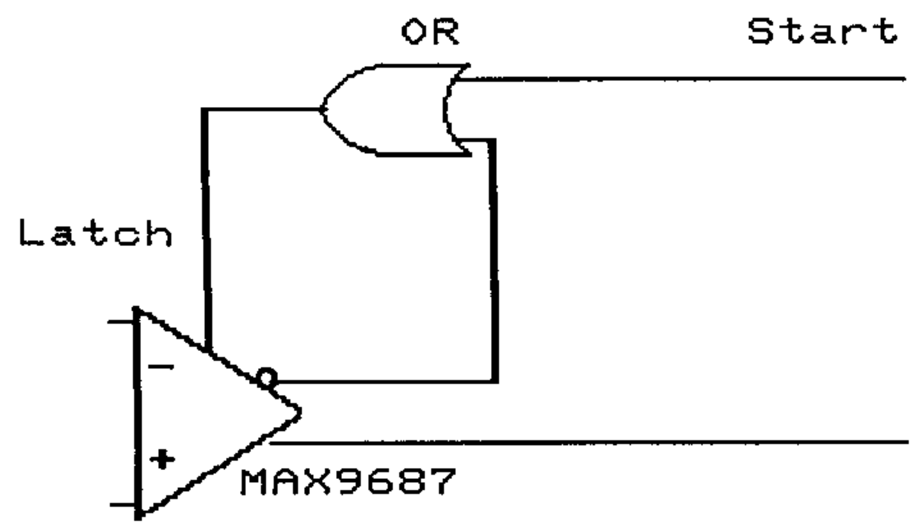


Fig. A - 4 Logic Hold Comparator

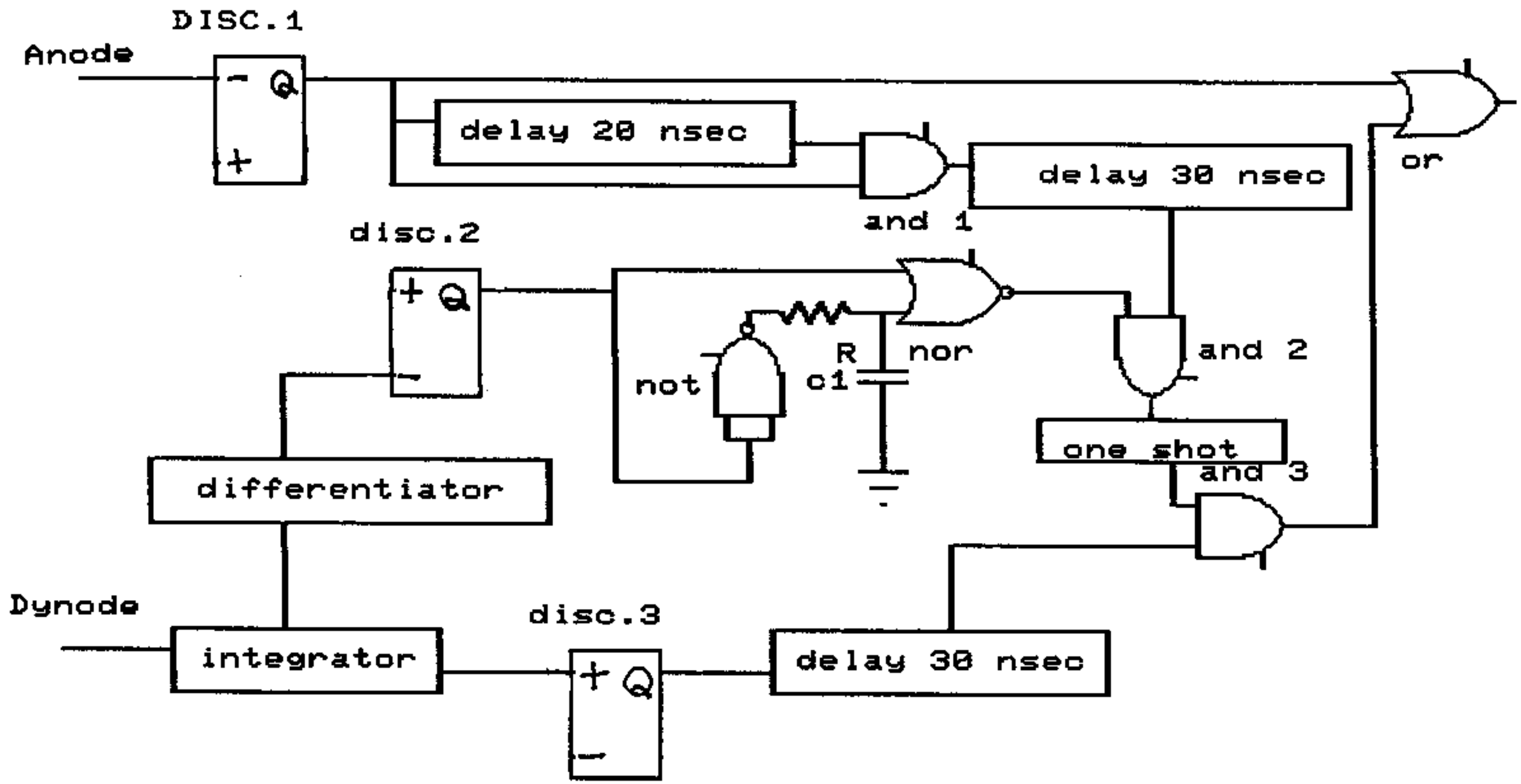


Fig. A - 5 a circuit for the structure “ Type 2 ”