DIR-20-90

Digital Circuit for Optical Module

Toshifumi Aoki (ICRR, Japan)
and
Japan DUMAND Collaboration

Introduction

We have chosen the one-chip microcomputer TMP68301 (Toshiba) as the CPU in OM, taking into account the following requirements :

(1) One of 68000 series, because 68000 will be used in SBC.
(2) low power consumption (CMOS),
(3) compact,
(4) easy to connect external devices.

TMP68301 consists of a core processor 68HC000 (CMOS version of 68000) and peripheral devices around it. Those are three serial I/F's, a parallel I/F, an external bus I/F, timers, an address decoder and so on. The block diagram inside the chip is shown in Fig.1 (in Japanese).

The connections of external devices necessary for OM are considered so as to use the internal devices effectively. In Fig.2, our rough idea is shown. There are still a few unsolved problems, so Fig.2 may not be the final version.

ROM

Since ROM is used only for the bootstrap program when the power is turned on, we do not need much memory. The ROM is located at the zero address only at the time of power-on or reset, and usually located at the rear of RAM in the address space. This can be realized without any extra decoder, by managing the resister in the CS (Chip Select) generator. Fig.4 shows our ROM interface circuit. Only one chip of ROM is enough for our purpose, and then a 8-bit latch is put in front of ROM to make it accessible in unit of word (16-bit).

RAM

A pair of RAM accessible in unit of word is designed, because small package-type SRAM is available which makes a high density mounting possible.

The internal decoder is also used like in the case of ROM. Our RAM interface circuit is shown in Fig.5.

ADC

If we adopt a kind of ADC with serial IO, we can utilize serial ports in 68301 effectively, and can make the ocuppying space on the board smaller. But, a further idea is needed with respect to its interface. The upper one in Fig.6 is a serial ADC.

DAC

The DAC chip we are going to use is made of CMOS and has four channels. It is connected directly to the parallel interface in 68301 and can be easily controled by generating a parallel output of both data and channel assignment signal. The lower one in Fig.6 is DAC.

Modem Circuit

Modem can be connected directly to one of three serial ports in 68301 and its parameters can be set through software. V.Commichau (Aachen) is developing a detailed design using a power line modem NE5050 (Signetics/ Valvo). M.Mignard (Hawaii) seems to have another idea of design. We may be able to follow their results.

Scaler Circuit

Using a 16-bit scaler and a timer inside 68301, the PMT count rate etc. can be measured.

To develope the circuit, we have purchased a personal computer PC9801(NEC), and a few softwares; OrCADs' for drawing the circuit diagram and for designing the print board, a cross assembler and cross compiler for 68000, etc.

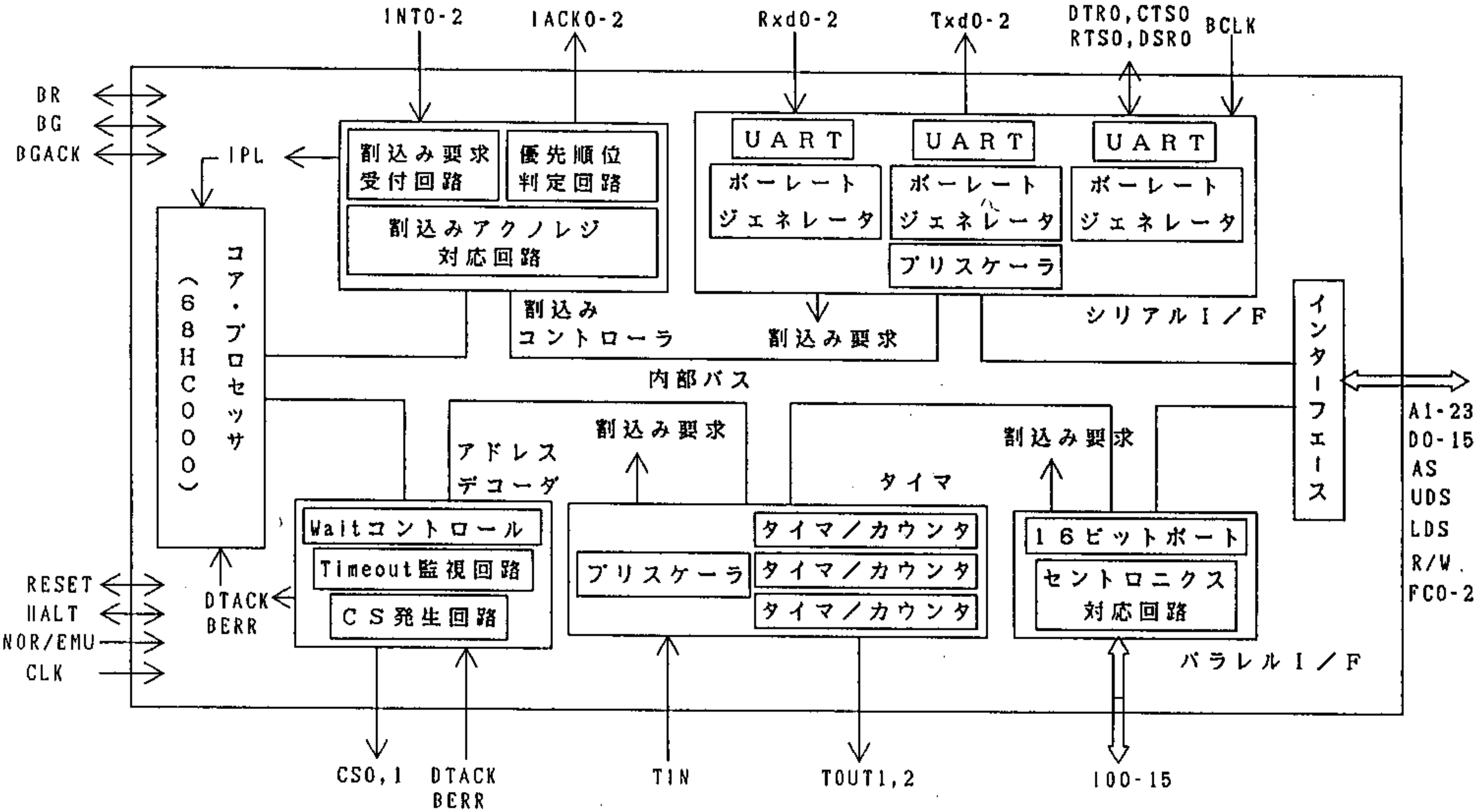
INT0-2
IACK0-2
Rxd0-2
Txd0-2
DTR0,CTS0
RTS0,DSR0
BCLK
BR
BG
BGACK
IPL
割込み要求
受付回路
優先順位
判定回路
割込みアクノレジ
対応回路
割込み
コントローラ
UART
UART
UART
ボーレート
ジェネレータ
ボーレート
ジェネレータ
ボーレート
ジェネレータ
プリスケーラ
割込み要求
シリアルI／F
インターフェース
A1-23
D0-15
AS
UDS
LDS
R/W
FC0-2
コア・プロセッサ
（68HC000）
内部バス
アドレス
デコーダ
割込み要求
タイマ
割込み要求
Waitコントロール
Timeout監視回路
CS発生回路
プリスケーラ
タイマ／カウンタ
タイマ／カウンタ
タイマ／カウンタ
16ビットポート
セントロニクス
対応回路
パラレルI／F
RESET
HALT
NOR/EMU
CLK
DTACK
BERR
CS0,1
DTACK
BERR
TIN
TOUT1,2
I00-15

Fig.1 Block Diagram inside TMP68301

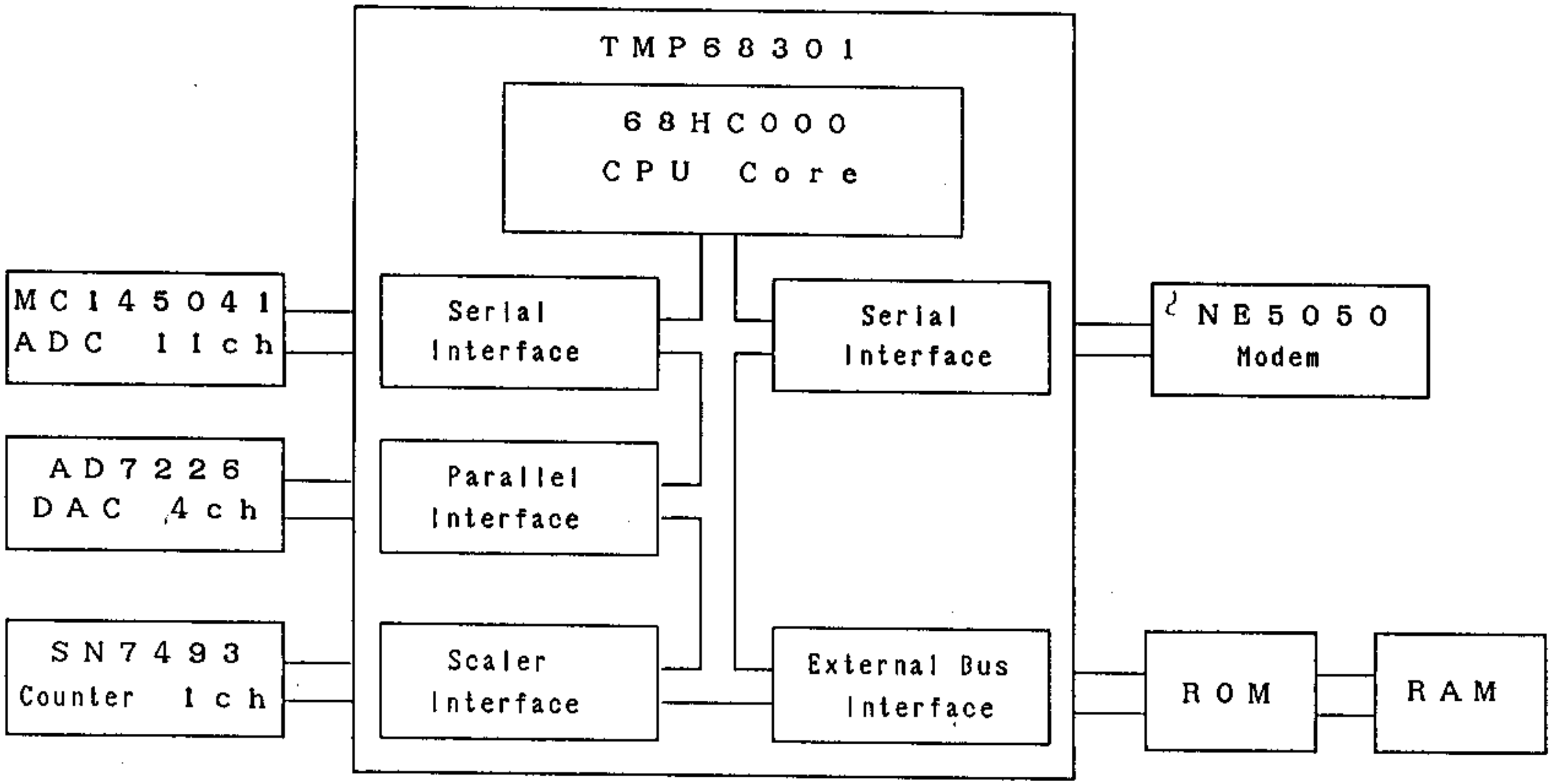
TMP68301
68HC000
CPU Core
Serial Interface
Parallel Interface
Scaler Interface
Serial Interface
External Bus Interface
MC145041
ADC 11ch
AD7226
DAC 4ch
SN7493
Counter 1ch
NE5050
Modem
ROM
RAM

Fig.2 Peripheral Devices for Optical Module

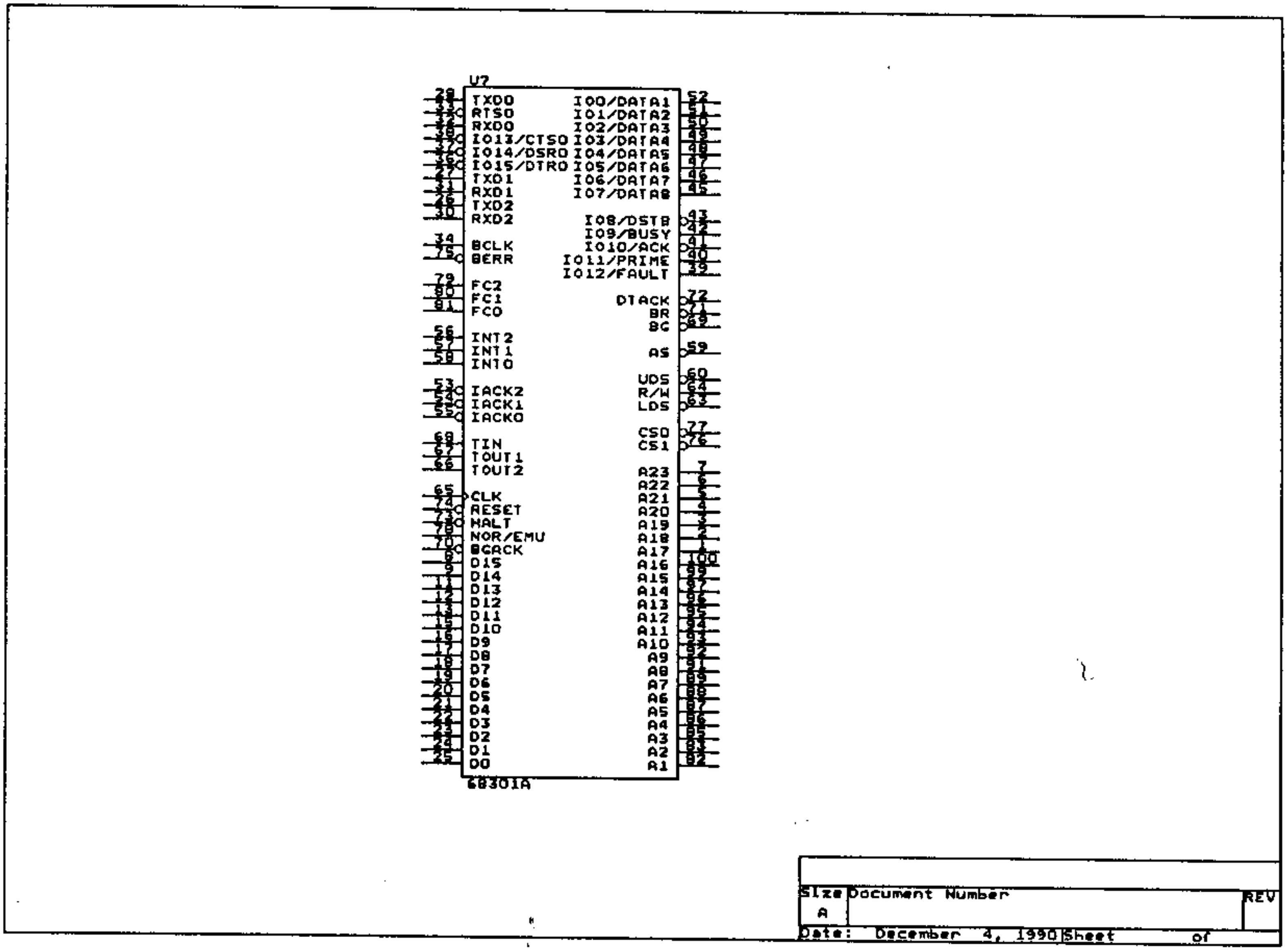
U7
68301A
28 TXD0
RTS0
RXD0
IO13/CTS0
IO14/DSR0
IO15/DTR0
TXD1
RXD1
26 TXD2
30 RXD2
34 BCLK
75 BERR
79 FC2
80 FC1
81 FC0
56 INT2
57 INT1
58 INT0
53 IACK2
54 IACK1
55 IACK0
68 TIN
67 TOUT1
66 TOUT2
65 CLK
74 RESET
73 HALT
78 NOR/EMU
70 BGACK
8 D15
9 D14
11 D13
12 D12
13 D11
15 D10
16 D9
17 D8
18 D7
19 D6
20 D5
21 D4
22 D3
23 D2
24 D1
25 D0
52 IO0/DATA1
51 IO1/DATA2
50 IO2/DATA3
49 IO3/DATA4
48 IO4/DATA5
47 IO5/DATA6
46 IO6/DATA7
45 IO7/DATA8
43 IO8/DSTB
42 IO9/BUSY
41 IO10/ACK
40 IO11/PRIME
39 IO12/FAULT
72 DTACK
71 BR
69 BG
59 AS
60 UDS
64 R/W
63 LDS
77 CS0
76 CS1
7 A23
6 A22
5 A21
4 A20
3 A19
2 A18
1 A17
100 A16
99 A15
97 A14
96 A13
95 A12
94 A11
93 A10
92 A9
91 A8
89 A7
88 A6
87 A5
86 A4
85 A3
83 A2
82 A1
Size
A
Document Number
REV
Date: December 4, 1990
Sheet
of

Fig.3 TMP68301

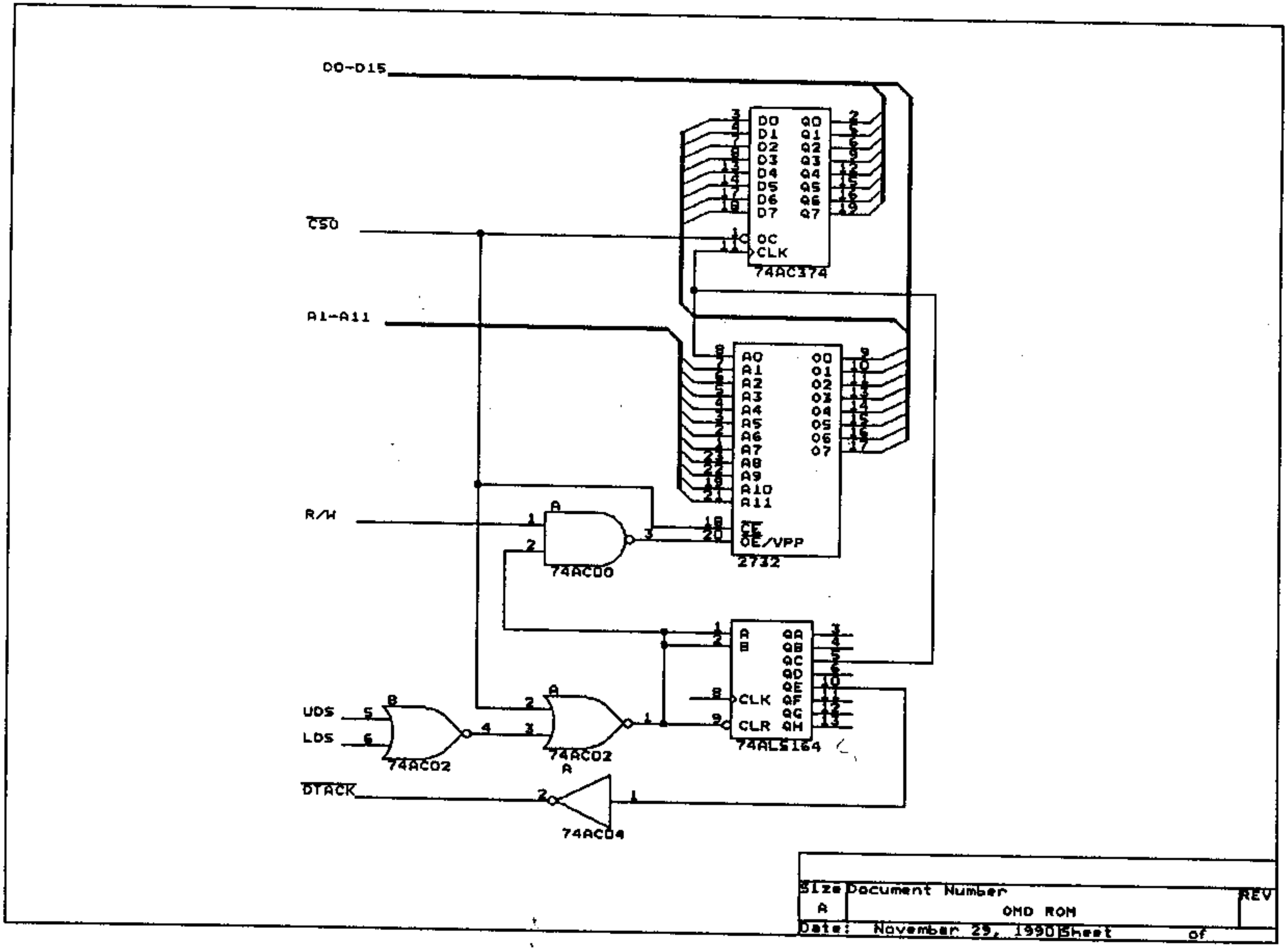
D0-D15
CS0
A1-A11
R/W
UDS
LDS
DTACK
74AC374
D0 D1 D2 D3 D4 D5 D6 D7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
OC
CLK
2732
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11
O0 O1 O2 O3 O4 O5 O6 O7
CE
OE/VPP
74AC00
74AC02
74AC02
74AC04
74ALS164
A B
QA QB QC QD QE QF QG QH
CLK
CLR
Size
A
Document Number
OMD ROM
REV
Date: November 29, 1990
Sheet
of

Fig.4 ROM

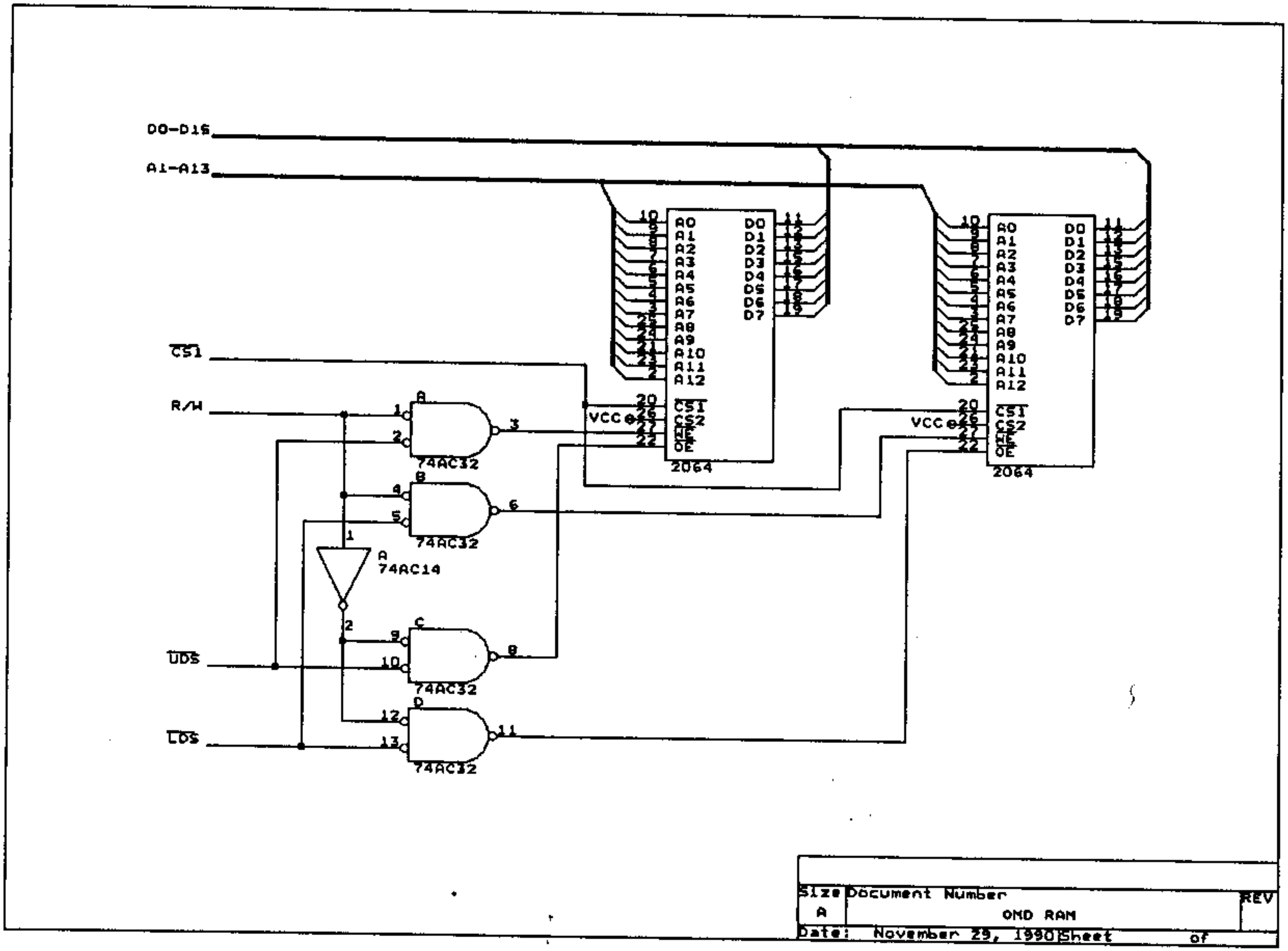
D0-D15
A1-A13
CS1
R/W
UDS
LDS
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
D0
D1
D2
D3
D4
D5
D6
D7
CS1
CS2
WE
OE
VCC
2064
2064
A
B
C
D
74AC32
74AC32
74AC32
74AC32
A
74AC14
Size
A
Document Number
OMD RAM
REV
Date: November 29, 1990
Sheet
of

Fig.5 RAM

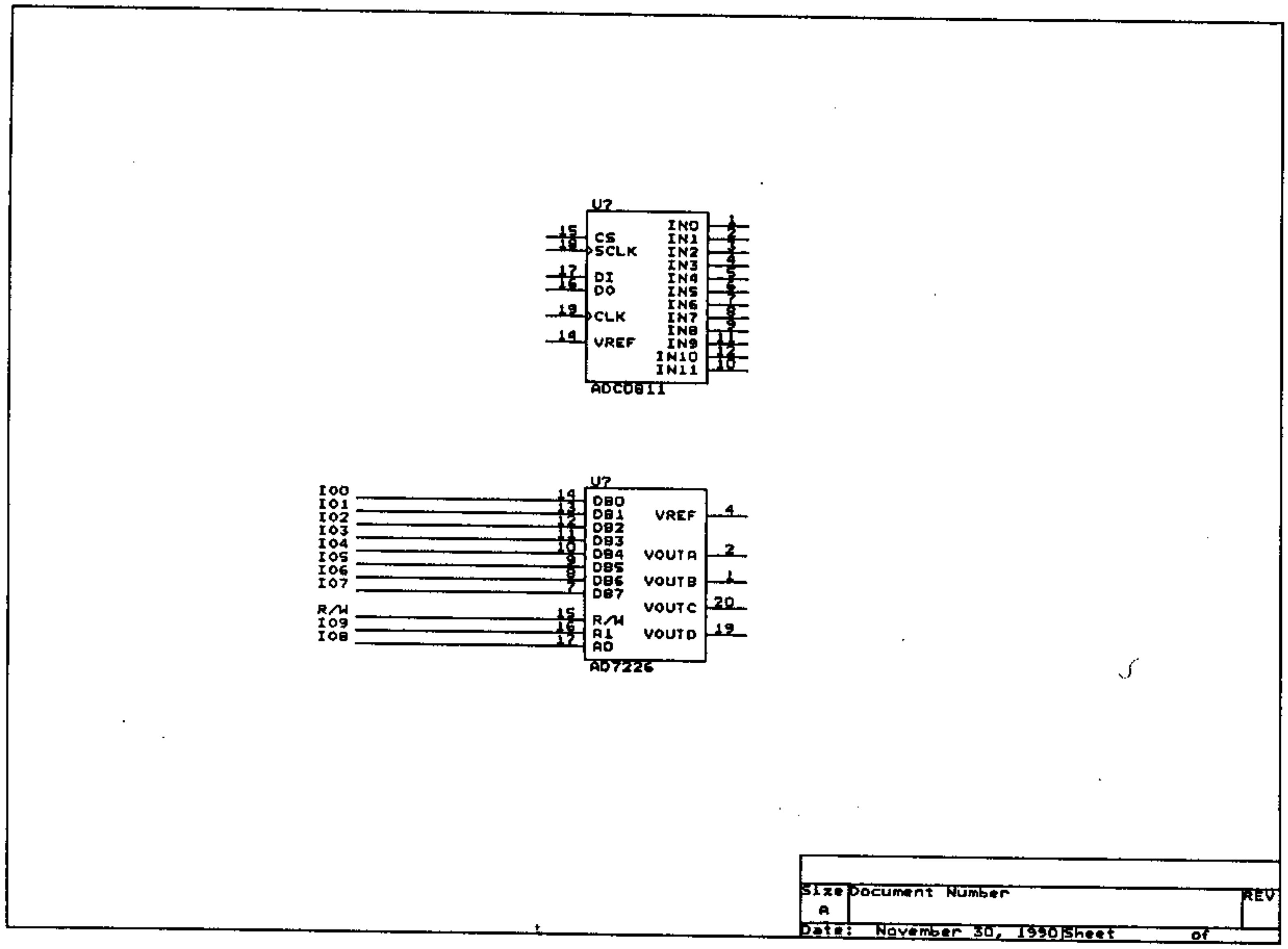
U?
CS
SCLK
DI
DO
CLK
VREF
IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
IN8
IN9
IN10
IN11
ADC0811
15
18
17
16
19
14
1
2
3
4
5
6
7
8
9
11
12
10
U?
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
R/W
A1
A0
VREF
VOUTA
VOUTB
VOUTC
VOUTD
AD7226
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
R/W
IO9
IO8
14
13
12
11
10
9
8
7
15
16
17
4
2
1
20
19
Size
A
Document Number
REV
Date: November 30, 1990
Sheet
of

Fig.6 ADC and DAC