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At the Seattle meeting I heard concern expressed over the fact that an ordinary crystal clock in the SBC digitizer would not be sufficiently stable to permit continued operation if its lock to the CCC link should fail. The proposal offered there was to put a better, e.g. Rubidium, clock in each String Bottom Controller. This will do the job, but I suggest an alternate way which puts the added hardware on shore where it can be repaired.

The idea is not to control the string clock phase drift, but to monitor and correct for it. Then a crystal clock is stable enough. This can be done transparently with a remarkably small amount of added hardware and code in the trigger processor, plus one precaution taken in the SBC.

In the SBC one must only choose the transmitted baud rate of the fast link to be some simple, preferably binary, submultiple of the string clock: 1/2 implying 250 MHz comes to mind. Then the baud rate clock which the on-shore receiver must recover anyway is a string clock signal available in the trigger whenever the link is working at all.

Next one combines this with the onshore phase reference in a circuit which can be viewed as a quadrature lock-in. The circuit can be very simple, using parts of three ICs. The two difference frequency outputs are quadrature square waves which can be handled with the same circuitry and algorithms used for quadrature angle encoders. In particular, you get to count either up or down as appropriate. It is easy to arrange for one count to be worth one cycle phase error of the string clock. (Actually it would be better for it to be 1/2 cycle or less, which is also easy, to eliminate any contribution to quantizing errors.) Further details depend on Matty's choices here, but those two low-frequency signals could be sent directly to the DSP, where he would maintain an up-down counter of accumulated clock phase error in, say, nanoseconds.

First level trigger processing involving only one string would not need any correction. When adding the calibration parameter to ready the data for correlation between strings, the DSP would also subtract the clock error count. That's all it takes.

See Seattle proceedings for a circuit.

Phil Ekstrom 13 Aug 90