DIR-11-90

13 August 1990

Time and Frequency Control in the DUMAND Array

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Abstract

During my two month visit at the UH High Energy Physics department, I was involved in the DUMAND project and especially the possible choices of transmitting time pulses to the array strings and synchronizing them with the main accurate shore station cesium clock. These choices and solutions varied from simple Phase Lock Loops (PLLs) to the use of accurate Rubidium standard oscillators. Finally one of the electrical engineers, David Harris, came up with a PLL device which provided many modes of operation covering the case of single point failure.

Discussion of Possible Solutions

Originally the problem was to synchronize all nine strings of the DUMAND array with pulses of 1GHz; accurate to 1ns; and maintain a relative stability of 10^{-12} short term. After various meetings the limitation of 1ns was relaxed to 2ns or 500-512 MHz. However the down coming cesium clock frequency is not exactly defined, but the most probable operating frequency is 125MHz.

As the main Fiber-Optic cable is coming down a 40Km distance, the time pulses become ill defined, due to inserted noise and losses of the splitter in the Junction Box. Hence we are not sure whether we can recover the signal and drive the S.B.C. clock mechanism accurately. Experimental measurements are to take place in due course, in order to measure the signal distortion along a long fiber with a one to nine splitter at

the end, so we hope that we'll be able to tell whether we can use the signal directly from shore to the array.

Then we examined the case of locking a PLL to the shore clock signal and controlling the loop's drift by a Digital to Analogue Converter at the Loop's Voltage Control Oscillator.

The loop design employs a signal receiver and a Schmidt trigger comparator for recovering our ill defined frequency, and a PLL locked there in order to smooth possible malfunctions. Then using frequency multipliers we can reach 500MHz. In theory this works, but we found out that there was no commercially available VCXO stable enough at 40-100MHz to construct the PLL. Most of the VCXOs coming from the shelf operated at 5-10MHz and also gave a poor stability compared to our requirements. So this solution was discarded.

What followed was an idea of having a pulse generator at the J-box and distributing this pulse along the strings, synchronizing everything according to the new reference pulses. This would employ either an optical repeater or a crystal oscillator as a pulse source and some diodes for transmission.

The problem that appears here is that we must place the mechanism at the J-box, and many people object to any active electronics in the power box, since it makes single point failure more likely.

Then we examined the choice of using Rubidium Standard Oscillators, one for each string, and using the communication lines to synchronize the counters together and also trim their frequencies. Such oscillators are very accurate, reaching short term stability 10^{-12} per sec and long term drift of 10^{-12}/month, which seems very nice for our specs. But after reaching several manufacturers we found out that such oscillators had an average lifetime of 8 years at best, and according to our specs we needed something for at least 10 years: we cannot afford the risk of failure at a probable 6 years. The cost of $36,000 per piece was also very high. Besides that, either the oscillators would have

to be redesigned to fit in the metal tubes or we would need an extra container for every piece. Hence this idea was cast aside as well.

Finally we returned to the PLL solution employing this time a Thermally compensated VCXO, after noticing that such crystal oscillators were compact, relatively stable, and at a much lower cost.

The design chosen (see diagram) is a multimode operating mechanism, which provides safety in terms of single mode failure. Actually it has three modes of operation, reaching finally 500MHz.

We receive the main cesium signal from shore and feed it into a Schmidt trigger at a frequency of 125MHz. The signal is cleared there in terms of noise and is then fed into the phase detector of a PLL. If the signal is strong enough it is fed directly to the time digitizer and the output.

The other modes of operation are using a PLL which is based on a CTS JKSC-142 Thermal compensated VCXO. This TXVCXO approaches our requirements. It uses a precision over-tone SC-cut crystal along with custom designed double oven results in exceptional stability performance overtime and temperature. Its output frequency is 5.0MHz, and dc input requirements are +15Vdc and +5Vdc. Typical power input, at 15V and 5V are: at turn on 9W and 0.18W and at +35 degrees C 3W and 0.18W respectively. The range of operation is 0^{o}C to $+60^{o}$C. During warm-up ($+25^{o}$C) stability is 10^{-10} in 25 min from frequency at 1 hour. Stability; 10^{-7} for 20 years without adjustment or after stabilization$\pm$ 10^{-10} per day with any 15^{o}C ambient temperature change and a 0.3% input voltage change. Finally its size suits the tube's dimensions 4.5"*3.25"*3.5"H, and the lifetime is more than 250,000 hours.

Taking all these specs and bearing in mind that we can have a voltage controller DAC at the i/p of the TXVCXO we think that its stability can be improved. Hence with a DAC fine adjustments and small corrections can be made, observed by an A/D converter at the oscillator's i/p. The purpose of the resistors and capacitor is to

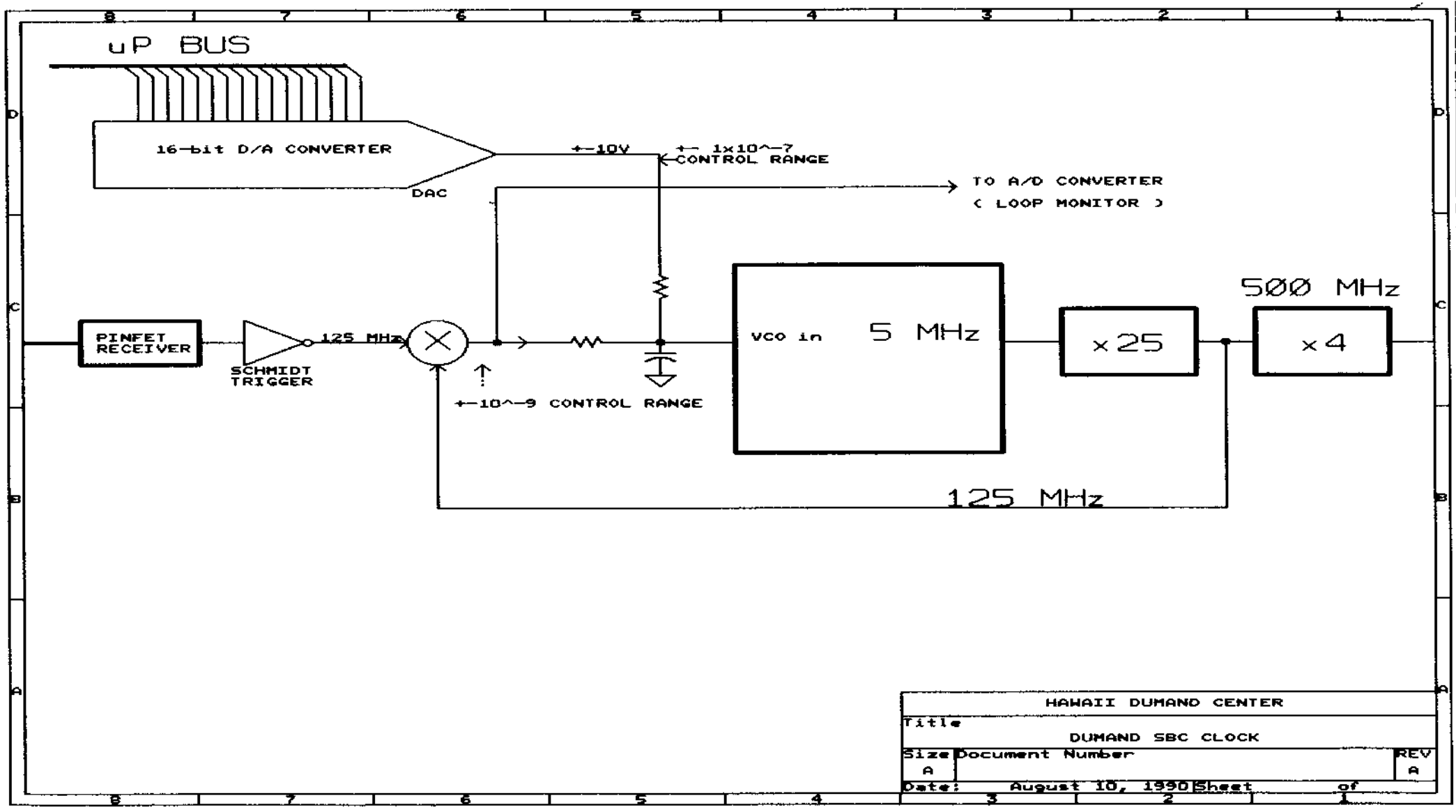
stabilize the PLL locking oscillations around the frequency lock point. This is due to the added impedance of the above extra components.

The 5MHz signal is then multiplied 25 times to reach a frequency of 125MHz, which is fed back to the phase detector and close the loop. This 125MHz is also used for time digitizing the up going data. And finally the PLL output is multiplied by four to reach the 500MHz, or clock frequency.

Finally in case we are unable to use the down going signal due to any kind of failure, we can run the system just by the TXVCXO and the step-up multipliers keeping the control with the input voltage fed by the DAC to the oscillator.

The only thing that remains to be explored is whether there are crystal multipliers of times 4 and 25 commercially available. So if we get around this problem, the next step is to construct the whole design and test it for some time, so that we can be confident about its operation and behavior.

In conclusion, I believe that we need to work more carefully on this problem because every day one sees more and more new products which may make the problem easier to solve. So, plans might probably change in future.


uP BUS
16-bit D/A CONVERTER
DAC
+-10V
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CONTROL RANGE
TO A/D CONVERTER
(LOOP MONITOR)
PINFET
RECEIVER
SCHMIDT
TRIGGER
125 MHz
+-10^-9 CONTROL RANGE
vco in
5 MHz
x25
x4
500 MHz
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