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Curtis W. Ward
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Radiation Damage in CLEO II.5 and CLEO III Silicon and Readout Electronics

Abstract

In this document the CESR/CLEO II.5 radiation environment and radiation damage mechanisms in semiconductor devices are discussed. The radiation tolerance of the CLEO II.5 silicon vertex detector and readout electronics is presented along with methods which have been used to improve the radiation resistance of the CLEO III silicon detector and electronics.

1 Introduction

The CLEO detector at the Cornell Electron Storage Ring (CESR) recently underwent an upgrade which included the installation of a silicon vertex detector (CLEO II.5). Several improvements were also made to the accelerator in an effort to improve the ring's luminosity. Unfortunately, the addition of the CMOS readout electronics for the silicon, in close proximity to the interaction region, placed stringent limits on background radiation levels. Initially there was concern about radiation dose rates since they were quite high during startup. Much effort was spent improving the background radiation levels during both injection and colliding beam operation and these levels have improved dramatically. For 1998 another upgrade (CLEO III) to both the detector and the accelerator is planned. The detector upgrade will include the installation of a new silicon vertex detector, drift chamber, and particle identification system (Ring Imaging Cherenkov Detector). Increases to the accelerator's luminosity as well as the addition of a large amount of electronics in the detector will make background radiation a concern once again. In order for the upgrade to be successful, considerable attention must be paid to the radiation sensitivity of the detector electronics.

2 Background Radiation in CESR

In addition to the products of colliding beams, a variety of background radiation is produced in an e^+e^- collider. Several processes produce photon radiation. First, copious amounts of synchrotron radiation is created as the orbits of the electrons and positrons are bent by transverse magnetic fields. In CESR, operating at a beam energy of 5.3 GeV, the synchrotron photon spectrum extends from about 4 to 20 keV, although harmonics are produced out to much higher energies. Second, as the beams approach each other at the interaction point (IP) they can emit high energy bremsstrahlung photons (beamsstrahlung). These photons can also be produced during scattering with beam gas particles. Particle backgrounds are produced by various processes. Certainly the scattering of orbit electrons with residual gas in the IP beampipe will produce particle radiation. In addition, scattering in other regions of the accelerator will cause orbit particles to lose energy. These particles will then be over-focussed by the magnets near the interaction region (IR), causing them to shine into the detector.

Table 1 shows the contribution of background radiation from various regions in CESR [1]. The relative contributions from synchrotron radiation (all sources) and particle backgrounds created from beam gas events in the intermediate straight pipe (ISP), soft bend, 1/4 normal bend, and hard bend regions are indicated. A significant portion of the dose comes from the hard bend regions which are 15–35 meters from the IP. The backgrounds created by scattering in the rest of the lattice has been found to be negligible. These values were experimentally determined by monitoring background radiation levels at the IP, using silicon diode radiation monitors, as a function of the pressure in each pipe and the beam current. The contributions from each element were then scaled to a uniform pressure. The synchrotron dose is expected to scale linearly with beam current while the particle dose should scale quadratically with beam current. The quadratic nature is the result of the beam pipe pressure rising linearly with sychrotron radiation load and hence, with the beam current. The beam gas scattering probability is proportional to the product of beam current and pipe pressure. Note that Table 1 shows that the synchrotron radiation component of the total background radiation is small. This is due to careful control of the beam orbit in the IR and the addition of tungsten masks in the beampipe adjacent to the IR. The relative synchrotron contribution to the dose is expected to be even smaller at higher beam currents. Currently the dose rate during high energy physics (HEP) operation (including HEP injection) is 1.7 Rads(Si)/hour at 100 mA per beam. Neutrons comprise only 1–2% of this dose.

In addition to normal luminosity running conditions, several mechanisms produce high radiation dose rate bursts. These include injection, ion trapping and beam dumps. Table 2 shows the experimentally determined time and dose fractions from the mechanisms mentioned above. Sudden, short rises in the radiation dose rate during luminosity running are called bump events. They are probably a result of localized ion trapping or pressure bursts. In spite of the high dose rates produced by the above processes, they occur rarely and hence, contribute little to the total background radiation dose. Injection does not contribute significantly more to the radiation dose than one would estimate based solely on its time fraction.

Table 1: Sources of background radiation in CESR (100 mA/beam) [1].

Region	Background Contribution
Synchrotron	8%
ISP	30%
Soft Bend	35%
1/4 Normal	0%
Hard Bend	27%

Table 2: High dose rate processes and their contribution to total background radiation.

Process	Time Fraction	Dose Fraction
Ion Trapping	1.7%	4.0%
Injection	15%	20%
Beam Dumps	.10%	1.1%
Bump Events	3.0%	9.0%

3 Damage in Semiconductors

The interaction processes of radiation with solids result in two types of damage in semiconductor devices. Photons and charged particles both cause ionization of the lattice atoms, while neutrons and heavy charged particles cause displacement of atoms in the lattice. Ionization radiation effects are usually transient in semiconductor materials but can cause permanent damage in insulators. Displacement damage is usually permanent. Ionization damage is the primary concern in the CESR environment. We will treat damage to semiconductor materials by ionization and displacement separately.

3.1 Ionization Damage

The average energy required to eject an electron from the valence band is typically several times that of the bandgap. Table 3 lists bandgap energies, average ionization energies, and density of generated electron-hole pairs per Rad for common semiconductor and insulating materials [3]. These ionization energies are independent of temperature [2]. Immediately after ionization occurs a process called thermalization takes place in the lattice. Here the excess kinetic energy of the electron is removed by scattering with the lattice and the energy of the ejected electron is reduced to the conduction band edge. Thermalization takes place quite rapidly – typical time constants are on the order of 10^{-12} sec. The conduction electron and valence band hole are free to drift in the presence of electric fields, recombine, or be trapped at a defect site. This radiation induced photocurrent can itself cause problems in semiconductor devices. For example, in memory or digital logic ciruits errors or data loss can occur. These currents also cause background occupancy in silicon detectors. Table 4 shows the measured and simulated occupancy from background radiation for CLEO II.5 and the predicted CLEO III occupancy. The results have been scaled for the shaping times used in CLEO II.5/III readout electronics and are for the beam currents indicated. Radiation induced currents, while troublesome, generally do not lead to permanent device damage or failure. One notable exception to this is SCR latchup caused by these induced currents which can cause thermal failure of the device due to large power supply current draw.

Photocurrents are usually less disturbing in insulating (such as SiO_2 and Si_3N_4) materials due to the lower carrier mobilities (and subsequent higher recombination rates). However, insulating materials have a much higher density of trapping centers. Carriers produced by ionization can be trapped at these sites for long time periods. Table 5 shows the electron and hole mobilities for various materials [2, 4]. Charge trapped in the gate oxide of MOS devices causes permanent voltage threshold shifts and changes in operating points which can lead to device failure. In addition, charge trapped in the field or passivation oxide can cause parasitic leakage currents between adjacent devices on the same substrate. These effects are more severe for smaller

Table 3: Electron-hole pair generation energies, bandgap energies, and pair densities per Rad for common semiconductor materials [3].

Material	Pair generation energy $E_p(eV)$	Bandgap $E_g(eV)$	Pair density per Rad $g(pairs/cm^3)$
Silicon	3.6	1.12	4.0×10^{13}
Silicon Dioxide	17	8.8	8.1×10^{12}
Gallium Arsenide	4.8	1.43	7×10^{13}
Germanium	2.8	.803	1.2×10^{14}

Table 4: Background occupancy for CLEO II.5 and III silicon detectors.

Detector	Simulation	Measured
CLEO II.5	.29% (300 mA/beam)	.18% (150 mA/beam)
CLEO III	.26% (500 mA/beam)	

device geometries and higher integration densities. They will be treated in detail in the section on MOS devices.

3.2 Displacement Damage

The displacement of a single lattice atom causes two defects in the lattice; a vacancy in the original location of the scattered nucleus and the creation of an interstitial location in the lattice where the knock on atom comes to rest. These simple defects alter the periodicity of the lattice and result in the formation of discrete energy levels

Table 5: Electron and hole mobilities for various semiconductor materials [2, 4].

Material	Electron mobility $\mu_e(cm^2/V \cdot sec)$	Hole mobility $\mu_h(cm^2/V \cdot sec)$
Germanium	3900	1900
Silicon	1500	600
Silicon Dioxide	20	2×10^{-5}
Gallium Arsenide	8500	400

in the bandgap. High energy neutrons can produce cluster defects. Here the location of the valence and conduction band edges are locally modified. This modification creates a potential well trap for carriers. Protons, which stop at the end of their range, can cause cluster defects as well. Simple defects are relatively mobile and can recombine at room temperature. However, divacancies and cluster defects are immobile and do not anneal at low temperatures.

The formation of states within the bandgap leads to several effects. First, levels created near the center of the gap serve as sources of thermally generated carriers. This increases leakage currents of reverse biased junctions. Second, these states act as recombination centers and result in reduced minority carrier lifetimes. Since bipolar transistor gain is roughly proportional to the minority carrier lifetime over the base transit time, transistor gain is decreased by displacement damage. Transistor switching speed is also degraded. Radiation hard bipolar transistors are constructed using narrow base regions in a effort to keep base transit time low. The bandgap states also act as scattering centers, reducing carrier mobilities. This increases the collector resistance of bipolar transistors (increasing V_{sat}) and the channel resistance of FET devices (increasing R_{DSon}). Deep traps in the bandgap act as sites which compensate donors, reducing the carrier concentrations. This also leads to an increase in channel and collector resistivity and causes voltage threshold shifts in FETs. Finally, these traps facilitate tunneling currents by allowing tunneling to procede by an intermediate state. Junction leakage is increased as a result of this tunneling current.

Typically bipolar devices are most sensitive to displacement damage since minority carriers are dramatically affected by bandgap traps. Neutron fluences (number of neutrons passing a unit area) of 10^{13} n/cm^2 cause significant gain reductions in non hardened bipolar devices [3]. However, FET (majority carrier) devices can withstand fluences of 10^{14} n/cm^2 without significant degradation [5].

4 MOS Devices

The predominate technology used in very large scale integration (VLSI) electronics today are the complementary metal oxide semiconductor (CMOS) devices. These devices have excellent speed, are easily manufactured, and have low power consumption. However, they are relatively sensitive to damage from ionizing radiation. This sensitivity is due to the use of oxide in the critical gate region of the transistors. The consequences of damage to the insulating gate are discussed here.

Typical n-channel and p-channel enhancement mode MOSFETs are shown in Figure 1. The bias configurations for conducting (on) devices are indicated. Applying a gate voltage creates an electric field in the gate oxide and causes an inversion layer to form in the channel (provided $V_G > V_T$). It is this inversion layer which supplies the carriers for current flow between the source and drain. The threshold voltage

(V_T) for an n-channel (p-bulk) MOS device is given by Equations 1 and 2.

$$V_T = 2\phi_F + \frac{K_s d_{ox}}{K_{ox}} \sqrt{\frac{4qN\phi_F}{K_s \epsilon_0}} \tag{1}$$

$$\phi_F = \frac{kT}{q} \ln(\frac{N}{n_i}) \tag{2}$$

In Equation 1, d_{ox} is the oxide thickness, K_s and K_{ox} are the semiconductor and oxide dielectric constants, and N is the acceptor doping density. The intrinsic semiconductor carrier concentration (n_i) which is used in Equation 2 is equal to $1.2 \times 10^{10} cm^{-3}$ for silicon at 300 K. The threshold voltage for p-channel (n-bulk) devices is given by Equation 1 with the sign of the second term reversed and N equal to the donor doping density. For high speed, low voltage devices small voltage thresholds are desirable and this requires thin gate oxides. However, low gate capacitance, $C_{ox} \propto 1/d_{ox}$, is also required for fast switching speed, making very thin oxides also unpalitable.

When these devices are exposed to ionizing radiation four processes occur in the oxide:

1. Electron-hole pairs are generated in the oxide and the electrons are swept out of the gate by the electric field.
2. Holes begin transport throughout the oxide, migrating toward the $Si - SiO_2$ interface.
3. Deep hole trapping near the interface occurs.
4. Interface traps are formed in the Si bandgap.

The result of positive charge captured in the oxide is shown schematically in Figure 2. The trapped charge causes a lowering of the voltage thresholds for n-channel devices and an increase in p-channel threshold voltages. The threshold voltage shift caused by radiation can be divided into three parts as indicated in Equation 3.

$$\Delta V_T = \frac{qN_h}{C_{ox}} + \frac{q\Delta N_{ot}}{C_{ox}} + \frac{q\Delta N_{it}}{C_{ox}} \tag{3}$$

The oxide capacitance per unit gate area is given by

$$C_{ox} = \frac{K_{ox}\epsilon_o}{d_{ox}}, \tag{4}$$

where N_h is the free hole density created by the radiation, ΔN_{ot} is the density change of holes in deep oxide traps, and ΔN_{it} is the density change of interface trapped charge. Within picoseconds after the production of electron–hole pairs the electrons are swept out of the oxide by the electric field. Recombination also takes place during this time. Typical thermalization distances are 8 nm, so recombination is highest for radiation which produces pairs with small average separations (e.g. photons and protons). High energy electrons produce pairs at an average distance of 50 nm and the recombination rate is quite low [3]. If the fraction of holes which survive recombination is taken to be f then the first term of Equation 3 can be written as

$$\Delta V_T = \frac{qgd_{ox}fD}{2C_{ox}}. \tag{5}$$

In Equation 5, D is the dose in Rads(SiO_2). Note that the initial threshold voltage shift rises as the square of the oxide thickness.

At temperatures above 140 K hole transport is thermally activated and is thought to occur by two methods. The most important method is trap hopping. In this process holes tunnel between traps located within the bandgap of the oxide. The other process is valence band conduction modulated by bandgap traps. Here the transport occurs in the valence band but thermal fluctuations cause the holes to get stuck in the bandgap. The release time from traps is known to vary considerably and this accounts for the long time constants associated with annealing due to transport. Experimentally the recovery of irradiated MOS devices due to hole transport has been found to have a time dependence given by Equation 6 [3].

$$t_{recovery} \propto d_{ox}^4 \exp \frac{\Delta E_{ox}}{kT} \tag{6}$$

In Equation 6, ΔE_{ox} is an electric field dependent activation energy experimentally determined to be about 0.6 eV for typical electric fields. For a 100 nm thick oxide with a 1 MV/cm electric field the room temperature half recovery time is $\sim 3 \times 10^{-4}$ sec [3]. The strong dependence on oxide thickness underscores the immobility of the holes as well as the need for thin oxides in radiation tolerant devices.

As the holes come to within 10 nm of the $Si - SiO_2$ interface they can be trapped in deep states within the oxide bandgap. Deep trapping is often the dominant oxide damage mechanism and is responsible for long term voltage shifts. Holes trapped in these states can survive for hours to years before they are released. The traps are the result of an insufficient number of oxygen atoms at the silicon–oxide interface which leads to formation of strained Si–Si bonds instead of the preferred Si–O–Si bonds. These strained bonds can be broken by incoming holes which then recombine with an orbital electron, leaving a net positive charge at the interface. Once the holes are captured by these traps they can only be removed by tunneling to the Si valence band or by recombination with electrons produced by ionizing radiation. The latter method usually results in a saturation of holes trapped at deep sites at 1–10 MRad [3]. Thermally assisted tunneling is responsible for the logarithmic time dependence of the annealing process. In addition to voltage shifts, these deep traps introduce additional scattering centers in the channel which reduce carrier mobilities and increase the $1/f$ noise component. This mobility degradation results in reduced device speed and increased device noise. However, these effects are usually secondary when compared to the voltage shifts caused by deep traps. The threshold shift caused by deep traps is proportional to the density of deep traps and this is strongly dependent on the processing of the oxide. Radiation hard oxides are produced using steam instead of dry O_2 during growth and by eliminating high temperature (> 900 C) annealing operations after formation of the gate oxide [3]. Very thin oxides are also less likely to have deep traps due to more complete interface oxidation. The number of deep oxide traps is also dependent on the silicon crystal orientation. The ratio of trap densities for $< 111 >$ to $< 100 >$ orientations is approximately 3:1 [6]. It is for this reason that MOS devices are almost exclusively formed on $< 100 >$ silicon.

The fourth result of hole creation in the oxide of a semiconductor device is the formation of radiation induced interface traps in the silicon bandgap. These interface traps can affect device operation in several ways. The first effect is a simple voltage threshold shift due to the trapped charge as mentioned above. Second, these traps introduce coulomb scattering centers and reduce carrier mobilities in the channel of MOSFETs. Third, they produce distortions in the capacitance–voltage and current–voltage characteristics of the device. The distortions are caused by the voltage dependence of the unfilled trap density as shown in Figure 3. In the figure, the conduction and valence band edges are shown for three gate voltage bias configurations. During inversion all interface traps are empty and can contribute to the two effects just mentioned. However, as the voltage is changed toward accumulation, these traps are filled by valence band states and do not contibute to the voltage threshold shift. The result can be seen in Figure 4 which shows the capacitance versus gate voltage for a n-bulk MOS capacitor after exposure to various doses of 20 keV synchrotron radiation [7]. Note that in addition to an overall threshold voltage shift as a result of deeply trapped holes, the slope of the C–V curve is reduced in the transition region indicating an increase in interface traps.

Small radiation induced threshold voltage shifts cause a slight reduction in speed and noise immunity. However, large shifts can cause n-channel devices to be permanently turned on or p-channel devices permanently turned off resulting in circuit failure. For the p-channel devices, the direction of the electric field causes the holes to be attracted to the gate metal (or polysilicon) where there are no interface deep hole traps. Thus, for a given dose on similarly constructed n and p-channel devices the p-channel voltage shifts are generally smaller. The result is that p-channel devices are more radiation tolerant. Of course, removing the electric field (circuit off) improves the hole recombination efficiency which significantly reduces the number of free holes for a given dose. This can lead to a large increase in radiation tolerance. For example, the CMOS preamplifiers used in the CLEO II.5 silicon vertex detector can withstand 4 times the radiation dose before failure if the devices are unpowered during irradiation [9]. This led us to the decision of leaving the electronics off during injection and machine studies when no data is being taken.

It should be noted from Figure 2 that trapped holes also accumulate in the field and passivation oxides between adjacent devices on the same substrate. If the threshold voltage shifts from this trapped charge are high enough, the n-channel parasitic transistor between two devices can be turned on, causing an increase in leakage and power supply currents. Note that for p-channel devices the threshold shift is in the cutoff direction and this failure does not occur. This is another reason for the improved radiation tolerance of p-channel devices. Due to the thickness of the field oxide, the threshold voltages are high (typically 15 V) but the threshold shift is more rapid in a thick layer of oxide (see Equation 5). The effects of radiation induced parasitic leakage currents are not confined to MOS devices. They affect any silicon device which has SiO_2 passivation including diodes, JFETs, and bipolar devices. This is the principle mechanism for damage in silicon vertex detector wafers exposed to ionizing radiation [7]. In these devices, radiation induced strip leakage currents are problematic because the increase in shot noise reduces the signal to noise ratio (SNR) of the detector.

5 Rad Hard Devices for CLEO III

5.1 Readout Electronics

The hardening of CMOS devices to the effects of radiation requires improving the circuit's tolerance to threshold shifts and use of a hardened oxide which has a lower hole trapping efficiency and fewer deep interface traps. Thin gate oxides are used to reduce the slope of the threshold voltage change with radiation dose. SCR latchup is prevented by forming transistors in a lightly doped epitaxial layer grown over a conductive substrate (to reduce voltage drop from radiation induced leakage currents) or by using an insulating substrate to isolate FETs and eliminate parasitic bipolars. Parasitic leakage currents are significantly reduced by the addition of a p-type guard ring between adjacent n-channel transistors. The region above the highly doped guard ring has a large threshold voltage (80–100V) which prevents parasitic transistor action even after large doses of ionizing radiation. The hardening process requires changes in the device layout and processing which can lead to significant increases in cost. Compromises in device perfromance such as speed, packing density, and noise performance often need to be made in order to meet a specific radiation tolerance.

A comparison of the radiation tolerance of the readout electronics for the CLEO II.5 and the proposed CLEO III silicon detectors is shown in Table 6. Indicated in the table are the measured lethal dosage for powered and unpowered CAMEX and JAMEX amplifiers as well as the expected lethal dose for the CLEO III chipset. Here we define lethal dose as the point when the average chip gain drops by 50% or when digital (multiplexer) failure occurs. Measurements on the CLEO II.5 electronics was performed using a 20 keV monochromatic X-ray beam at CHESS [9, 10]. It was observed that the noise performance of the CAMEX ICs degrades by 20% as the chips near the lethal dose.

The CAMEX 64 channel preamplifiers use conventional rad-soft CMOS technol-

Table 6: Radiation tolerance of CLEO II.5 and CLEO III readout electronics [9].

Device	Powered kRad (Si)	Unpowered kRad (Si)
CAMEX	25	100
JAMEX	170	~ 200
CLEO III	1000	2000

ogy. The JAMEX preamplifiers which were selected for use in layer 3 for their improved noise performance have the added benefit of being rad-firm. Their radiation tolerance results from the use of n-channel JFETs and p-channel MOSFETs as complementary devices on the same substrate. Since JFETs do not use oxide in the critical gate region of the device they are inherently radiation tolerant. Utilizing complementary JFETs and MOSFETs results in a rad-firm device without the cost associated with a rad-hard CMOS process [8].

The CLEO III preamplifier and readout ADC, which are being fabricated by Honeywell Corporation (Solid State Electronics Center, Minneapolis, MN 55441), owe their radiation tolerance to the use of hard gate oxides and guard rings, and to a design which allows critical voltages to be adjusted externally. This allows radiation induced voltage shifts to be accommodated by adjustment of these voltages as needed. A test of this design philosophy was performed on a rad-soft version of the preamplifier IC. After 34 kRad (Si) of 20 keV X-ray irradiation, gain remained constant (after tuning) and noise performance was degraded by less than 20%. The threshold voltage shifts observed during the test are the same as the maximum voltage shift of the rad-hard device after 1 MRad of exposure. Thus, the circuit design has been properly optimized to accomodate radiation induced threshold voltage shifts.

5.2 Detectors

It was mentioned in section 4 that ionization damage to passivation oxide in silicon detector wafers results in increased leakage current. Due to the detector design and noise performance of the CLEO II.5 detector it is unlikely that we will see additional noise from radiation induced leakage current during its operating life. However, this is not the case for the CLEO III detector and noise caused by detector leakage currents could be significant. Therefore, careful attention has been paid to the detector design and its relation to radiation tolerance. The damage constant of prototype detectors has been found to be 5nA/cm^{2}kRad [7], independent of bias. This would imply that noise due to radiation induced leakage currents would become dominant at 100 kRad (Si). However, due to the initial SNR performance of the system the detectors would be useable after at least 300 kRad. After discussion with the manufacturer of the detectors (Hamamatsu Photonics), the processing was changed and tests on prototype production detectors give damage constants half as large as indicated above. Simulations predict that the layer 1 silicon detector would receive 18 kRad(Si)/year at 500 mA/beam (includes HEP, injection, and machine studies) in the CLEO III environment. Simulations predict the dose rate to be proportional to $1/r^{1.8}$ which indicates that only layers 1 and 2 (which have the best initial SNR) will show significant noise increases from radiation damage.

6 Conclusion

It has been shown how the effects of ionizing radiation on CMOS devices can be detrimental to device performance. In the e^+e^- collider environment both synchrotron and charged particle radiation sources exist. However, the type of ionizing radiation is of little consequence to CMOS devices and detectors since the oxide damage mechanisms do not depend on the process by which the electron-hole pairs are generated. This is important since the changes in the accelerator lattice for Phase III operation could drastically alter the relative background contributions indicated in Table 1. In particular, the use of round beams would significantly increase the synchrotron radiation component. Factors which do affect the lethal dose are the dose rate, construction of the device and quality of the oxide, and whether the device is powered during the irradiation.

Due to the expected dose received by the silicon readout electronics in the CLEO III detector we have concluded that the readout chips should be constructed in a rad-hard technology. The current chip design allows us to compensate for threshold voltage changes. The result will be a factor of > 10 improvement in tolerance to both synchrotron and particle radiation as compared to CLEO II.5. While neutron radiation levels are expected to be low during CLEO III operation, CMOS electronics are inherently tolerant of displacement damage. All of these factors will make the lethal dose large compared with the expected absorbed dose during the life of the detector. Hopefully, a high radiation tolerance will allow a smoother accelerator startup and reduce the time to reach the goal luminosity.

7 Acknowledgements

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References

[1] D. Cinabro, presented at the CLEO plenary meeting, April 13, 1996. See summary in CBX 96–28.

[2] V.A.J. van Lint, et al., *Mechanisms of Radiation Effects in Electronic Materials.* John Wiley and Sons, 1980.

[3] W.R. Dawes, et al., *Hardening Semiconductor Components Against Radiation and Temperature.* Noyes Data Corporation, 1989.

[4] *Radiation Damage in Semiconductors.* Harris Semiconductor Corporation, 1984.

[5] D.L. Hartill, IEEE Trans. Nucl. Sci. **33** (1986).

[6] R. F. Pierret, *Field Effect Devices.* Addison-Wesley Publishing Corporation, 1990.

[7] A.D. Foland, et al., IEEE Trans. Nucl. Sci. **43** (1996).

[8] G. Lutz, et al., Nucl. Inst. Meth. **A264** (1988) 391.

[9] C. Ward, presented at the CLEO plenary meeting, February 10, 1996. See summary in CBX 96–10.

[10] J.P. Alexander, et al., Nucl. Inst. Meth. **A337** (1993) 171.

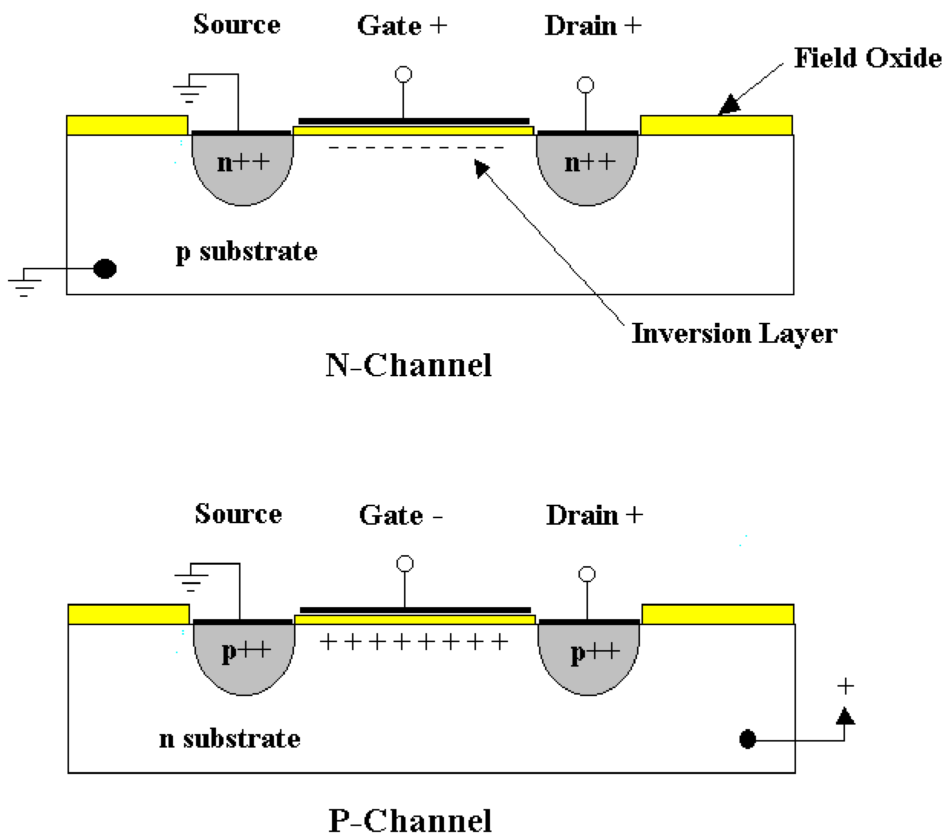

Figure 1: Construction and biasing of n and p-channel MOS transistors. The location of the field oxide is shown.

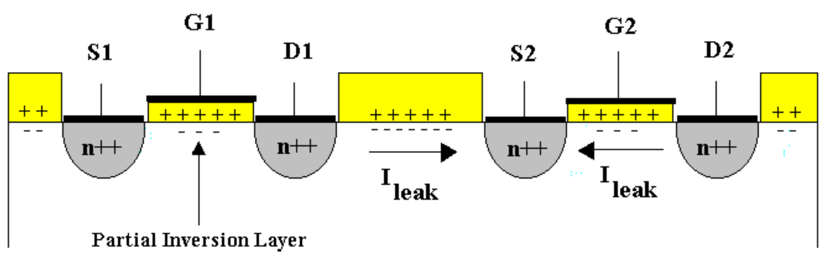

Figure 2: Parasitic n-channel transistor formed between adjacent devices. Also shown are leakage currents produced by holes trapped in gate and field oxides.

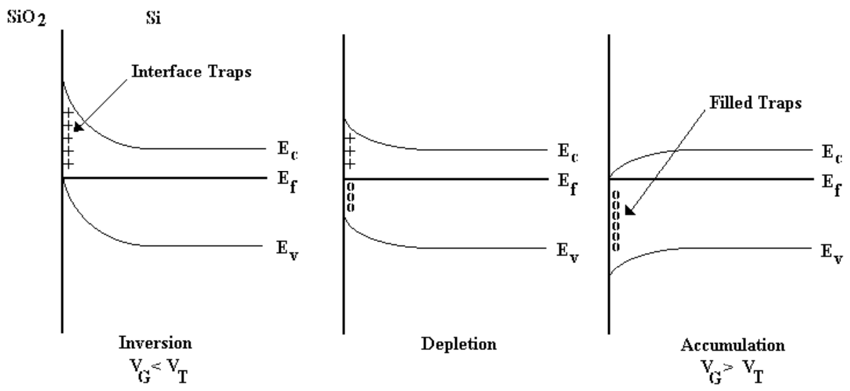

Figure 3: Voltage dependence of interface trap density for a n-bulk transistor.

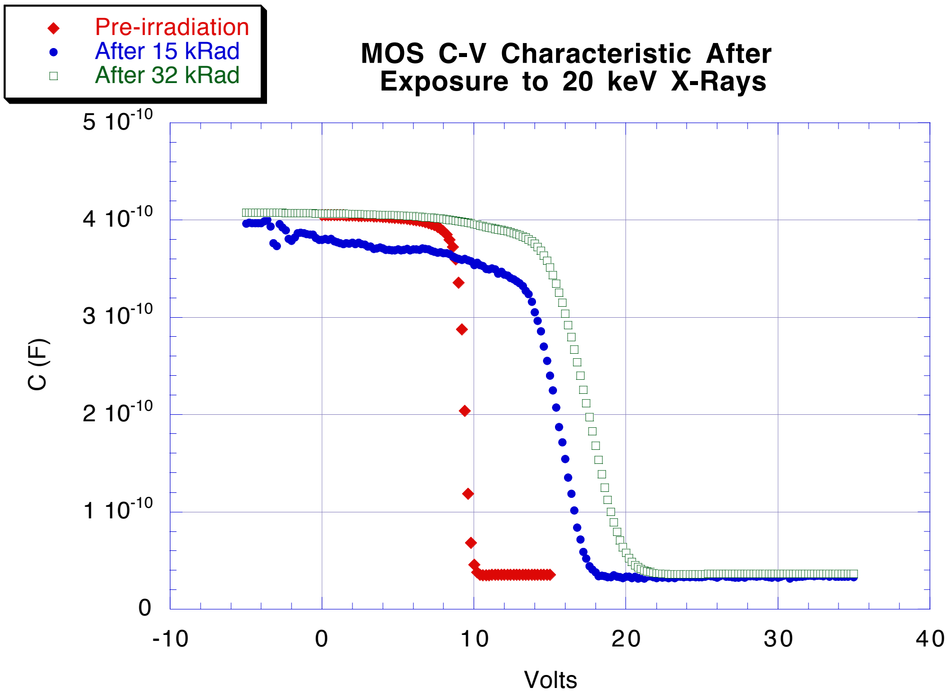

Figure 4: Capacitance-voltage characteristics of a n-bulk MOS capacitor after exposure to ionizing radiation. Inversion occurs for voltages greater than 20V. The voltage shift is caused by trapped charge in the oxide and the decrease in slope is the result of interface traps.