

Today's agenda (28-JAN-2010)

- Will check your web page (links), which should include
 - Block diagram
 - Acronym (what it is called)
 - Schedule outline
 - Description paragraph
- To be augmented with table of specifications
- Comings and goings

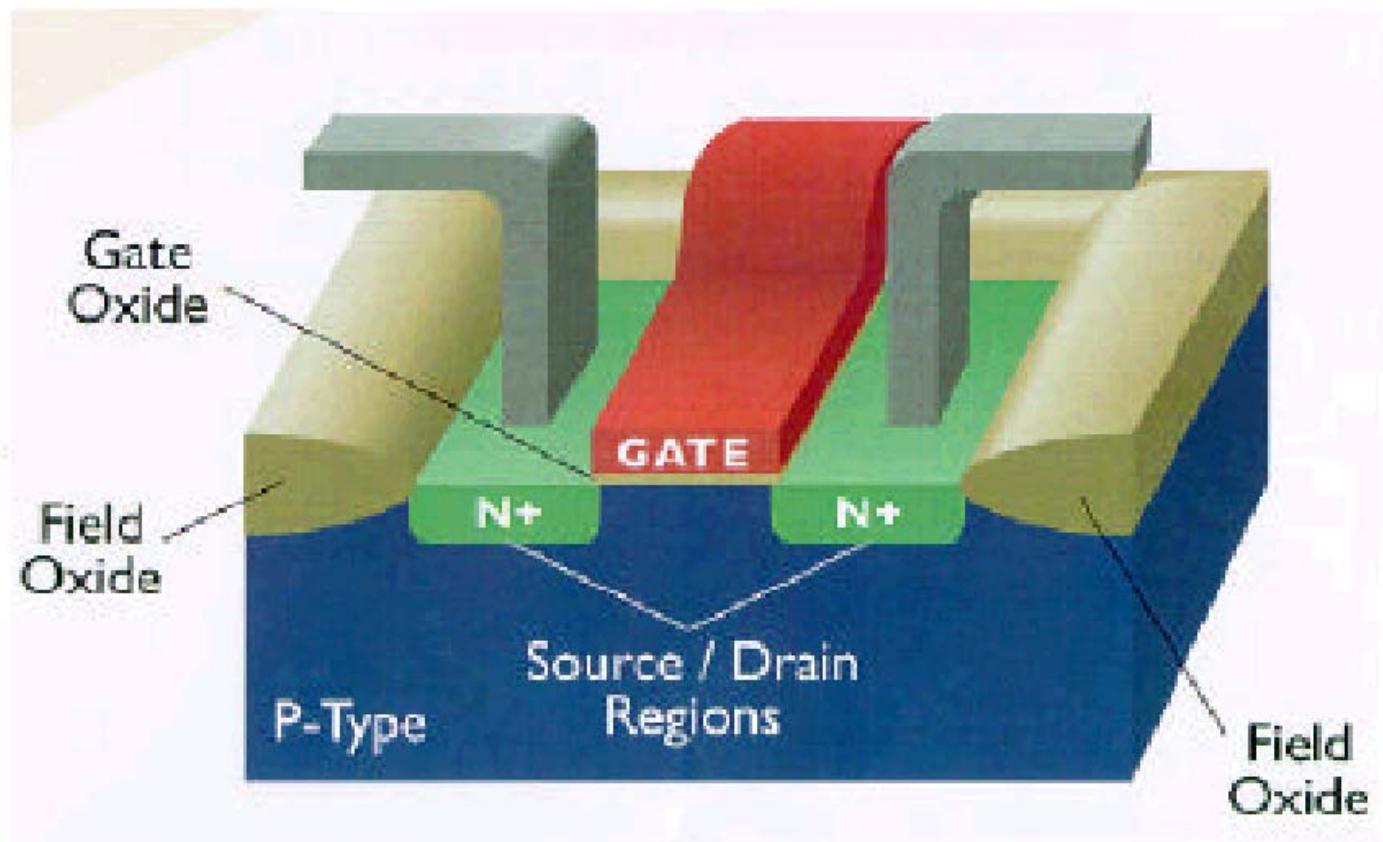
Suggested Milestones

- Specification Review [Feb 15]
 - Complete schematics
 - Block diagram
 - Table of key parameters
- Design Readiness Review [March 1-14]
 - Design simulations, iteration
 - Confirmation of key parameters
- Begin Layout [March 15]
 - Floorplanning
 - All April to complete layout
 - LVS checks during hierarchy build
 - Post layout simulations
- Final Design Review [early May]
 - Compile documentation, hold review
 - Final confirmation of key parameters

Suggested Template

Year 1 Development Schedule for Integrated x-ray Readout/DAQ														
		29-dec-09//GSV	Dec	Jan	Feb	March	April	May	June	July	Aug	Sept		
	Task	Subtask	1	2	3	4	1	2	3	4	1	2	3	4
1	350ps bunch separation demonstrator	optical comp acquisition												
		bench commission												
		acquire photodetectors												
		CDR												
		simple DAQ USB (exist)												
		PDI/RO interface board												
		Specs verification/TDR												
2	Fast DAQ system	commission												
		Measurements												
		XMC readout design												
		cPCI crate/CPU acq.												
		CDR												
		Fast link fabrication												
3	ps2 ASIC	firmware development												
		software development												
		Readiness Review												
		integration/test												
		Specs confirm												
		Preliminary design												
		CDR												
4	Custom Sensor 1	Detailed simulations												
		Layout												
		Design Review												
		MOSIS fabrication												
		Eval board fab + test												
		Integrated module design												
		Integrated module fab												
		Integration + operation												
		first beam												
		Specs confirm												

MOS Structure



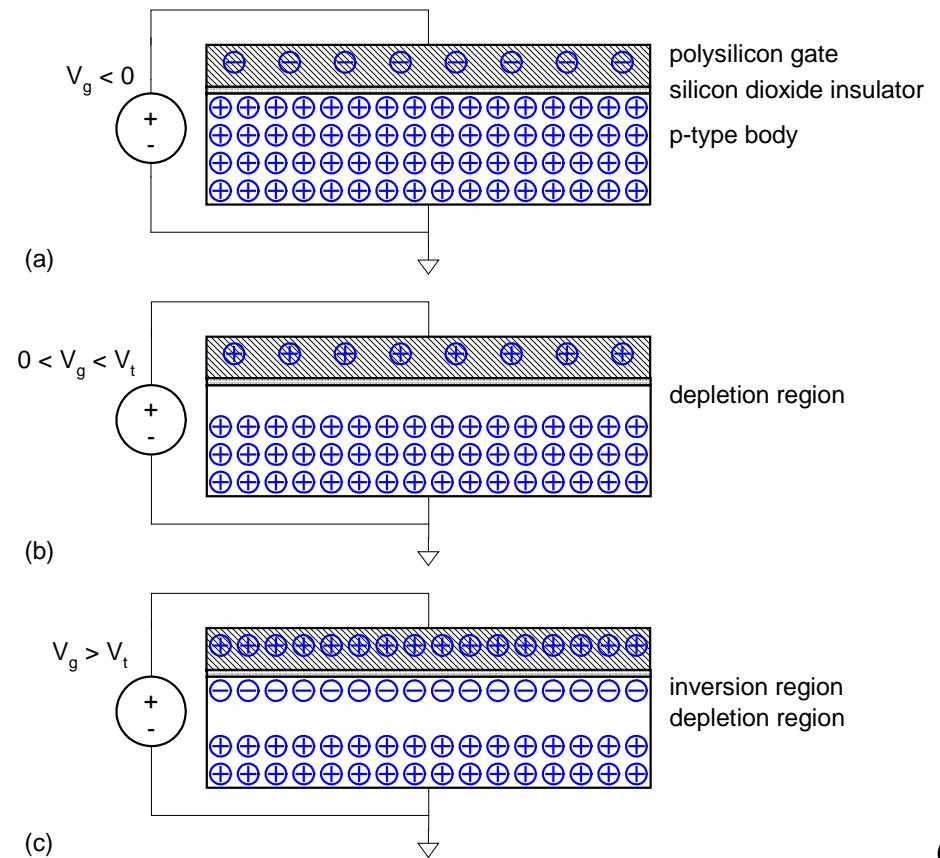
MOS Review

- Transistor gate, source, drain all have capacitance
 - $I = C (\Delta V / \Delta t) \rightarrow \Delta t = (C/I) \Delta V$
 - Capacitance and current determine speed
- MOS symbol



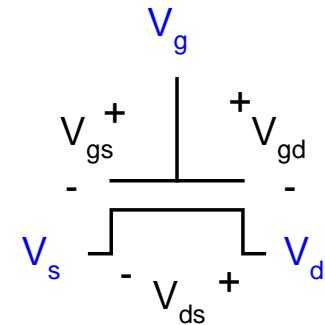
MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes
 - Accumulation
 - Depletion
 - Inversion



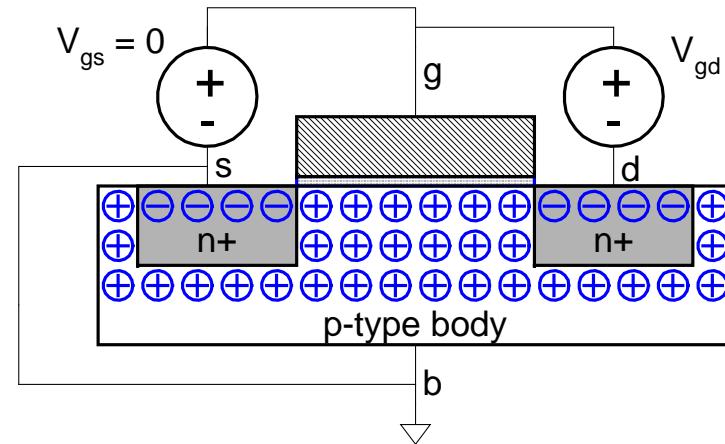
Terminal Voltages

- Mode of operation depends on V_g , V_d , V_s
 - $V_{gs} = V_g - V_s$
 - $V_{gd} = V_g - V_d$
 - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
 - By convention, source is terminal at lower voltage
 - Hence $V_{ds} \geq 0$
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
 - *Cutoff*
 - *Linear*
 - *Saturation*



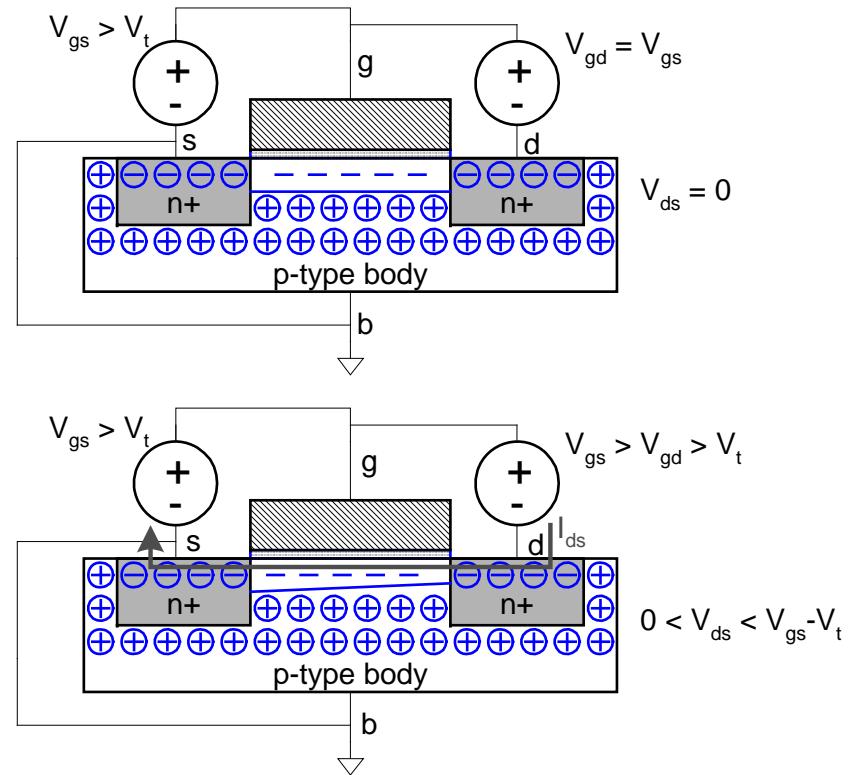
nMOS Cutoff

- No conducting channel
- $I_{ds} = 0$



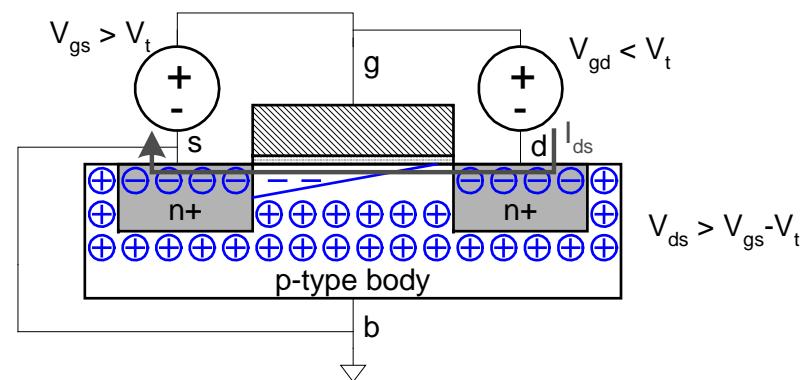
nMOS Linear

- Channel forms
- Current flows from d to s
 - e^- from s to d
- I_{ds} increases with V_{ds}
- Similar to linear resistor



nMOS Saturation

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current saturates
- Similar to current source



nMOS I-V Summary

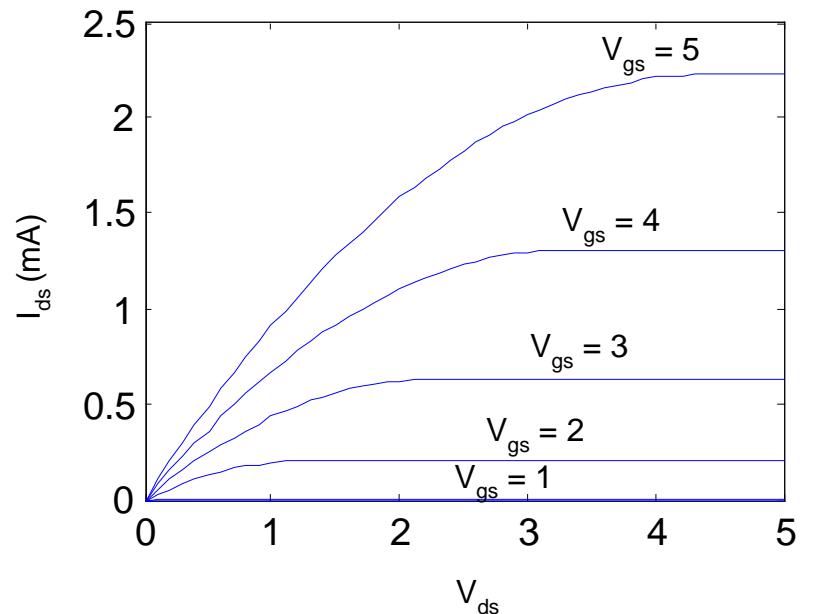
- Shockley 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \\ \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} \\ \frac{\beta}{2} \left(V_{gs} - V_t \right)^2 & V_{ds} > V_{dsat} \end{cases}$$

cutoff
linear
saturation

Example

- As an example, consider the $0.6 \mu\text{m}$ process from AMI Semiconductor
 - $t_{ox} = 100 \text{ \AA}$
 - $\mu = 350 \text{ cm}^2/\text{V}\cdot\text{s}$
 - $V_t = 0.7 \text{ V}$
- Plot I_{ds} vs. V_{ds}
 - $V_{gs} = 0, 1, 2, 3, 4, 5$
 - Use $W/L = 4/2 \lambda$



$$\beta = \mu C_{ox} \frac{W}{L} = (350) \left(\frac{3.9 \cdot 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}} \right) \left(\frac{W}{L} \right) = 120 \frac{W}{L} \mu\text{A}/\text{V}^2$$

pMOS I-V

- All dopings and voltages are inverted for pMOS
- Mobility μ_p is determined by holes
 - Typically 2-3x lower than that of electrons μ_n
 - $120 \text{ cm}^2/\text{V}\cdot\text{s}$ in AMI 0.6 μm process
- Thus pMOS must be wider to provide same current
 - As a starting point, assume $\mu_n / \mu_p = 2$

Current-Voltage Relations Long-Channel Device

Second Order Effect

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \epsilon_{ox}}{t_{ox}}$$

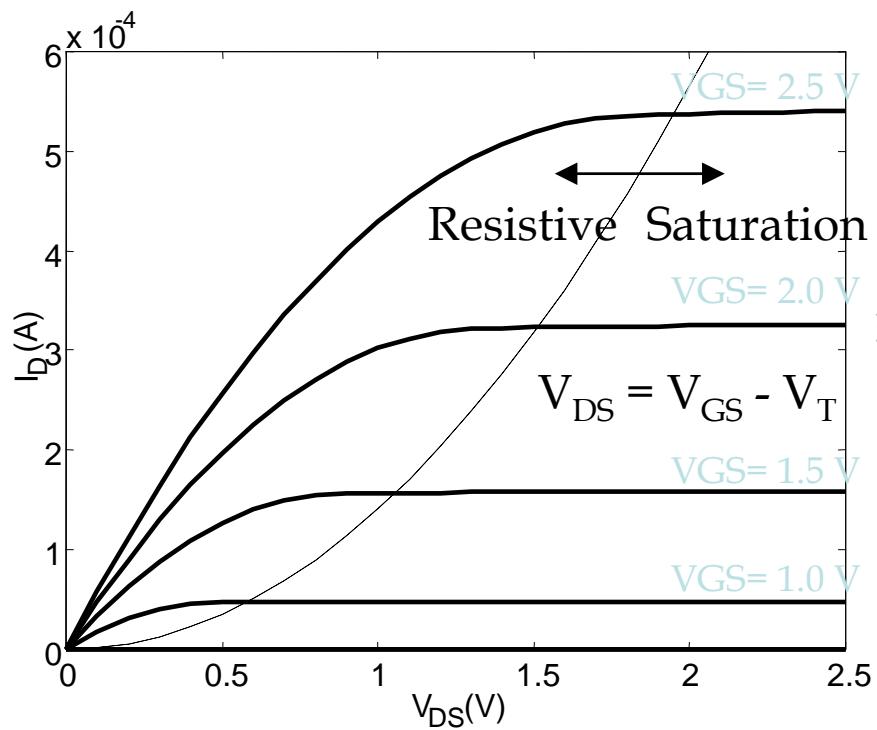
Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

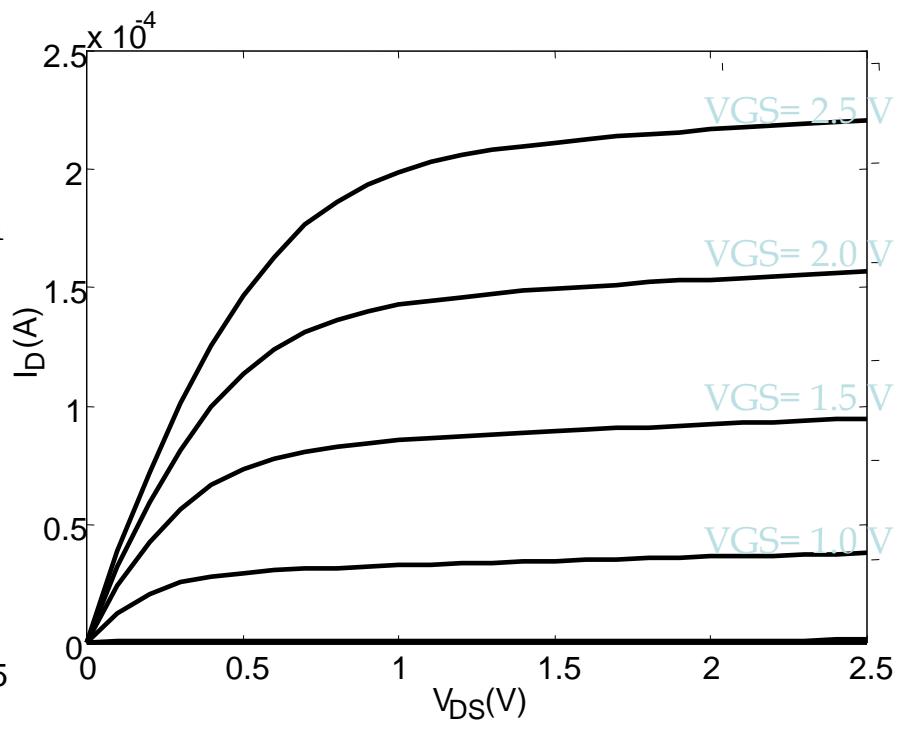
$$I_D = \frac{k'_n W}{2} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

↙
 Channel Length Modulation

I_D versus V_{DS}

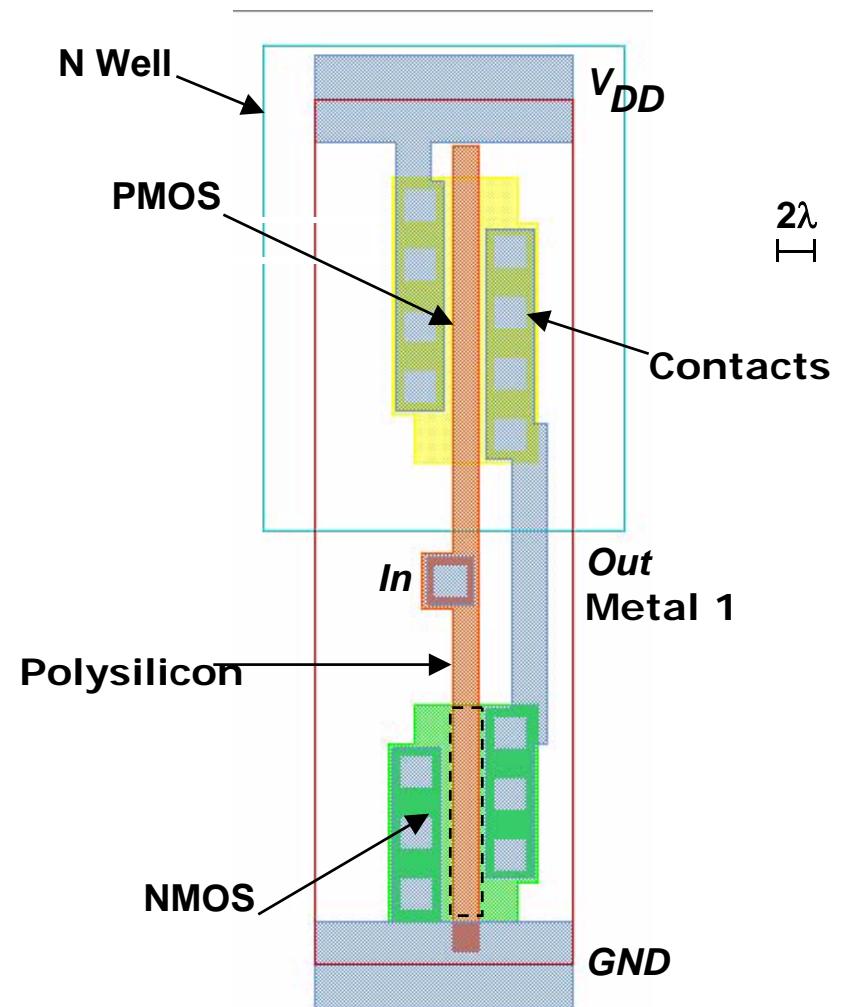
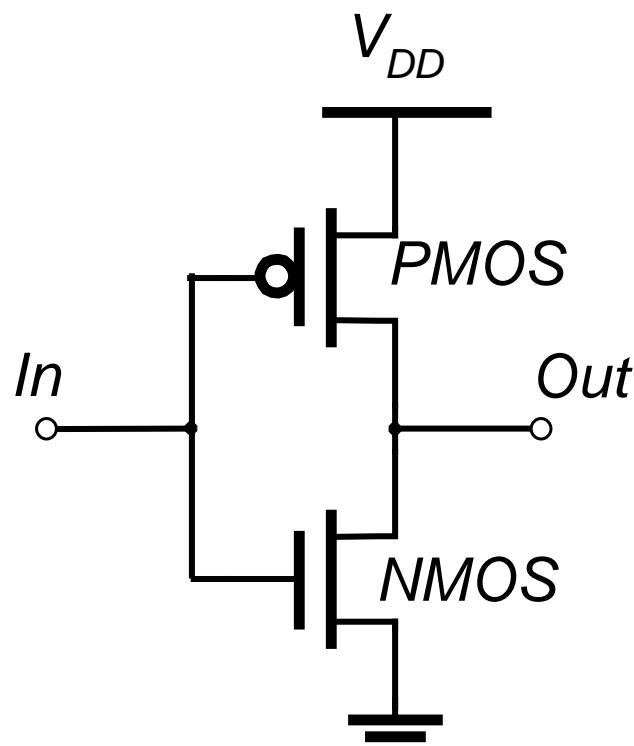


Long Channel



Short Channel

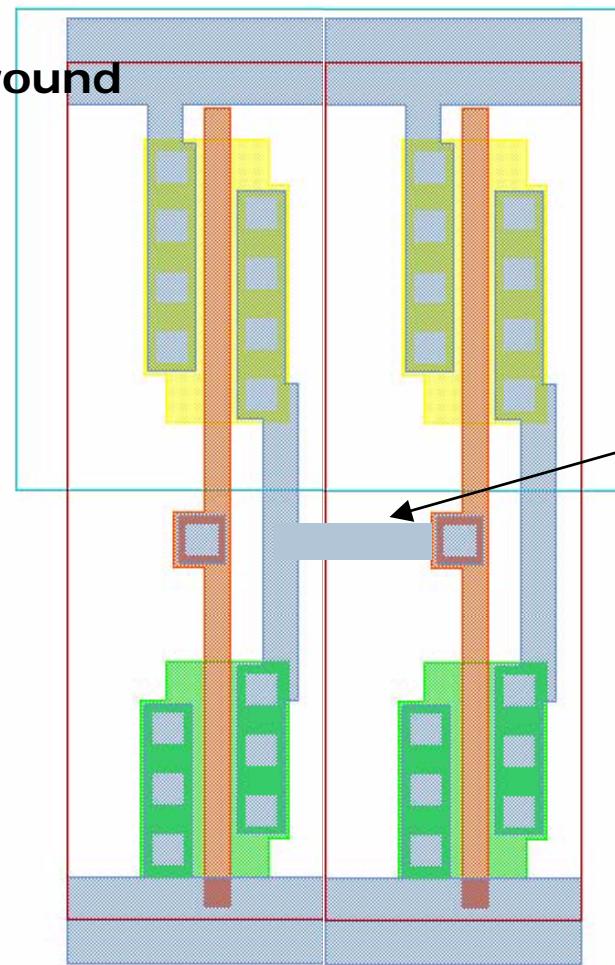
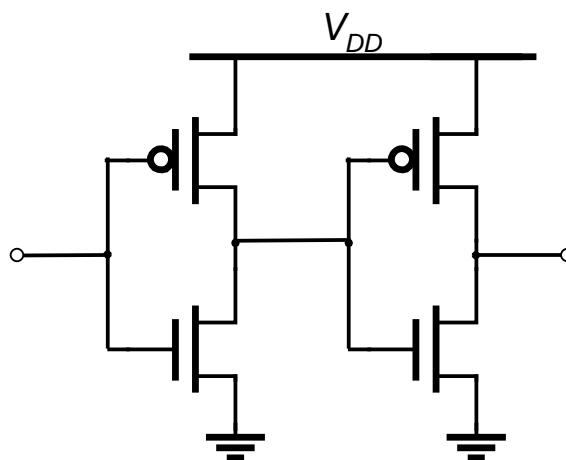
CMOS Inverter



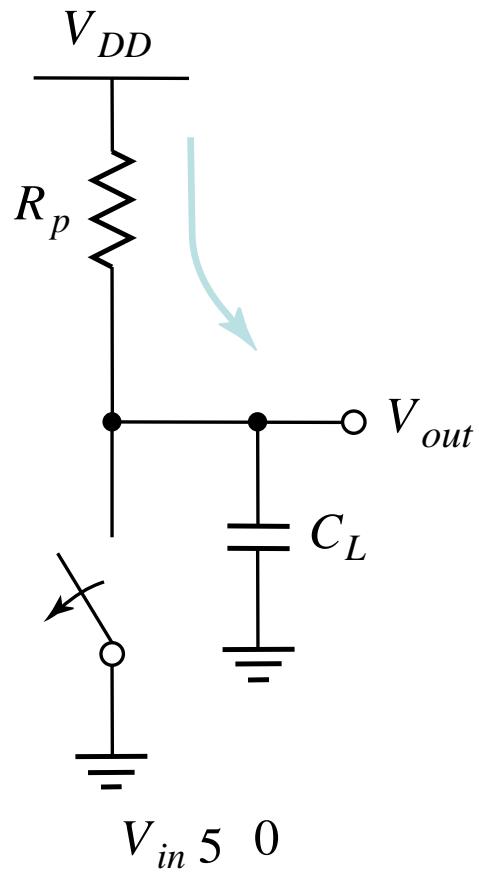
Two Inverters

Share power and ground

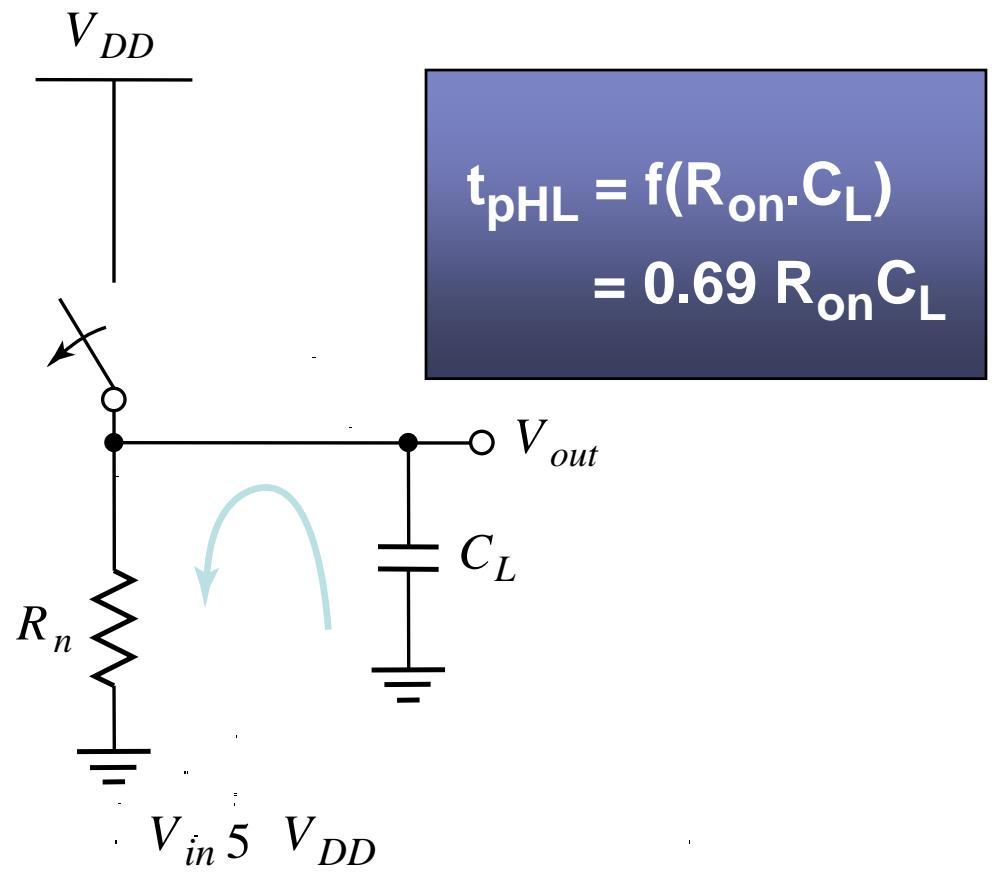
Abut cells



CMOS Inverter as Switch



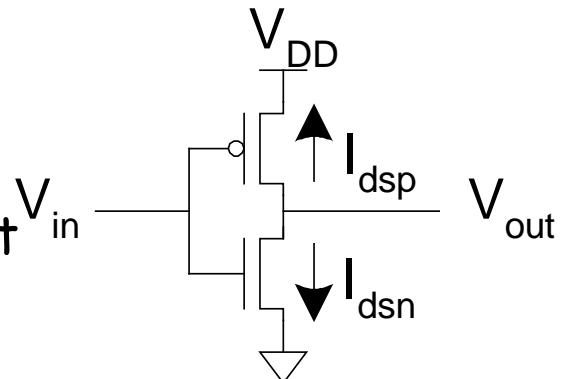
(a) Low-to-high



(b) High-to-low

DC Response

- DC Response: V_{out} vs. V_{in} for a gate
- Ex: Inverter
 - When $V_{in} = 0 \rightarrow V_{out} = V_{DD}$
 - When $V_{in} = V_{DD} \rightarrow V_{out} = 0$
 - In between, V_{out} depends on transistor size and current
 - By KCL, must settle such that $I_{dsn} = |I_{dsp}|$
 - We could solve equations
 - But graphical solution gives more insight

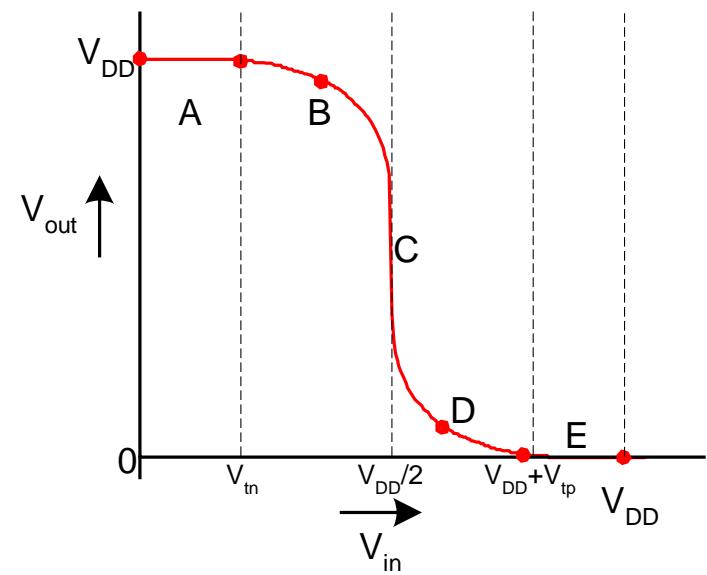
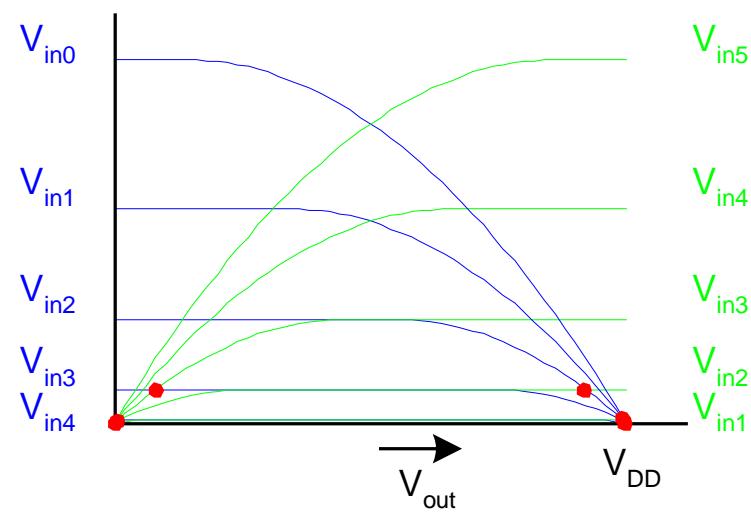


Transistor Operation

- Current depends on region of transistor behavior
- For what V_{in} and V_{out} are nMOS and pMOS in
 - Cutoff?
 - Linear?
 - Saturation?

DC Transfer Curve

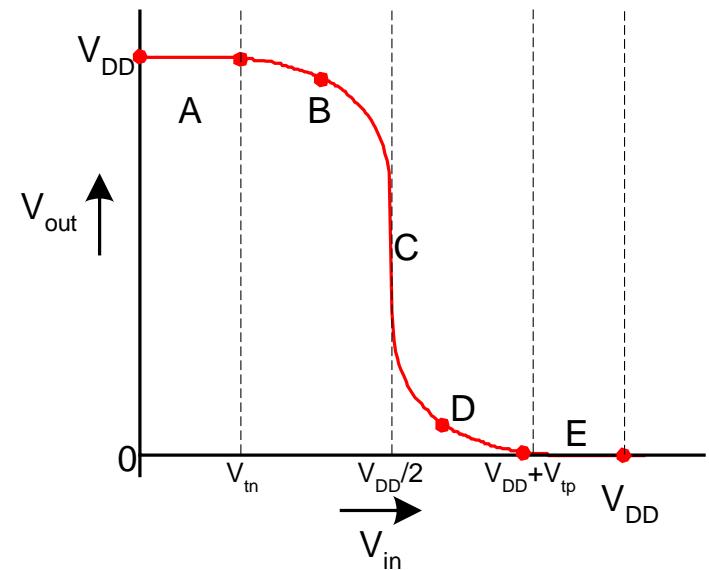
- Transcribe points onto V_{in} vs. V_{out} plot



Operating Regions

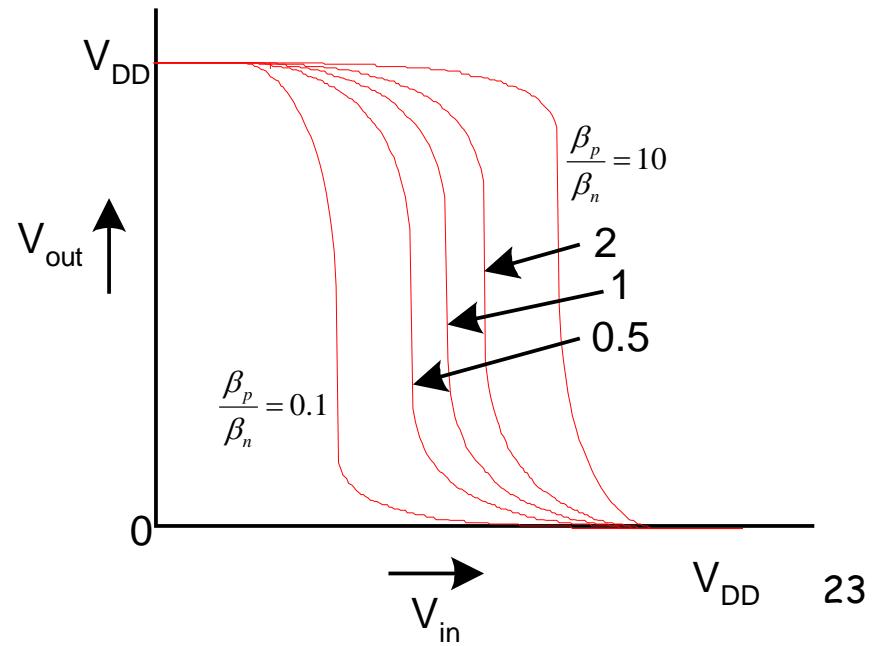
- Revisit transistor operating regions

Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff



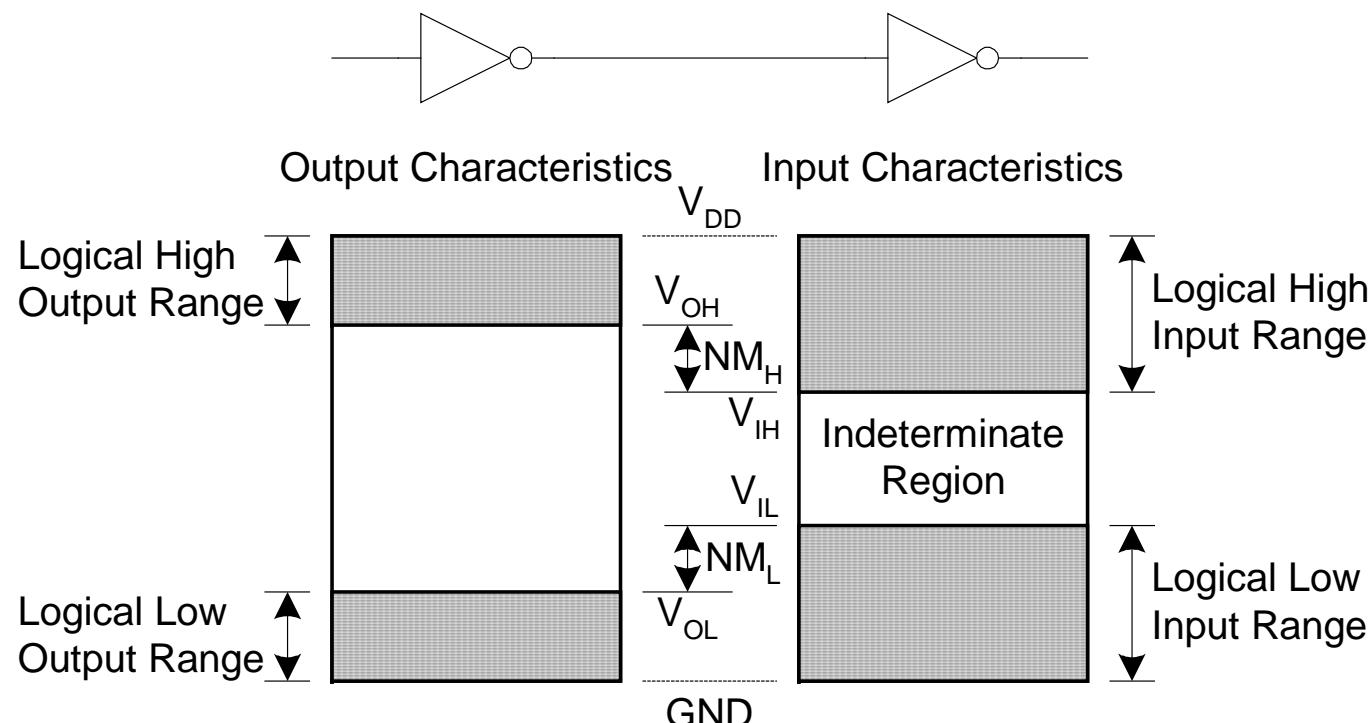
Beta Ratio

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed gate*
- Other gates: collapse into equivalent inverter



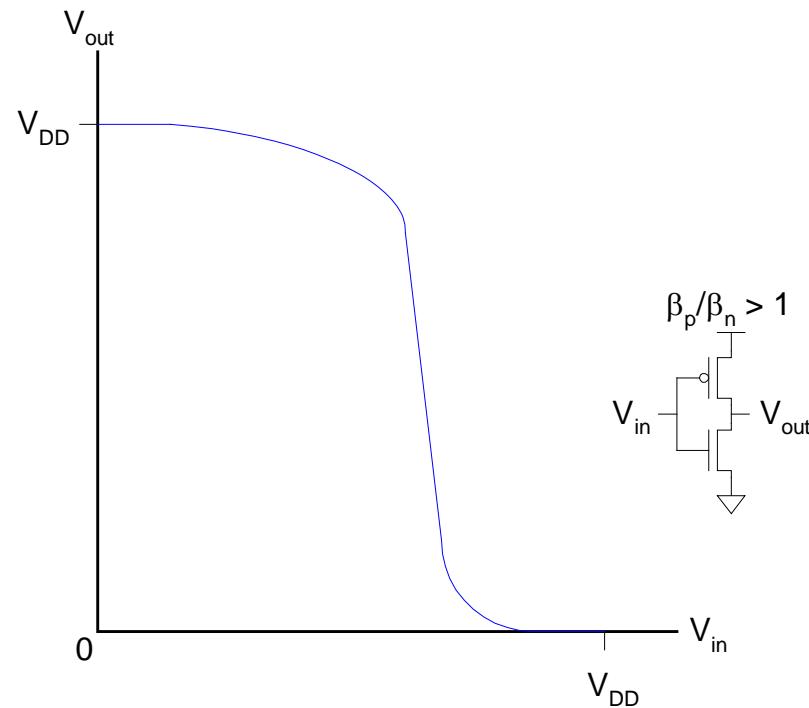
Noise Margins

- How much noise can a gate input see before it does not recognize the input?



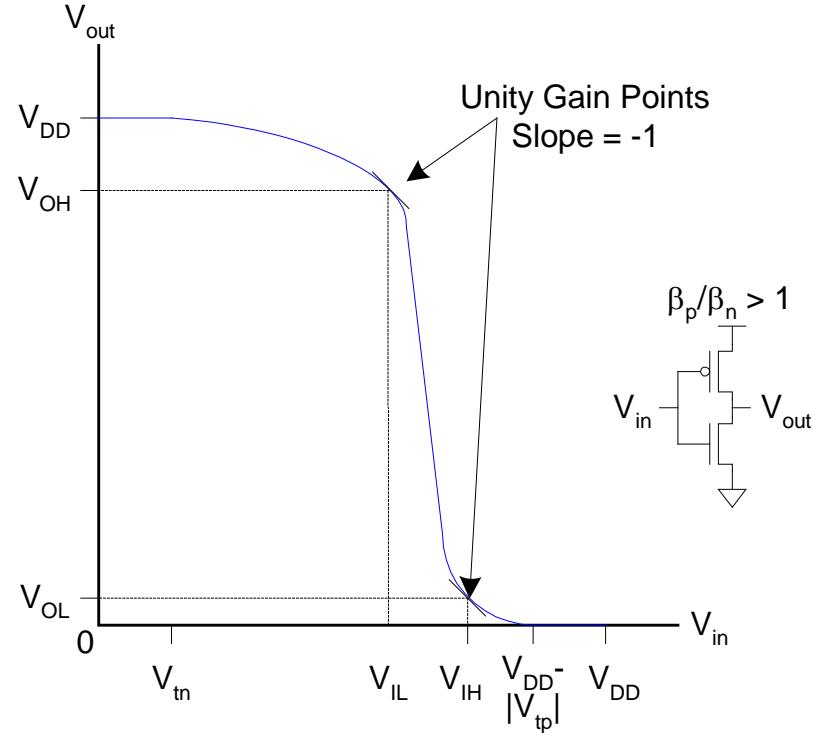
Logic Levels

- To maximize noise margins, select logic levels at



Logic Levels

- To maximize noise margins, select logic levels at
 - unity gain point of DC transfer characteristic



For next time

- Will check your web page (links), which should include
 - Block diagram
 - Acronym (what it is called)
 - Schedule outline
 - Description paragraph
- To be augmented with table of specifications
- Start building what can in Cadence - will start on simulation from next week

