Cadence Design Flows

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Feb. 18, 2010
Outline

- Cadence Design Flows
- Cadence Tools
- Simulations
- Design Checks
- Design Kit Info
Cadence Design Flows

- A design flow is from initial design conception to tape-out.
- Design flows are broken into three types:
  - Digital
  - Analog
  - Mixed – Signal
- Choose a flow based on what the majority of your design will use.
- In FPGA terms, the design flow is broken into three stages (with Xilinx) and all integrated together. ASIC tools are much more separated.
Digital Flow

- Design using an HDL
- The synthesizer does (most) placement and optimization of the design
- Designer might never even see the layout
  - How FPGA flow works
- Requires standard cells supported by the tool
  - Flip-flops, inv, pads, etc
Analog Flow

- Schematic based design flow and simulation
- Manual placement and drawing of all structures*
- Works with libraries from other tools

* Options for auto-placement and auto-routing.
Mixed Signal Flow

- Having both digital (HDL) and analog designed components in a single design
- Can be primarily digital or analog focused
  - Can mix and match for a design
Cadence Tools

- Versions:
  - Cadence 5 vs Cadence 6
  - L, XL, GXL

- Digital:
  - SOC Encounter

- Analog:
  - Virtuoso, Schematic

- Simulations:
  - ADE
Cadence Versions

- **Cadence 5:**
  - More design kit support
  - More PCELL / SKILL* support
  - CDB backend
  - Support phasing out in 1-2 years

- **Cadence 6:**
  - Completely different design kit requirements
  - Long term / future support
  - OA (Open Access) backend

PCELL: Automatically adjusted cells, e.g. transistors in the IBM kit
SKILL: Cadence scripting environment / language
Backend information

- CDB is the storage format for Cadence 5.
- OA is the storage format for Cadence 6.
- CDB and OA are NOT compatible!
- Conversion is supported. Kind of.
- If you have a design library from Cadence 5, you must convert the design to OA to use in Cadence 6.
- CDB → OA is possible. OA → CDB not so much.
Version Letters

• Cadence has three levels of products (applies to Virtuoso Schematic and Layout):
  - L – Basic tools, polygon editor (V)
  - XL – Interconnection information (V)
  - GXL – Automatic tools: placement, routing, etc.

• Cadence uses 'tokens' for licensing:
  - L might use 1 token, XL 3 tokens, GXL 9 tokens.
  - Stick with XL when possible.
  - NOTE: If you open a design with L in layout and save, you lose the interconnection information. Therefore, if you open later with XL, you won't see connection information.
SOC Encounter

- Cadence's digital RTL – GDSII program
- Supports HDL* while performing:
  - Floorplanning
  - Clock distribution
  - Power planning
  - Place and Route (PR)
  - Analysis
    - Timing, Power, Interconnect, Signal integrity, etc
    - Design for Manufacturing (DFM)
    - Design Rule Checking (DRC)

* HDL = Verilog, VHDL, Verilog-a, VHDL-a, System-C, etc
`Technically they are separate tools integrated into SOC.`
Virtuoso

- Cadence's analog design tools
- Includes:
  - Schematic
  - Layout
- Integrates analog layouts with block placements
Analog Design Environment (ADE)

- ADE is a visual wrapper to command line simulation environment (Spectre)
- Integrated results browser (wavebrowse)
- Performs many simulation types:
  - Trans, DC, parametric, etc
Spectre

- Spectre is Cadence's version of SPICE.
- Spectre is ~compatible with SPICE.
  - For proper models (IBM), both Spectre and SPICE will converge.
- We use Spectre 7.0
  - Default Spectre included with Virtuoso is 5.1, does not work with IBM models.
- Spectre models are different than SPICE models!
  - There is a tool (spp) to convert SPICE to Spectre models. It is touchy to say the least.
Some things to keep in mind

- You must place a vdc=1.2 somewhere in your schematic for simulations
- Simulations are only as good as the data you input
  - Simulations don't check manufacturability
- Design kits get upgraded
  - Don't save libraries/simulations/etc inside the design kit directory!
Folder Hierarchy

- /$USER
  - /design
    - /library
      - /$PROJECT_NAME
    - /kits
      - /IBM_1.6.2.5_IC614
        - /DRC
        - /LVS