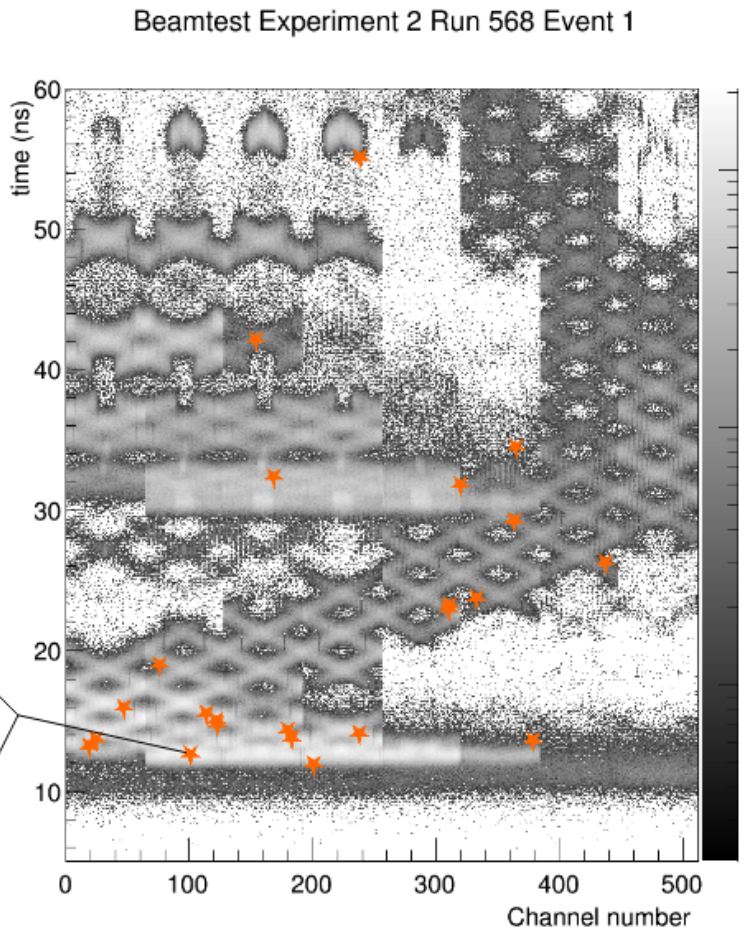
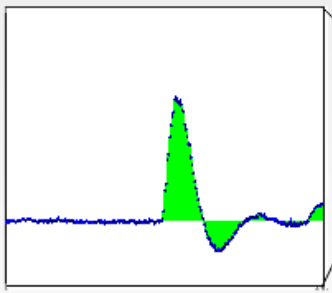
Prospect and Plan for IRS3B Readout

1. Progress on Key Performance Parameters
2. Understanding limitations during LEPS operation
3. Carrier02 Rev. C (with O-E-M improvements)
4. Pre-production tasks/schedule





Toru Iijima

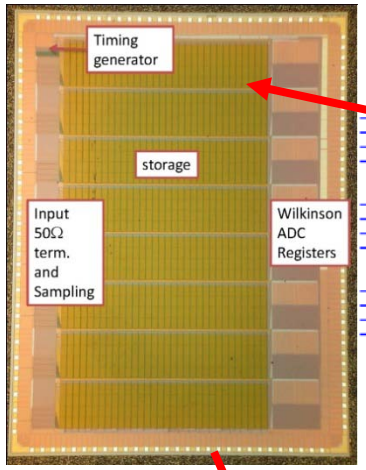
Aug. 21, 2013 KEKB Steering Committee report

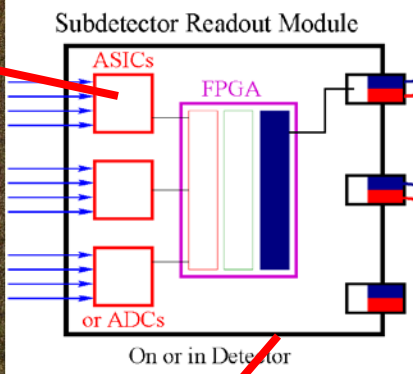
IRS3B-based Readout Overview

Waveform sampling ASIC

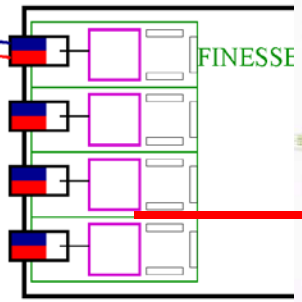
64 DAQ fiber transceivers

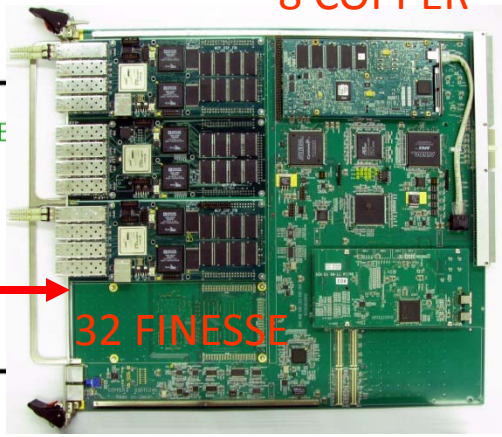
8 COPPER





Giga-bit Fiber Transceiver Links





32 FINESSE

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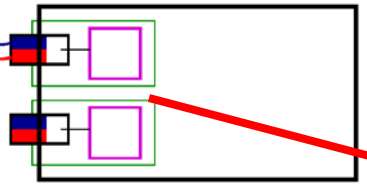


UT3 Trigger module

FPGA firmware consists of 3 parts:

1) ASIC/ADC driver (common)

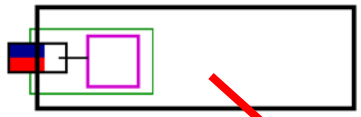
2) Trigger/feature extract (subdet. specific)

3) Unified DAQ transport protocol

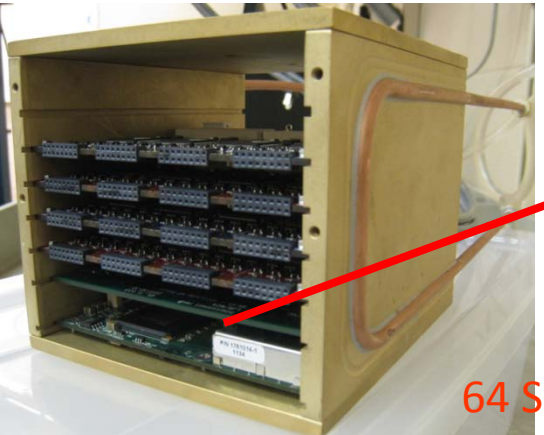
8k channels

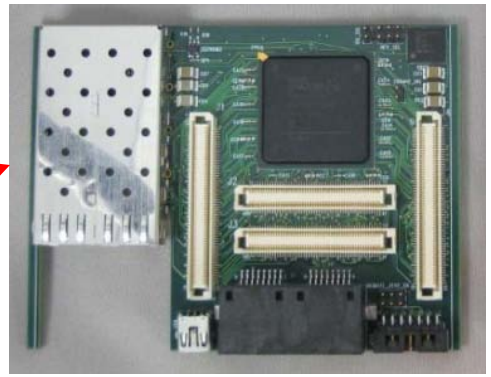
1k 8-ch. ASICs

64 SRM "board stacks"



Clock jitter cleaners





FTSW clock, trigger, programming

16 FTSW

64 SRM

Executive Summary

• After commissioning/learning period, now obtaining electronics resolutions commensurate with stated minimum requirements (<100ps timing)

• Still room to improve:

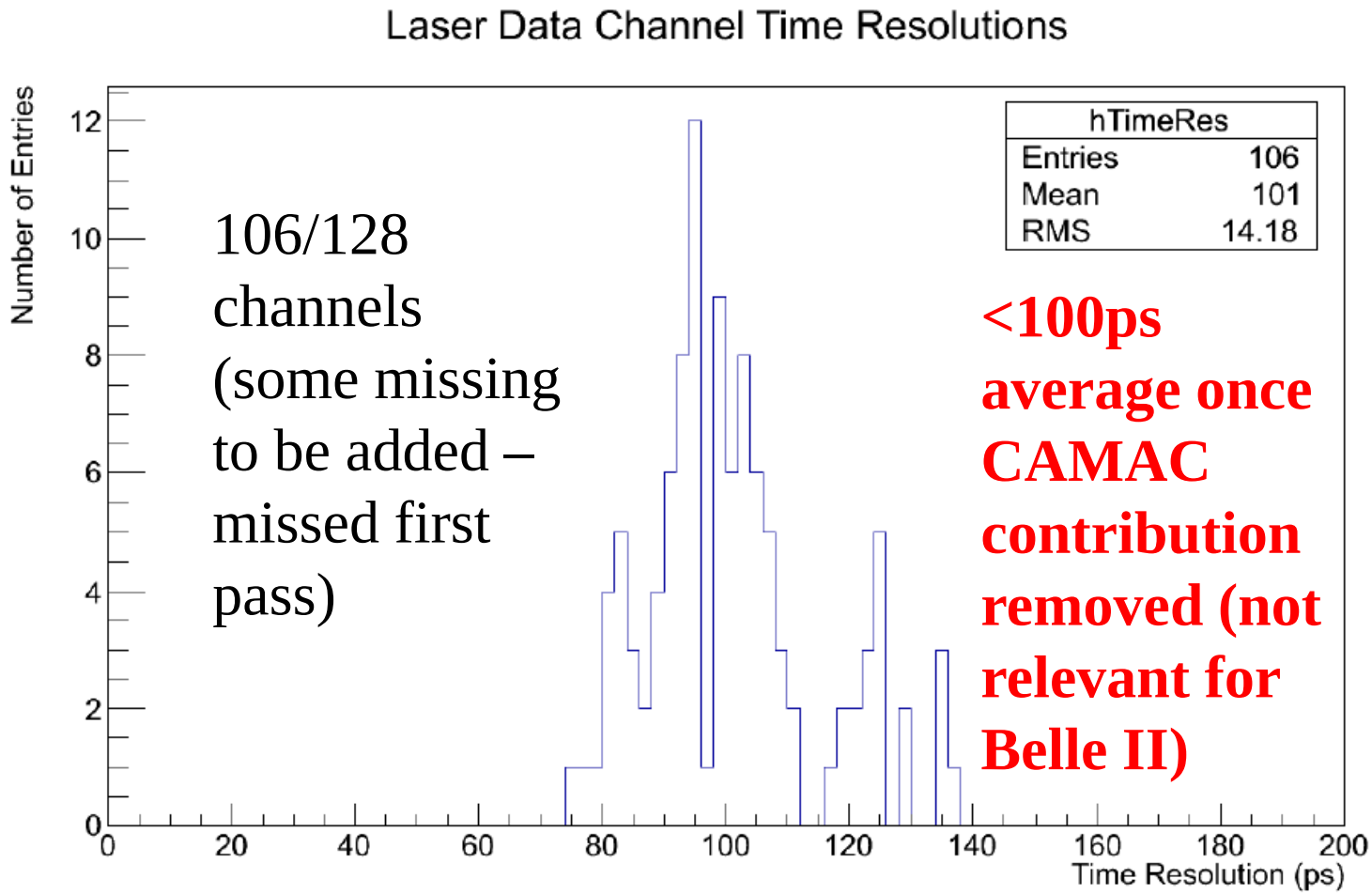
- Processing: timebase cal, leading edge timing extraction
- Board improvements: sampling timebase, gain, risetime

• Rev. C Carrier boards [improved mechanics, amplifiers, signal coupling] being assembled, testing soon

• IRS3C [extended dynamic range] due this week

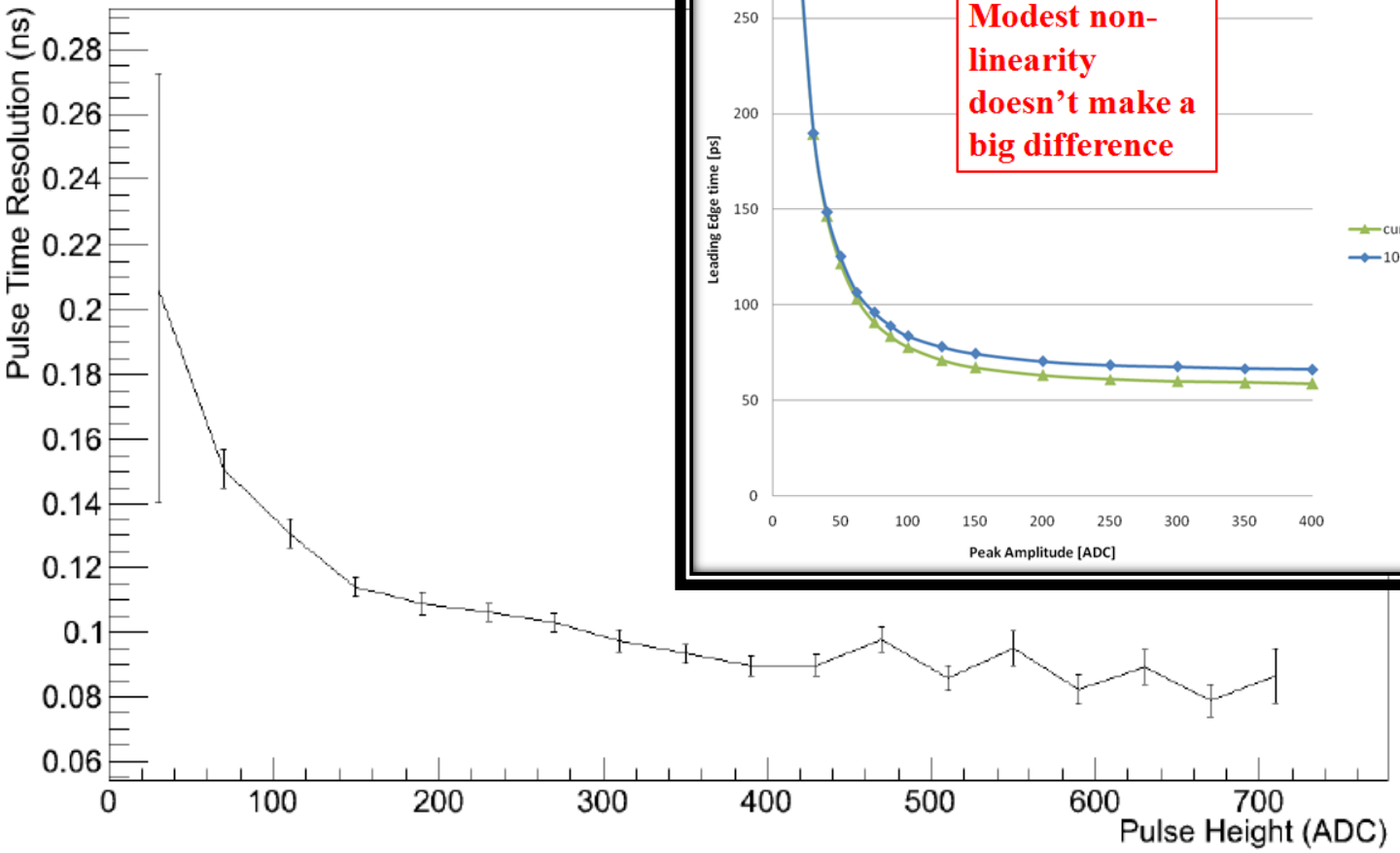
• **Details in subsequent slides**

Board Stack #37 single photon timing, no ADC cuts, no modifications from LEPS configuration



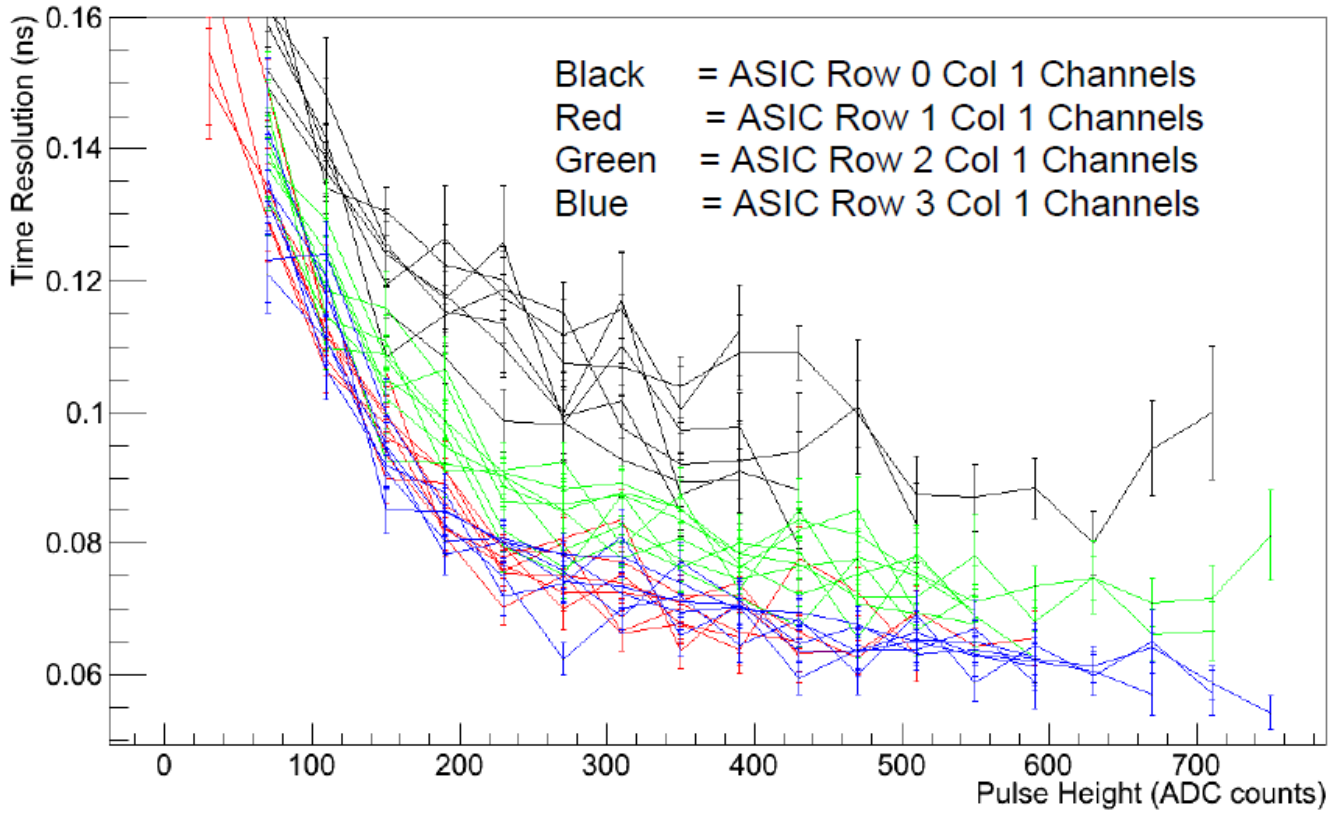
- Overall average time resolution is 101 +/- 14 ps
- Need to understand large variation in time resolution across channels

As understood from simulation



- Time resolution clearly depends on pulse height
- To a large extent, channel time resolution will depend on pulse height distribution

Channels within same ASIC similar – common timing/timebase issue

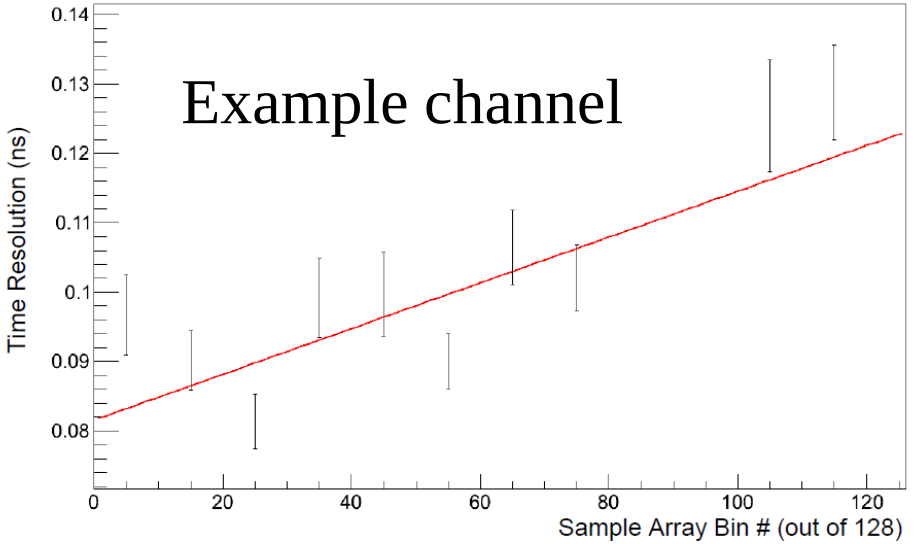


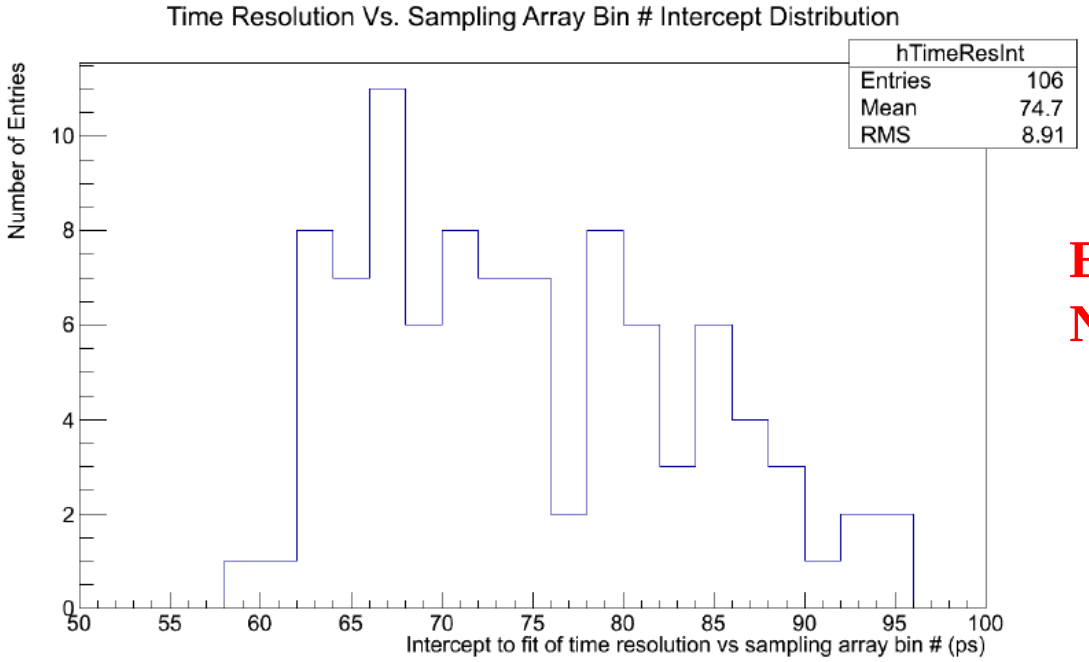
- Channels on same ASIC share have similar pulse height dependence for time resolution

If dominated by DAC/VadjN jitter, should see clear dependence…

And it is clearly observed

Probably a combination of jitter (noise on VadjN) and coarseness of DAC [under study]



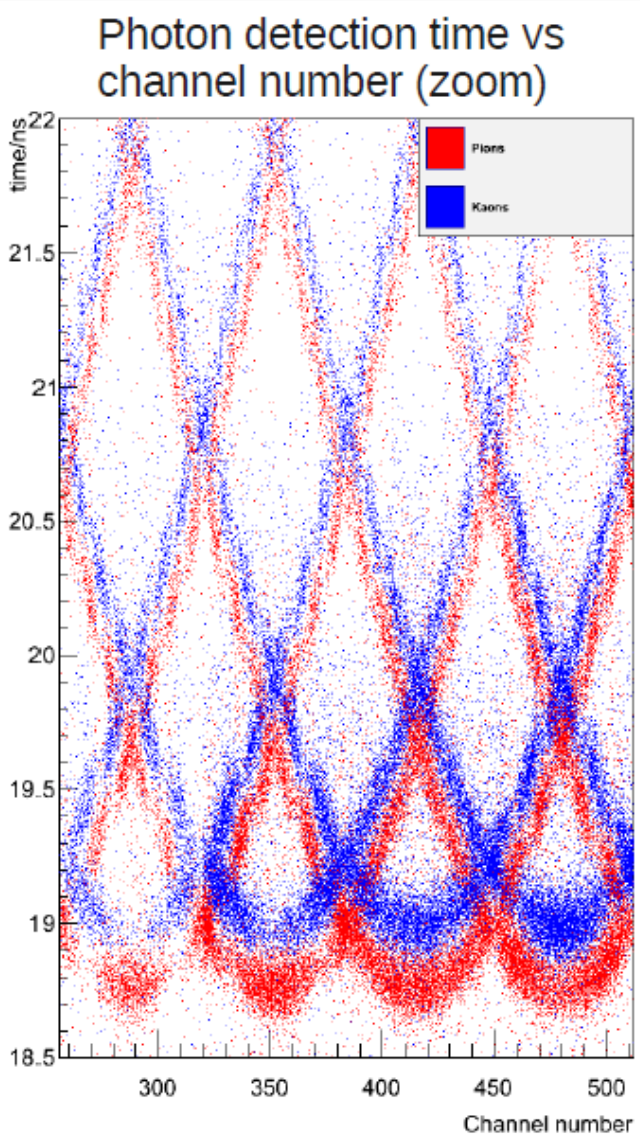


Ensemble distribution, No ADC cuts

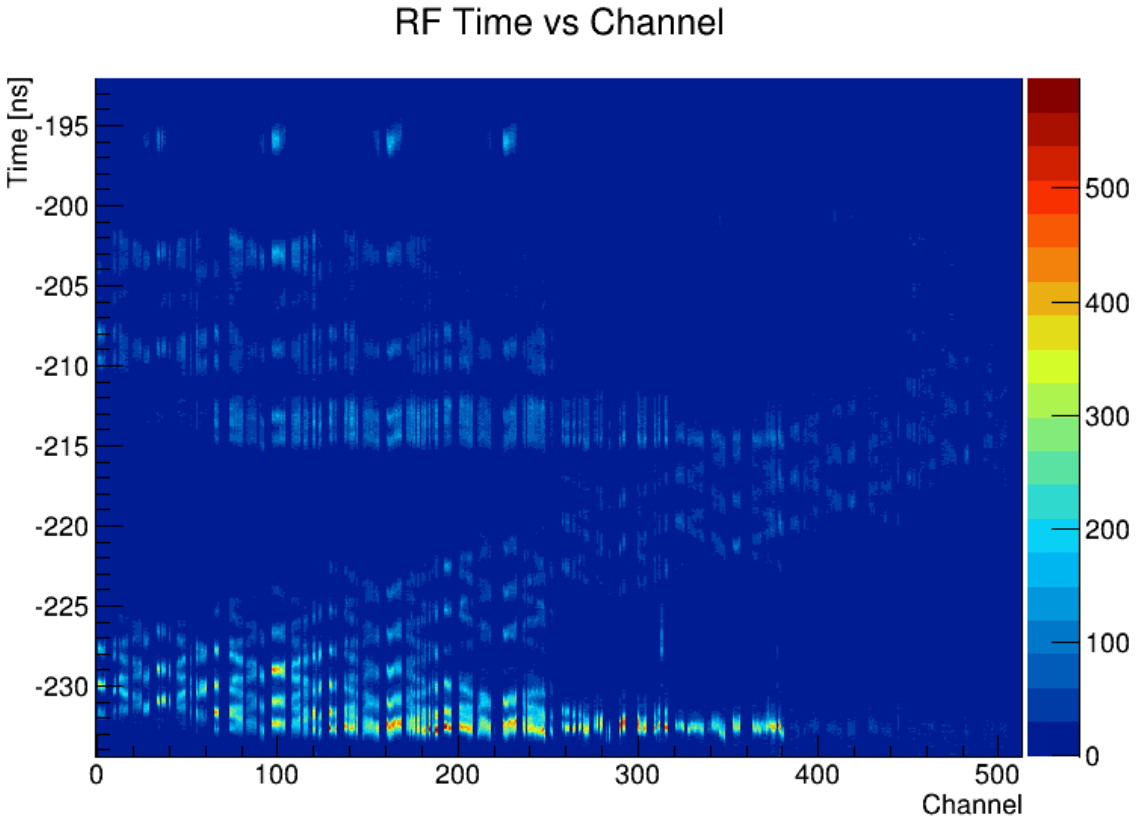
- Plot distribution of intercepts from linear fit to time resolution vs. sampling array bin # plot
- Represents time resolution if there was no degradation along sampling array

Pedagogical slides about timing…

- Space-time correlations

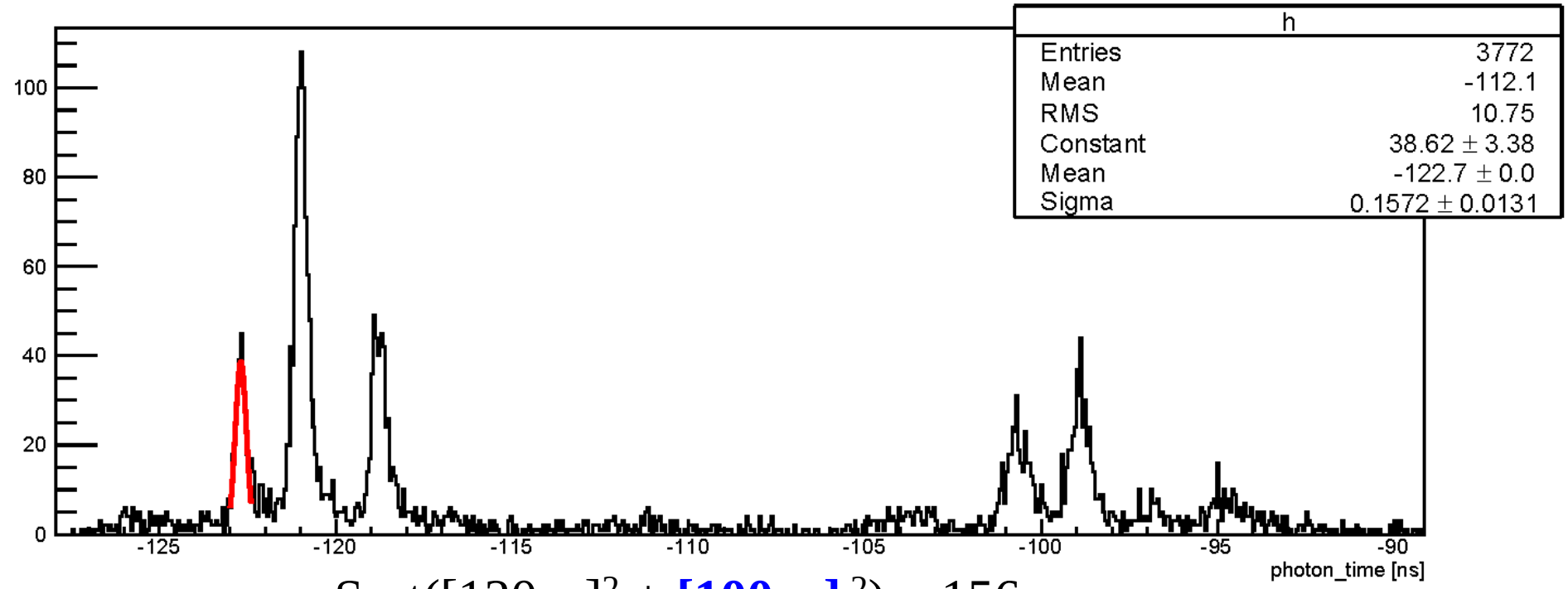


Beam Test Data



About LEPS timing current status… (work in progress)

- For large amplitude, corresponding to the tight cuts applied, and assuming (“120ps” width)…

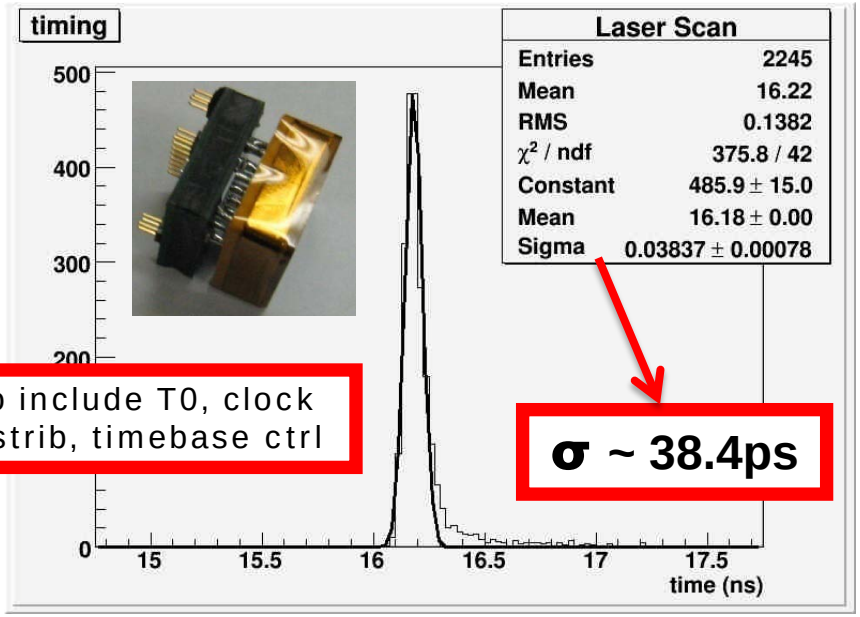


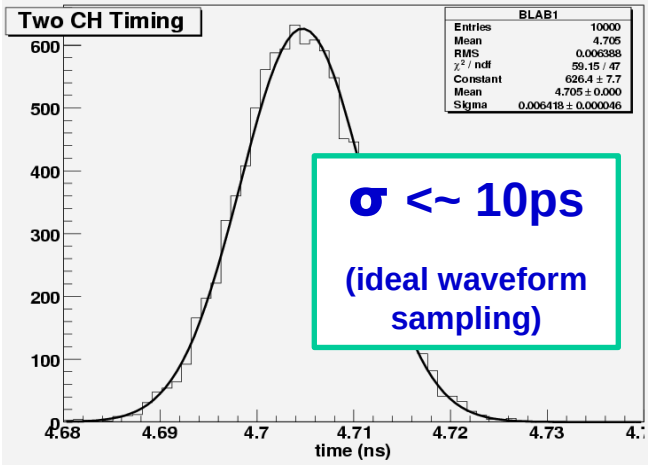
Sqrt([120ps]^2 + **[100ps]** ^{2}) ~ 156 ps

Electronics contribution

Performance Requirements (TOP)

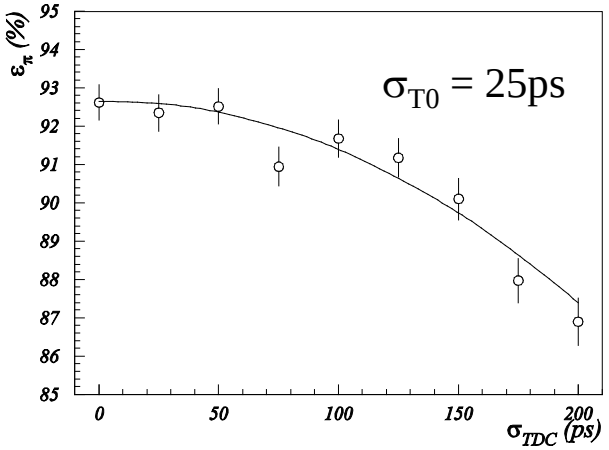
- Single photon timing for MCP-PMTs

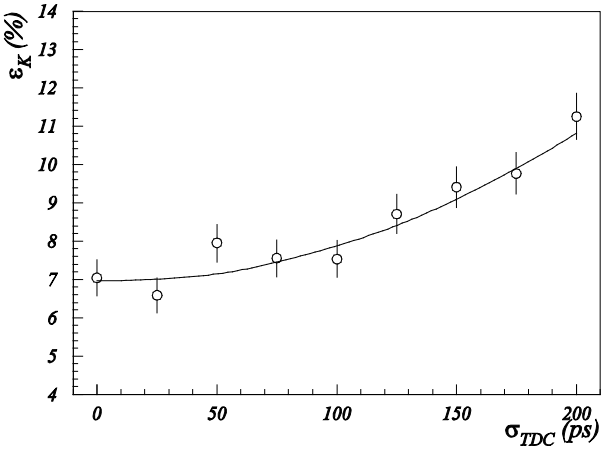




NIM **A602** (2009) 438

σ <= 100ps ➔ 1% impact



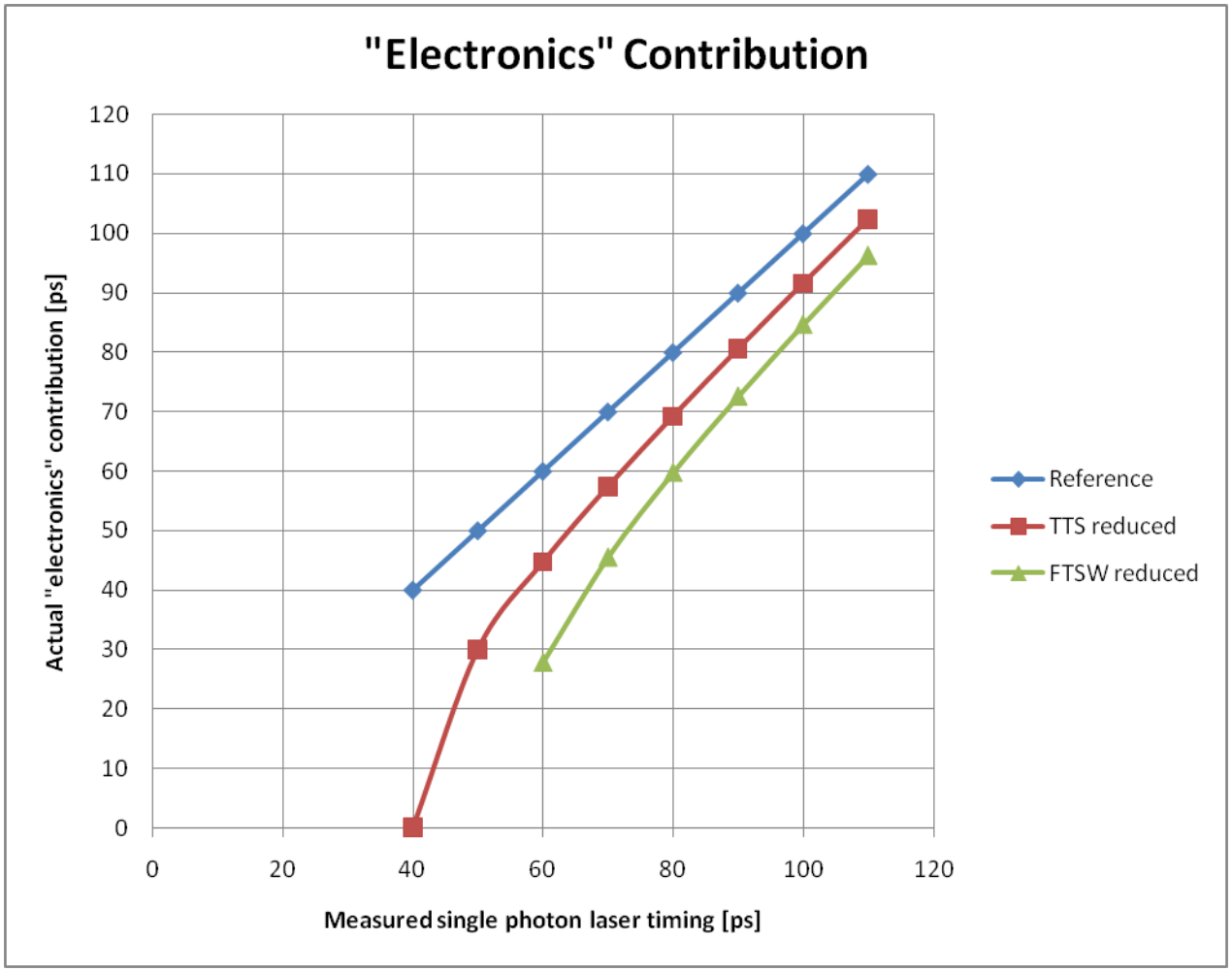


σ <~ 50ps target

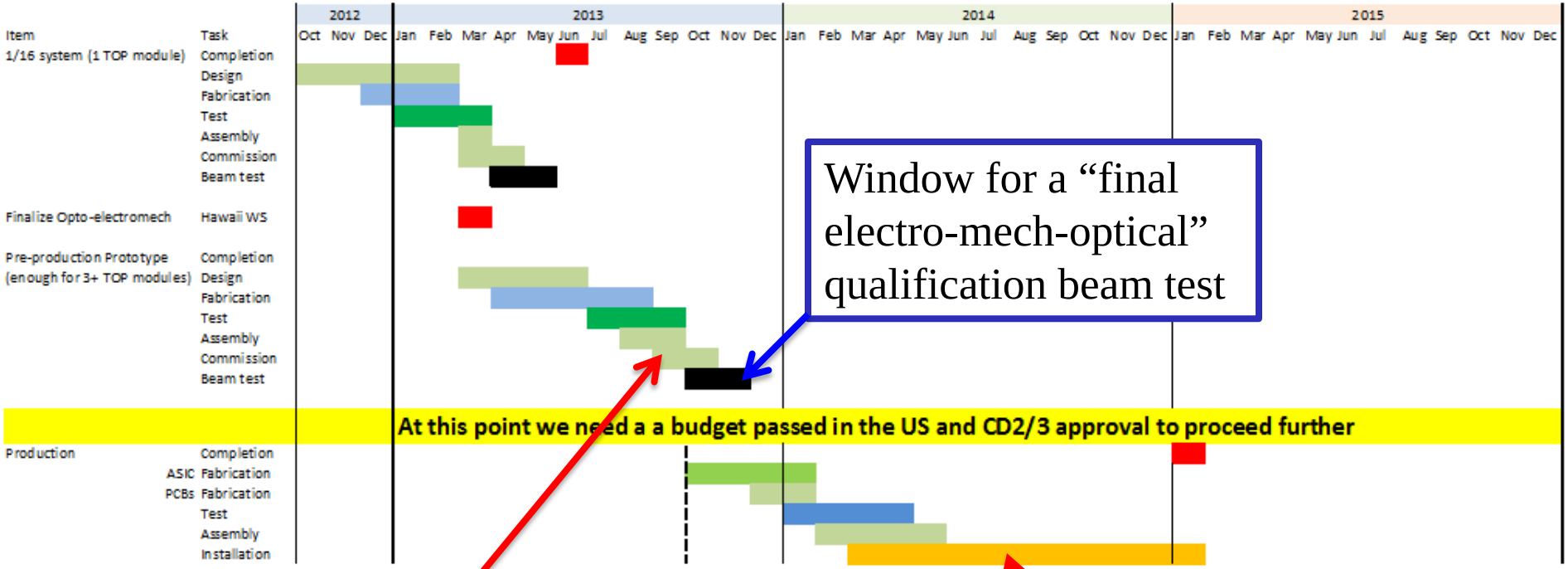
NOTE: this is single-photon timing, **not** event start-time "T_0"

Electronics contribution

- 100ps is min. required for Key Performance Parameters (50ps target)



TOP Electronics Production Schedule



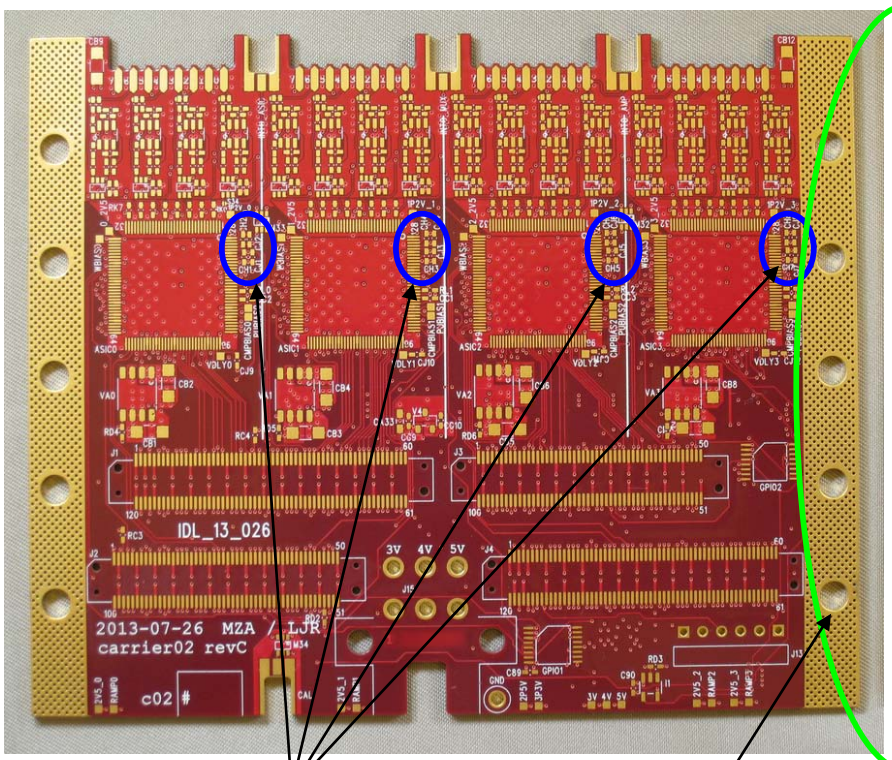
Window for a "final electro-mech-optical" qualification beam test

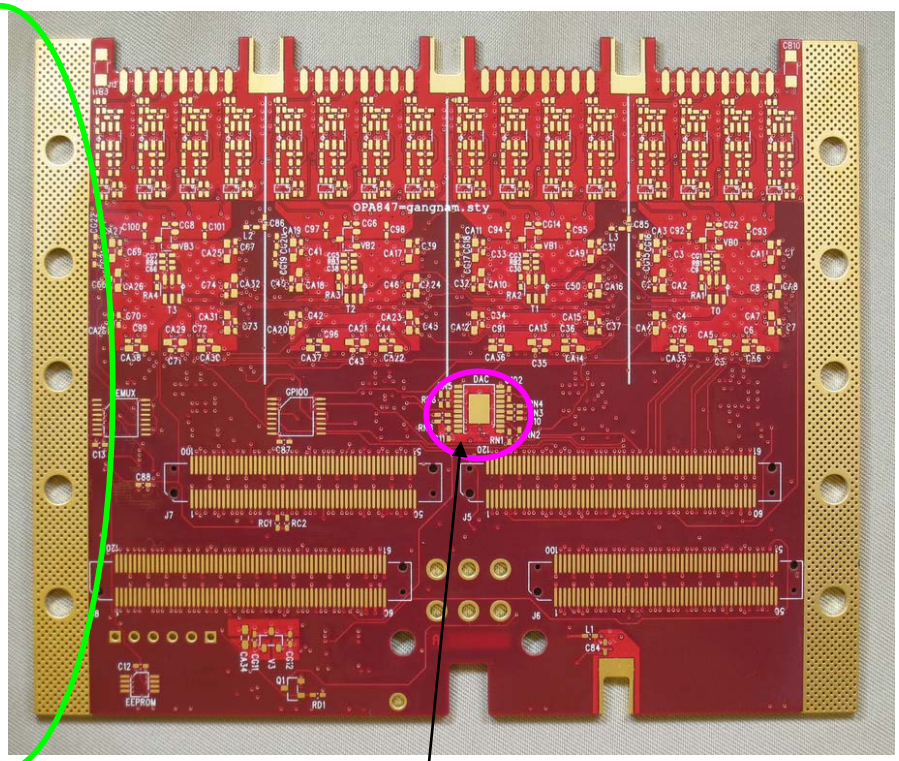
3+ TOP modules of readout possible (when actual modules ready?)

Install and operate completed modules in Fuji CRT

Enough ASICs, Rev. C or D (final, dual-stage amp), SCROD Rev. C (?)

carrier02 revC improvements





new VadjN/P filtering

new thermal wall connections

new 16 bit DAC with series resistance

- received PCBs last week
- assembly to begin imminently
- will have assembled boards by end of August

Status and Prospects

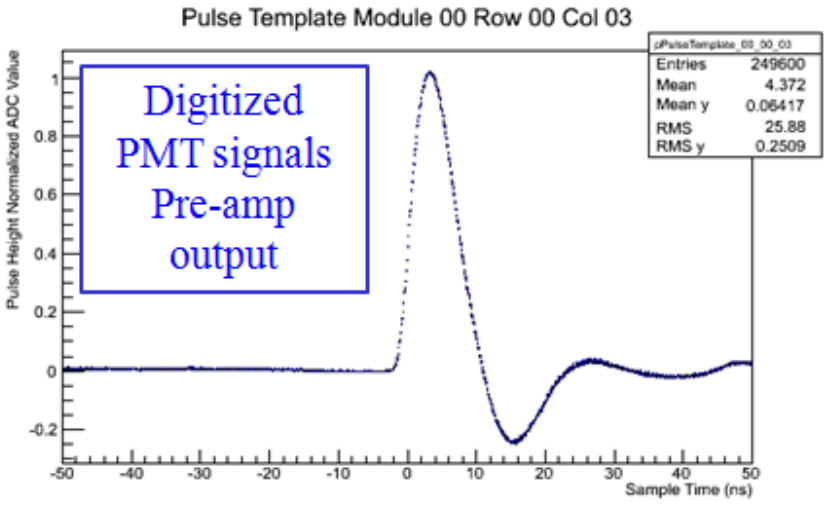
- Have achieved Key Performance Parameters over entire IRS3B-based readout module used in beam test; this is only minimum, <=50ps looks achievable

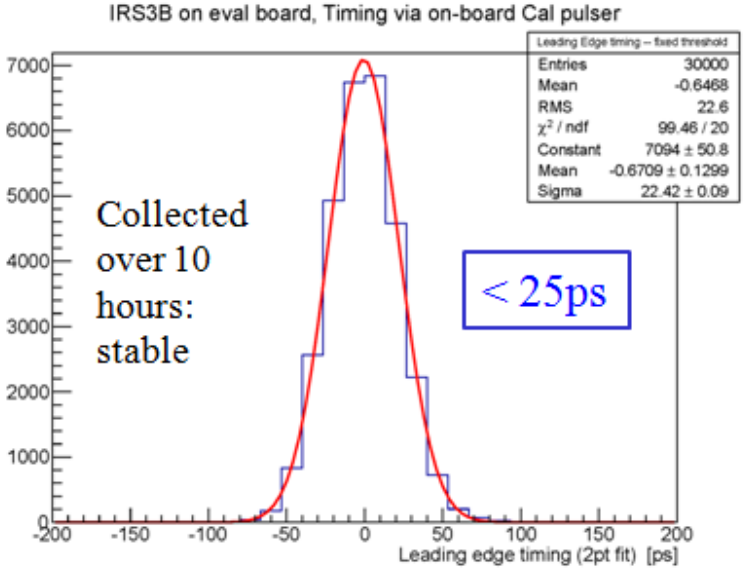
- Will fabricate/populate Carrier02 [IRS3B limited] so can have spares and distribute for testing elsewhere – improved thermo-mechanics

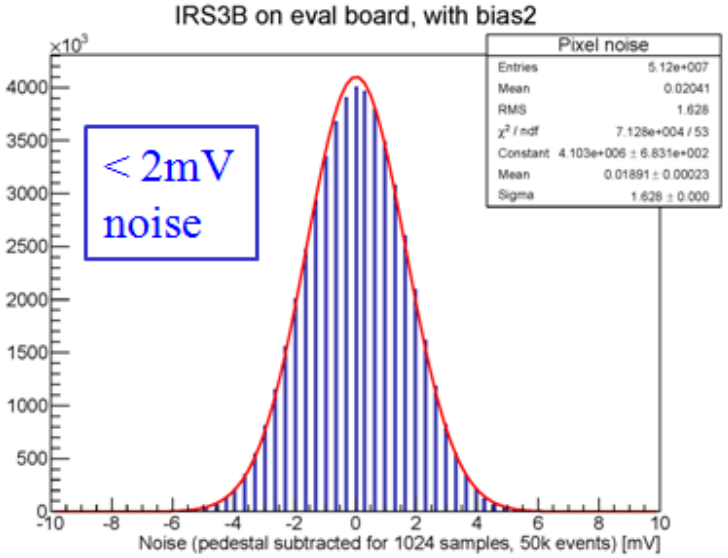
- IRS3C drop-in for IRS3B [extended dynamic range]

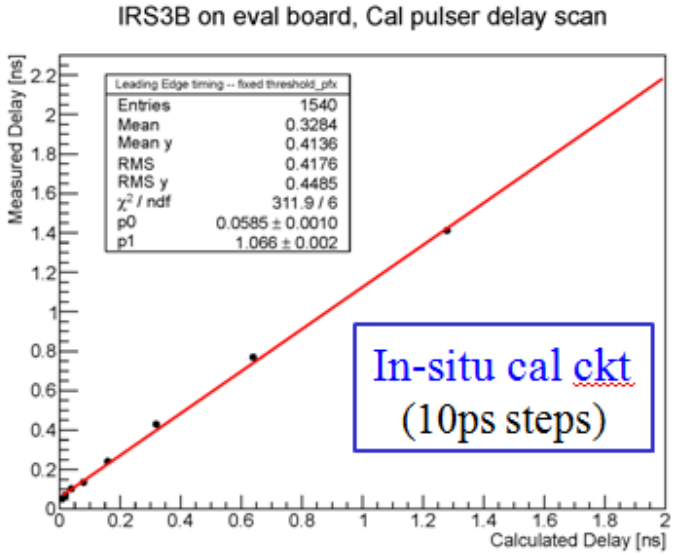
- Demonstrate true timing limits

Backup

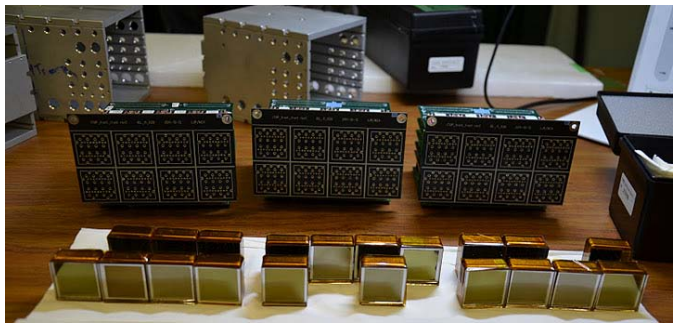
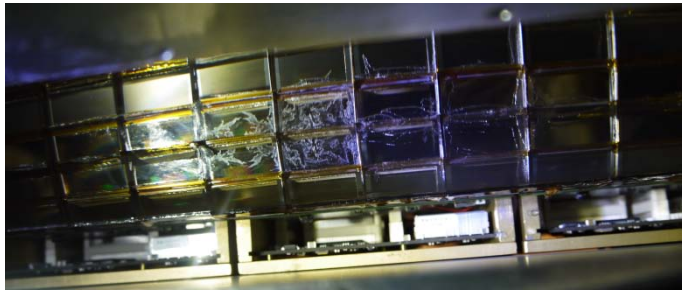

Pulse Template Module 00 Row 00 Col 03
Digitized PMT signals Pre-amp output
Entries 249600
Mean 4.372
Mean y 0.06417
RMS 25.88
RMS y 0.2509
Pulse Height Normalized ADC Value
Sample Time (ns)


IRS3B on eval board, Timing via on-board Cal pulser
Collected over 10 hours: stable
< 25ps
Entries 30000
Mean -0.6468
RMS 22.6
χ² / ndf 99.46 / 20
Constant 7094 ± 50.8
Mean -0.6709 ± 0.1299
Sigma 22.42 ± 0.09
Leading edge timing (2pt fit) [ps]


IRS3B on eval board, with bias2
< 2mV noise
Pixel noise
Entries 5.12e+007
Mean 0.02041
RMS 1.628
Constant 4.103e+006 ± 6.831e+002
Mean 0.01891 ± 0.00023
Sigma 1.628 ± 0.000
Noise (pedestal subtracted for 1024 samples, 50k events) [mV]


IRS3B on eval board, Cal pulser delay scan
In-situ cal ckt (10ps steps)
Entries 1540
Mean 0.3284
Mean y 0.4136
RMS 0.4176
RMS y 0.4485
χ² / ndf 311.9 / 6
p0 0.0585 ± 0.0010
p1 1.066 ± 0.002
Measured Delay [ns]
Calculated Delay [ns]

Development Timeline (next steps)

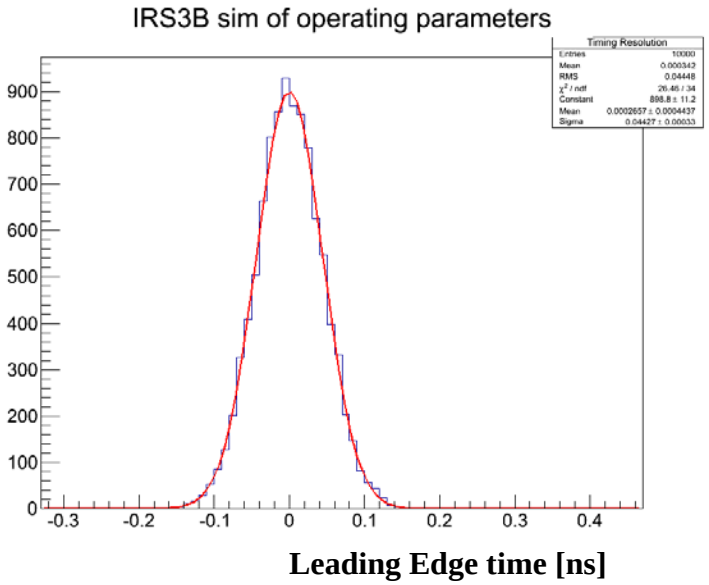
	Dates	Milestone(s)	Hardware
	< Spring ‘11	Prototyping	
Phase 1	Summer ‘11 – Winter 12	**FNAL beamtest**	
	Spring ‘12 – Winter 12	Semi-infinite reviews	
Phase 2	Spring ‘13 – Summer 13	**LEPS beamtest**	
	Autumn ‘13	**v. 3**	**IRS3C/IRSX**	**v.1 RT recon**	**FINv2, final boardstack**

Comparison IRS3B "toy" Monte Carlo

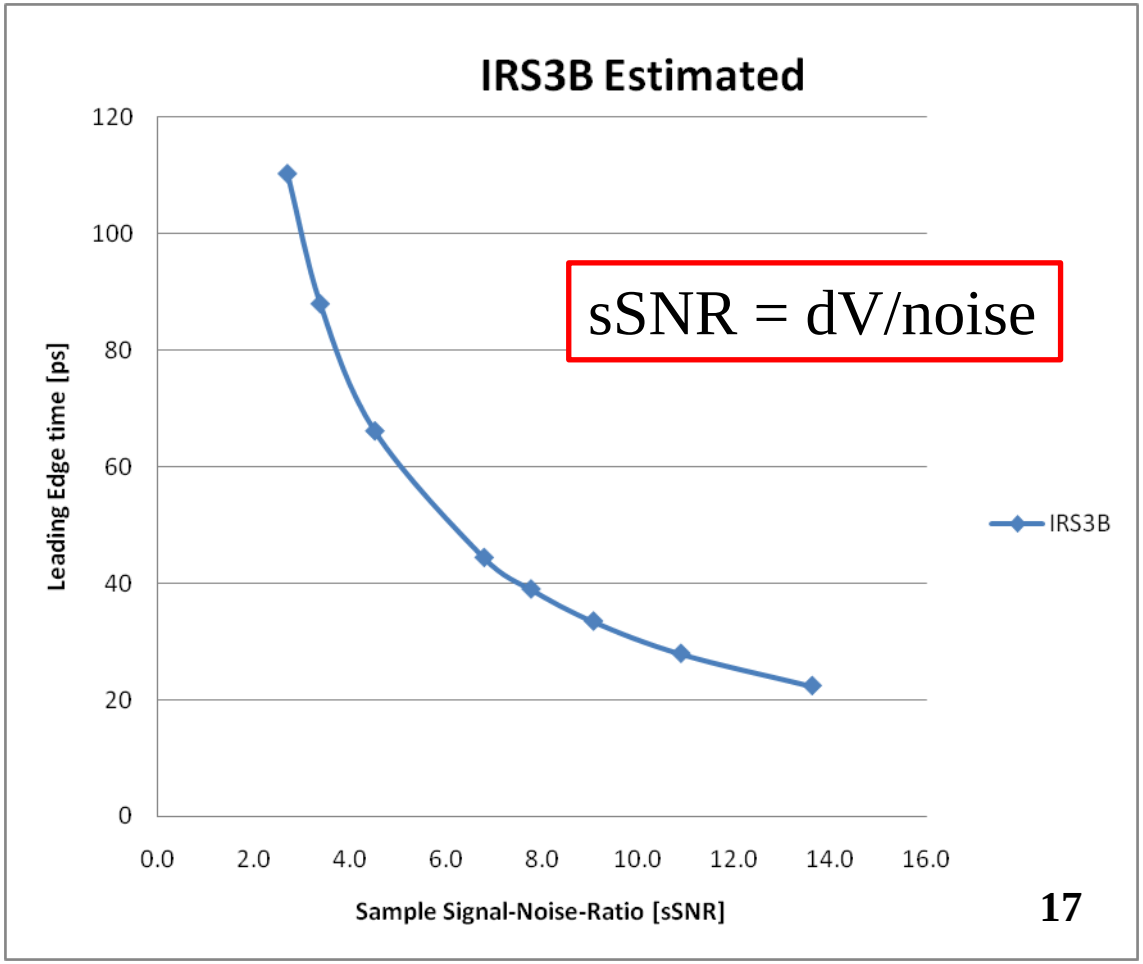
Vpeak	**100 ADC**
Risetime	**2.7 ns**
Sampling rate	**2.72 Gsa/s**
nom dT	**0.368 ns**
nom dV	**13.617 ADC/sample**

40% CFD ratio:

Applied between 2 points on leading edge that bracket this transition



~44ps for 100mV peak, 2mV noise



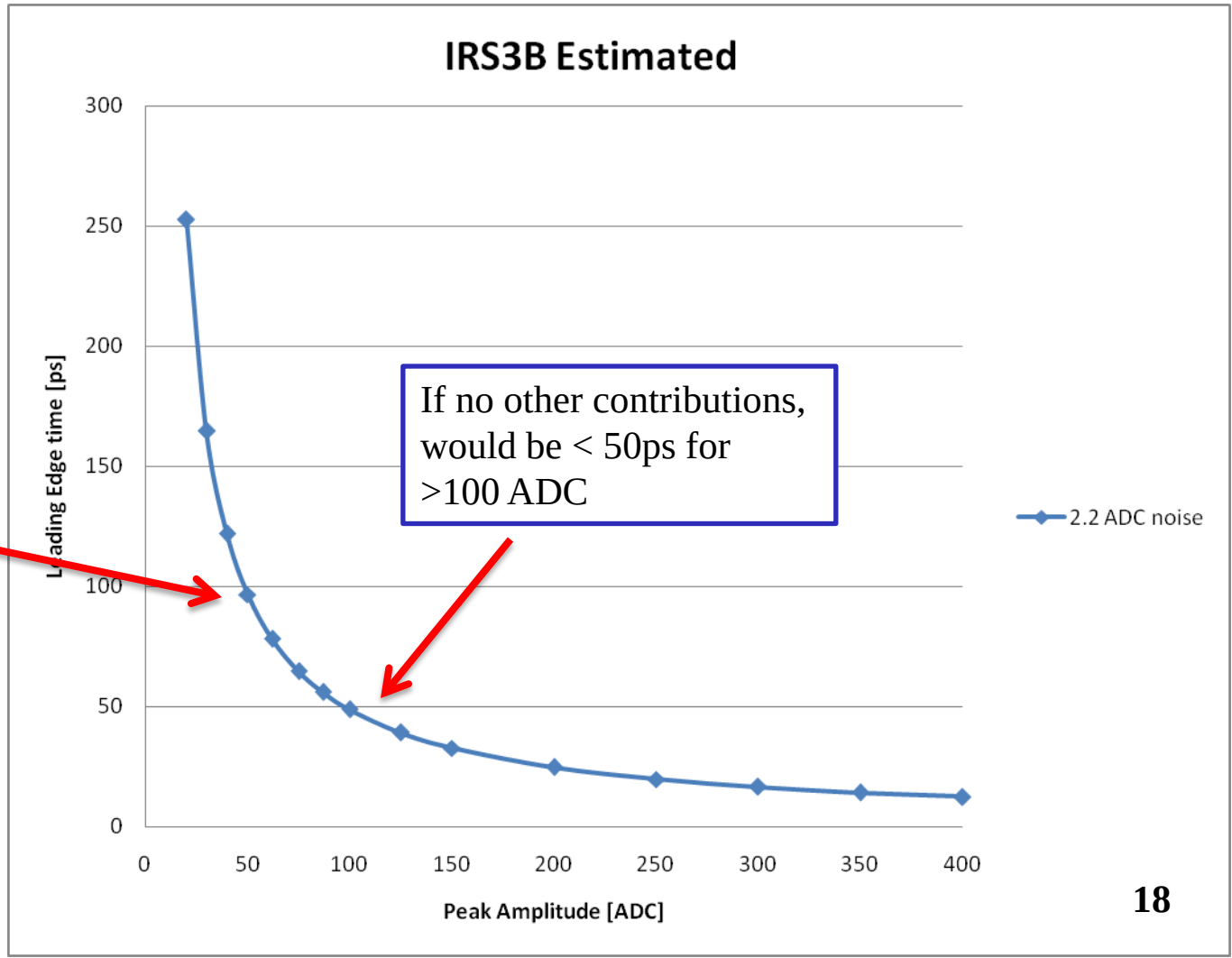
In general, noise ‘fixed’

Noise	**2.4 ADC**
Risetime	**2.7 ns**
Sampling rate	**2.72 Gsa/s**
nom dT	**0.368 ns**

40% CFD ratio

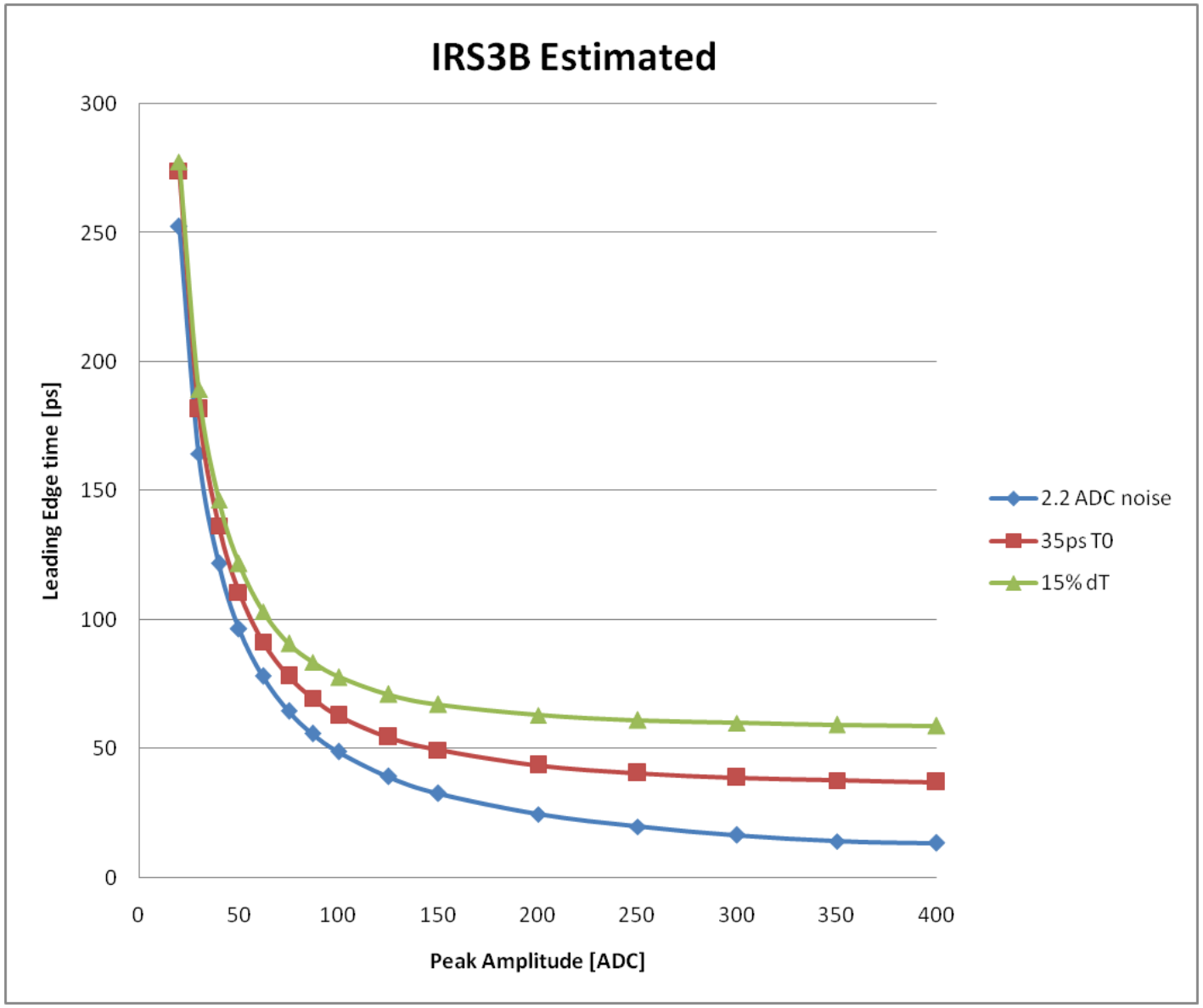
Even in ideal case, for only using 2 points on leading edge, need Vpeak >= 50 ADC to get below 100ps timing

(gain issue)



Adding in realistic degradations

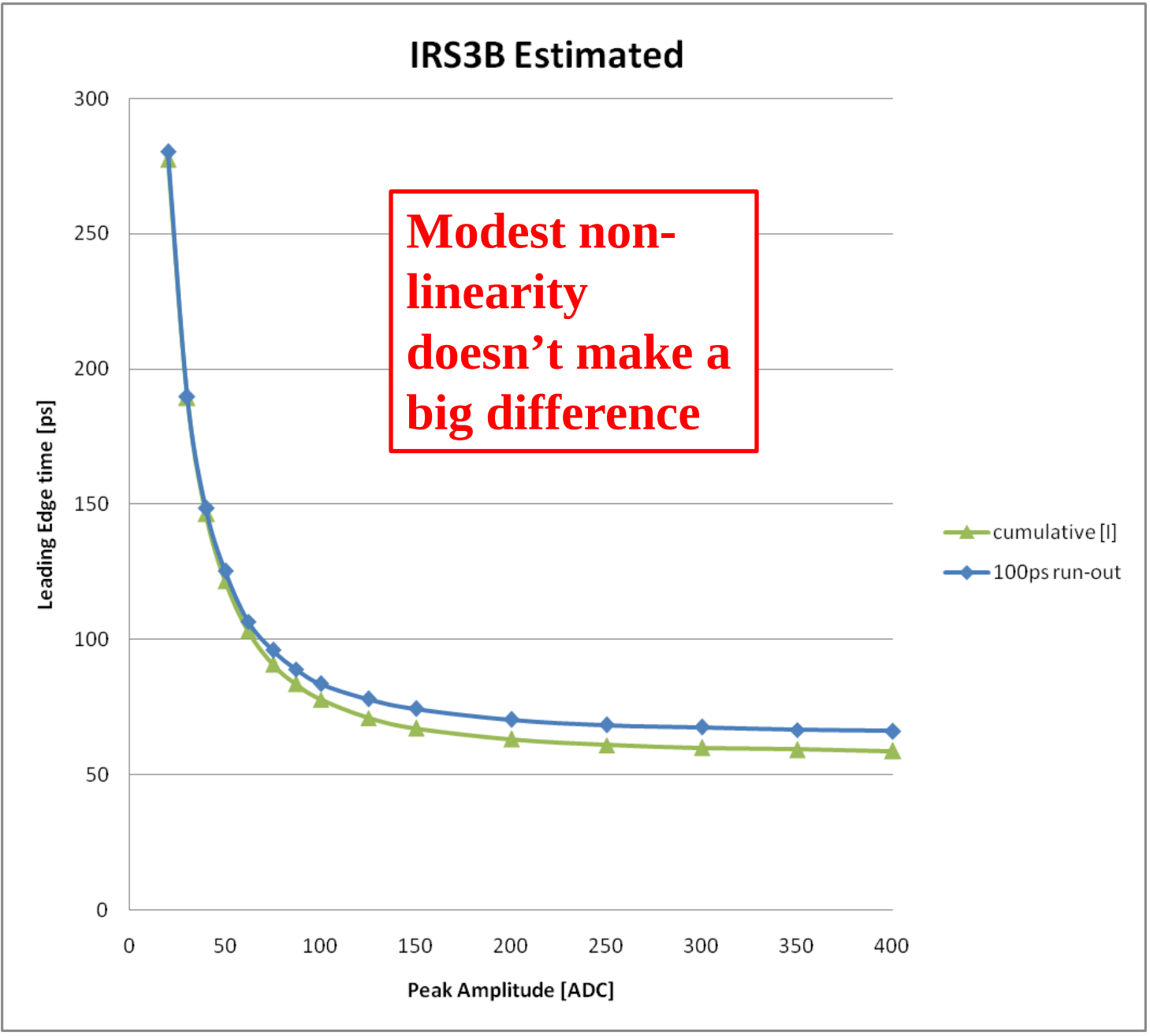
40% CFD ratio



What effects still missing?

- Residual Timebase jitter ?
- Non-linearity on leading edge?
- Something else ?

Adding in realistic degradations (II)



What effects still missing?

Amplifier noise? (doesn't impact pulser or sine data)

Ways to improve (short-term)

1. Increase gain (straightforward)
2. Add Voltage Regulator to amplifier power
3. Increase risetime
4. Add better VdlyN, VdlyP filtering (reduce timebase filter)

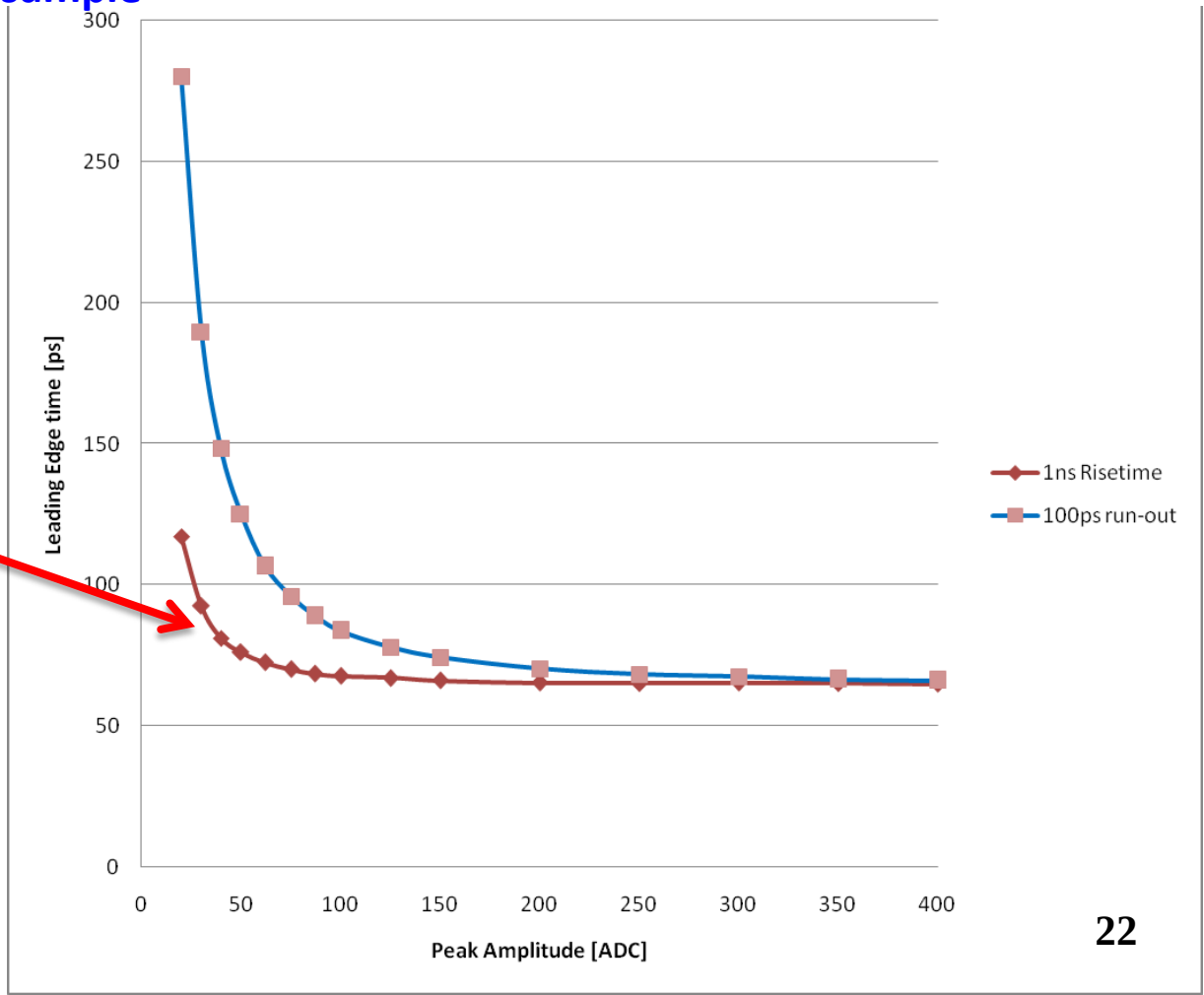
- All these to be improved on Carrier02 Thermo-mech prototype (boards have been fabricated, being assembled)
- Final mechanics after tests with new HV, front/PMT interface (final board-stack w/IRSX)

One example: improved Risetime

Vpeak	100 ADC
Risetime	1.0 ns
Sampling rate	2.72 Gsa/s
nom dT	0.368 ns
nom dV	13.617 ADC/sample

40% CFD ratio

Now < 100ps for ADC>30 (with no other changes)



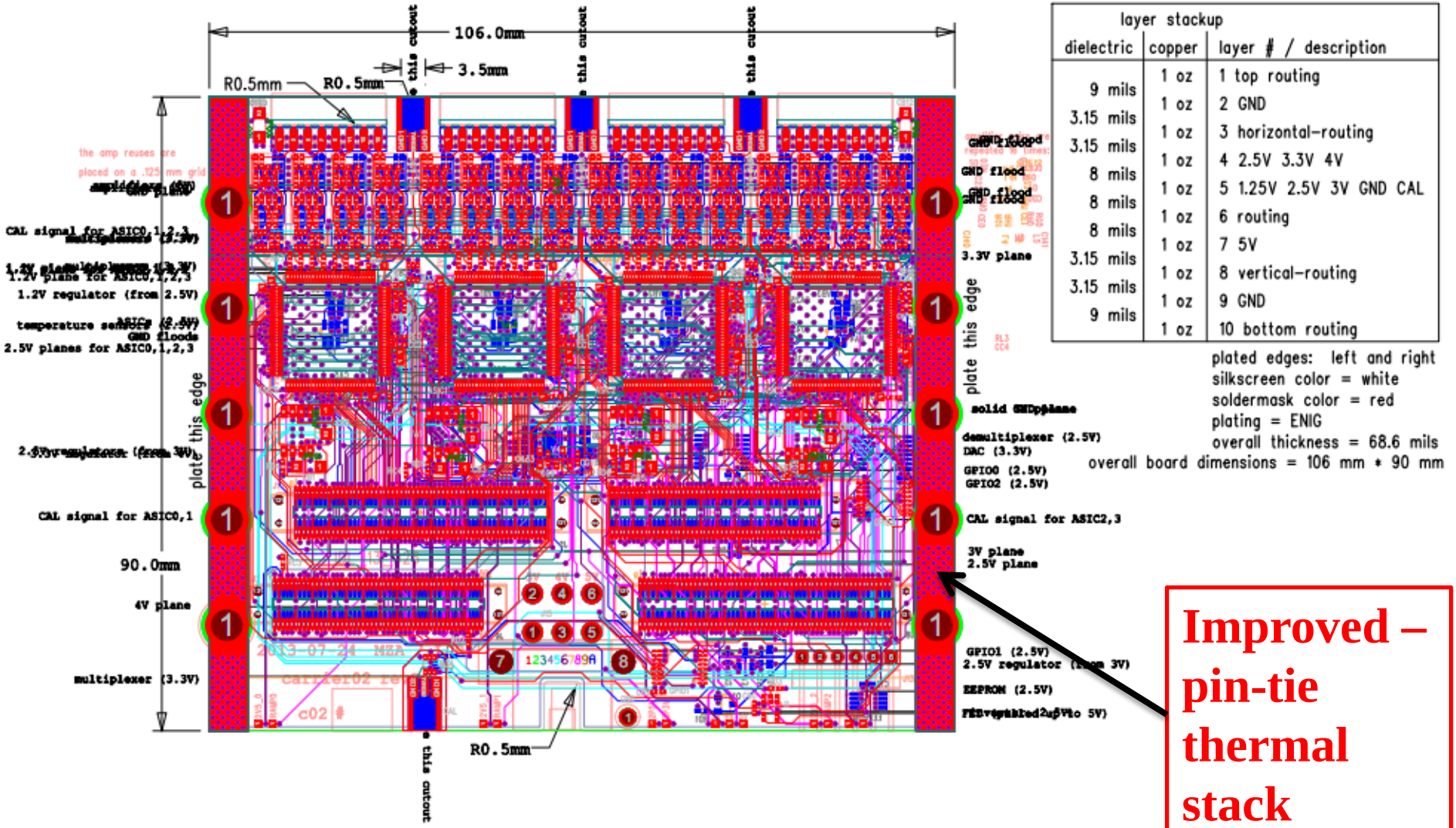
But will boost gain also

Improvements to carrier02

- √ Will populate with improved amplifiers
- √ add series resistor and capacitors to VadjN/VadjP (10 Ohm+200pF+47nF+2uF)
- √ exchange SMA connectors for MMCX
- √ exchange 12 bit external DAC for 16 bit one in same series
- √ re-visit c02 wiring to allow powering entire boardstack with just one cable
- √ extend width of boards and add holes for new thermal wall structure concept
- √ swap ASIC regulator for one with a shutdown feature

full list at http://www.phys.hawaii.edu/~mza/PCB/iTOP/boardstack-v3.html

Layout of carrier02 revC



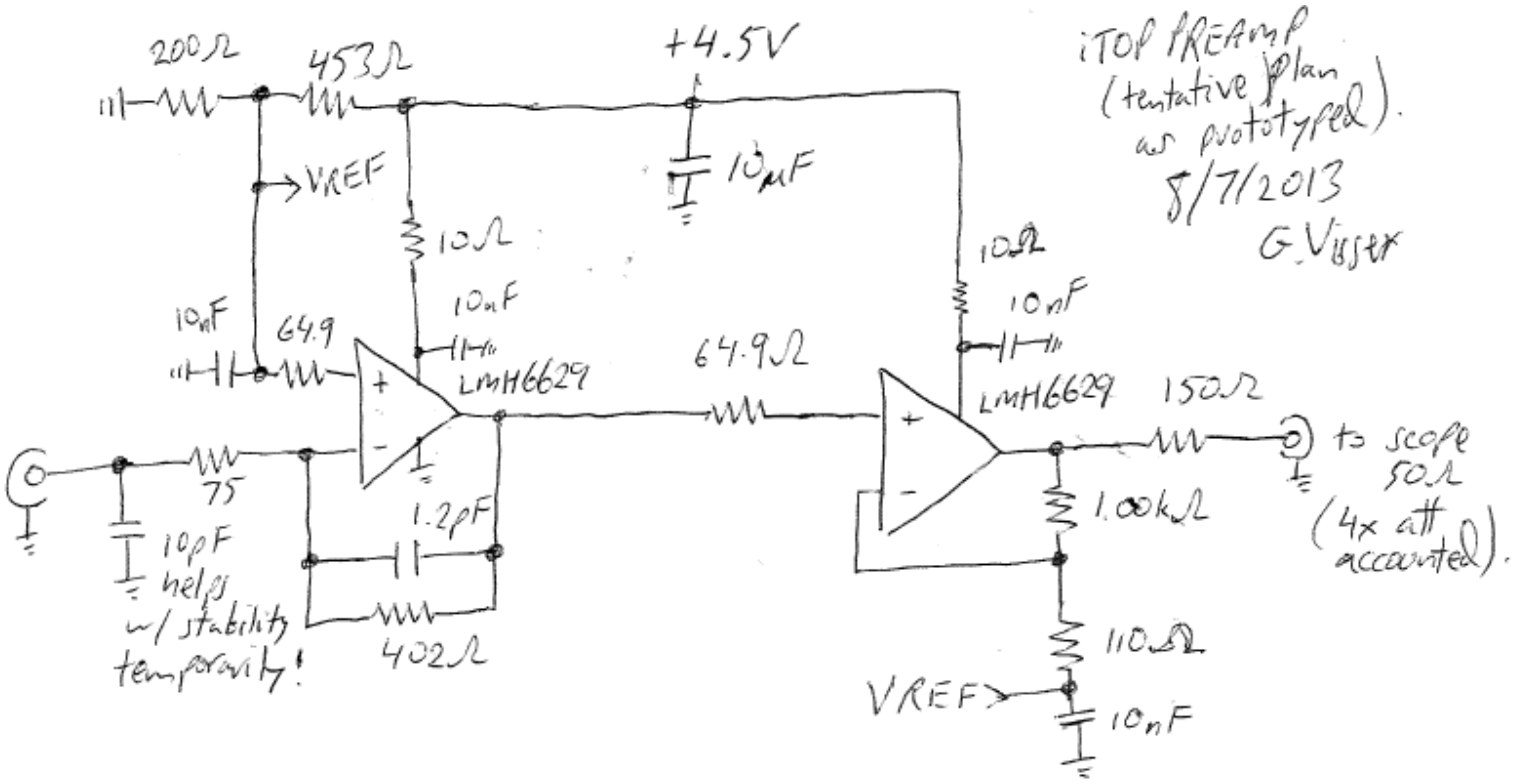
layer stackup		
dielectric	copper	layer # / description
	1 oz	1 top routing
9 mils	1 oz	2 GND
3.15 mils	1 oz	3 horizontal-routing
3.15 mils	1 oz	4 2.5V 3.3V 4V
8 mils	1 oz	5 1.25V 2.5V 3V GND CAL
8 mils	1 oz	6 routing
8 mils	1 oz	7 5V
3.15 mils	1 oz	8 vertical-routing
3.15 mils	1 oz	9 GND
9 mils	1 oz	10 bottom routing

plated edges: left and right
silkscreen color = white
soldermask color = red
plating = ENIG
overall thickness = 68.6 mils
overall board dimensions = 106 mm * 90 mm

Improved – pin-tie thermal stack

design posted at:
http://www.phys.hawaii.edu/~mza/PCB/iTOP/carriers/index.html

2-stage prototype Amp

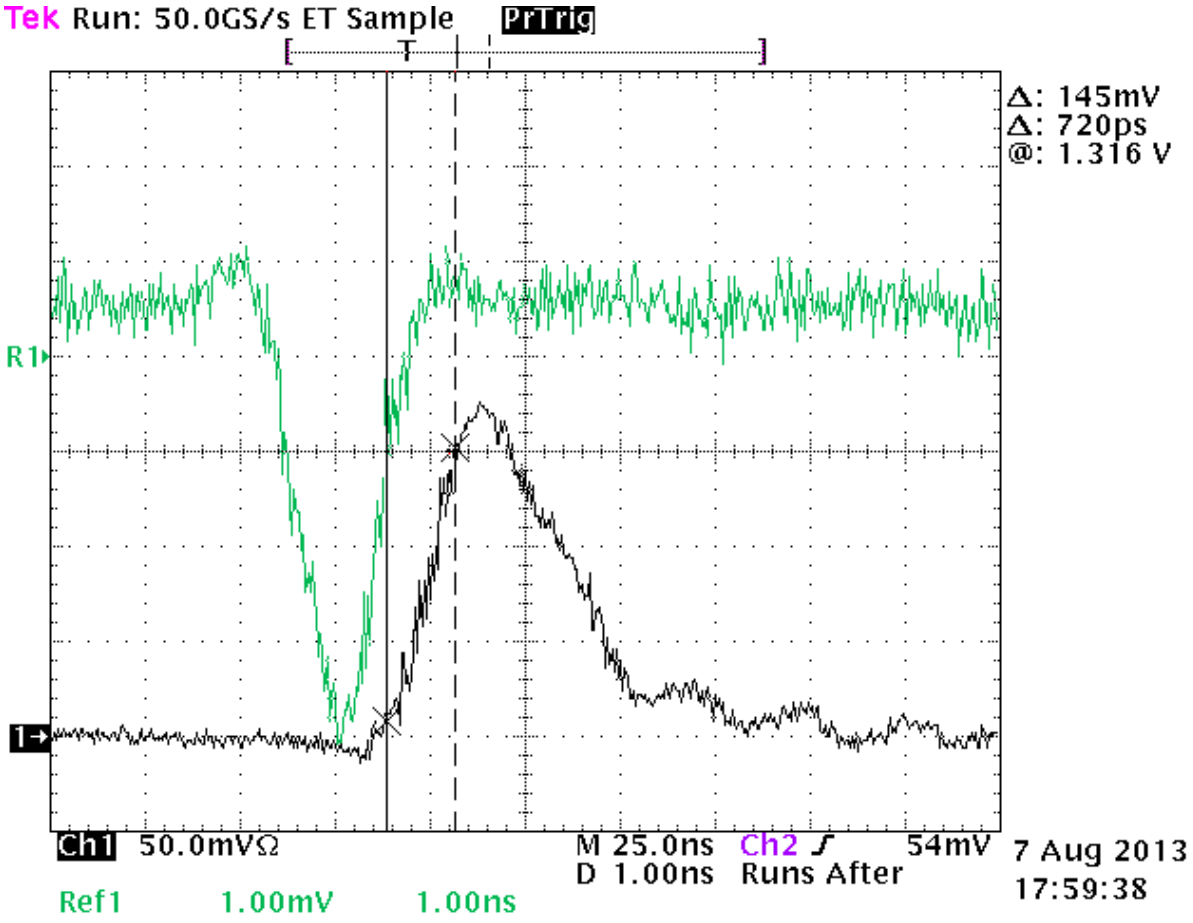


2.72 ns risetime

1.45 ns risetime

Optimization study ongoing …

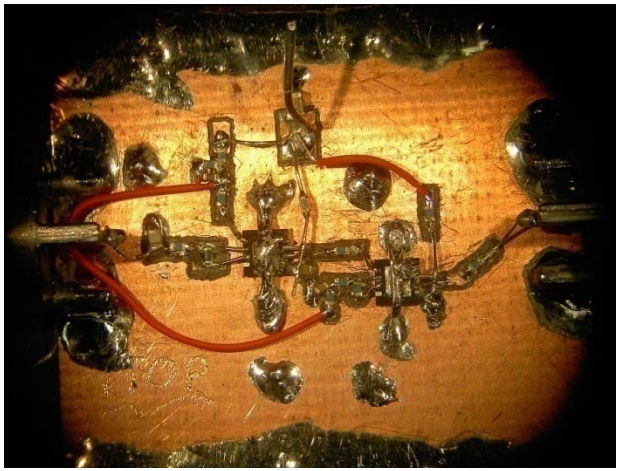
2-stage prototype Amp -- measurements



80fC injected charge

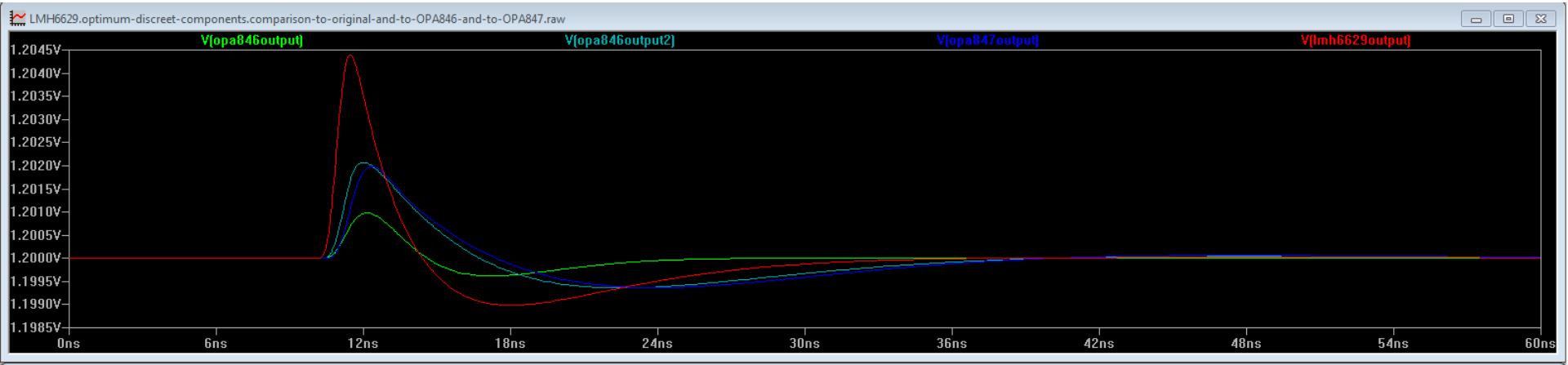
<1 ns risetime

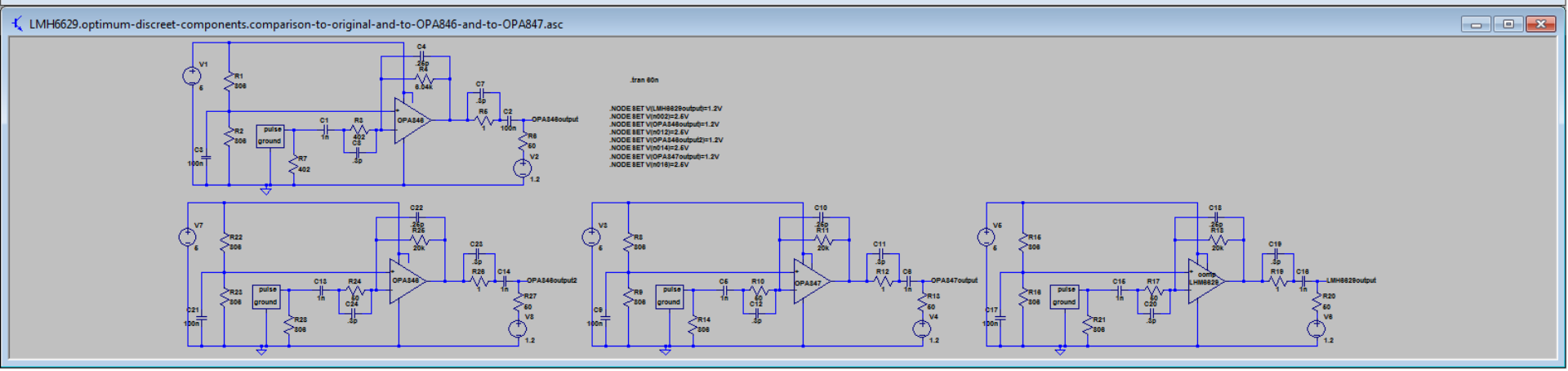
170mV peak
(~250-300 ADC counts)



Some care required to avoid oscillations..

For Rev C Carrier02





Simulation indicates -- prior to changing layout radically (2x stage design), can already improve amplitude/risetime by switching to LHM6629 (single stage)

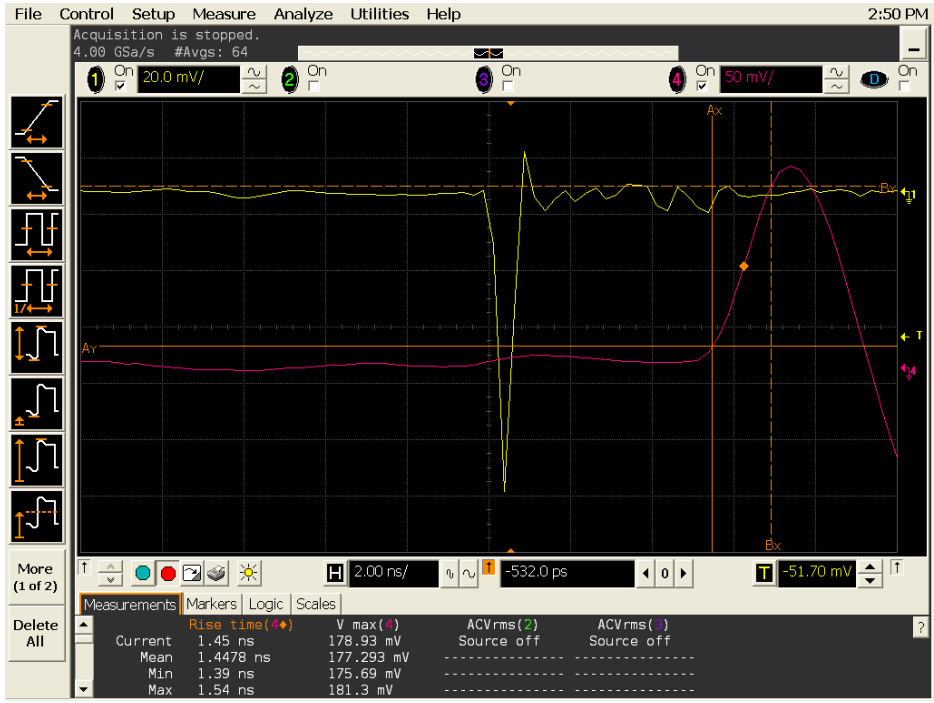
Need to confirm stability – will populate first batch with this circuit

Optimizing gain, risetime for “drop in” amp

original circuit (OPA846, 6k feedback)

2.72 ns risetime

new circuit (OPA847, 2.4k feedback)



1.45 ns risetime

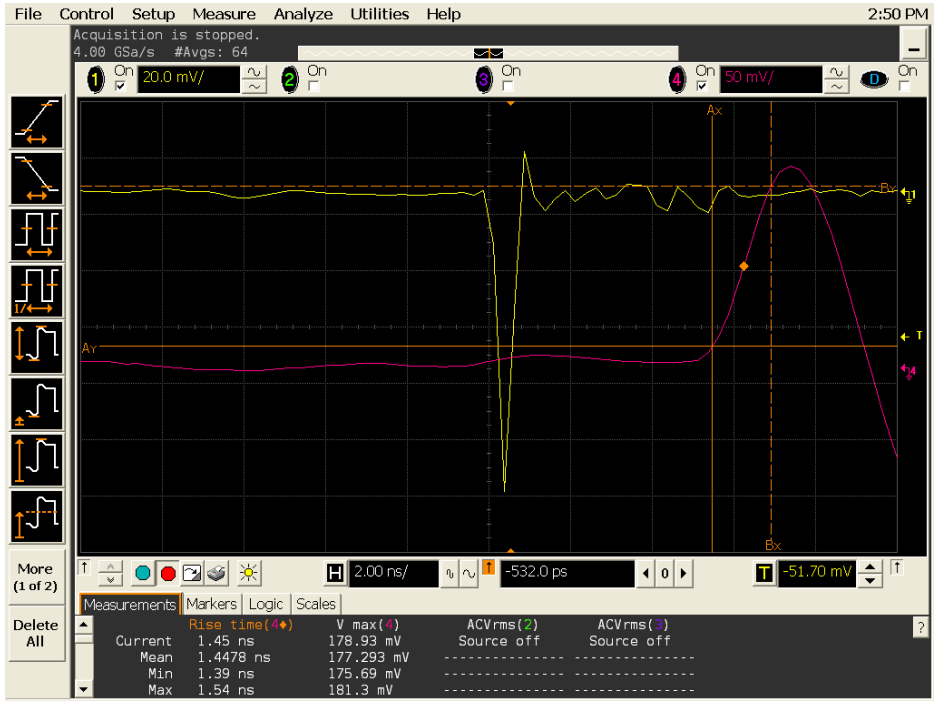
Previous measurements…

Optimizing gain, risetime for “drop in” amp

original circuit (OPA846, 6k feedback)

2.72 ns risetime

new circuit (OPA847, 2.4k feedback)



1.45 ns risetime

Optimization study ongoing …

Next steps: IRS3C & IRSX ASICs

www.phys.hawaii.edu/~idlab/taskAndSchedule/ASIC/IRSX/IRSX_homepage.html

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IRS Rev. X [Belle II iTOP (pen)ultimate ASIC]

Design Reference Page

Predecessor relevant documentation is provided on the IRS3C page and IRS3B page

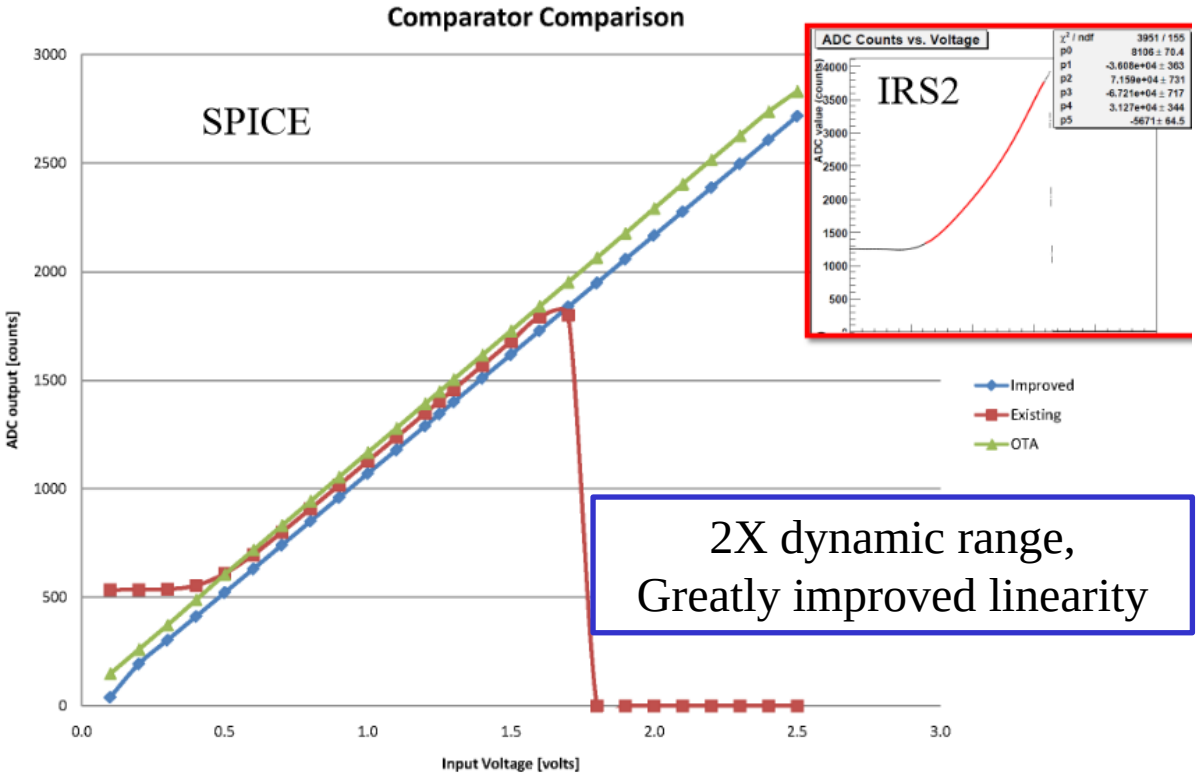
Submission Status Update (30-JUN-2013)

1. In order to match funding profile, "1/4" batch of ASICs need to be ordered "soon" (7/29 and 8/19)
2. Proposed changes (for discussion):
   1. Trigger path gain boost (for lower threshold operation)
   2. Make SSTin LVDS (and point-point from SCROD Rev. B)
      - Remove TRGmon to free up pins
   3. Move to common WL_CLK (Wilkinson clock), bring in as LVDS, sample phase (2x sampling speed)
      - Remove Vdly, TST_out
      - No Start, overflow detect needed (just stop counting at desired saturation valu
   4. WBias as monitor only? (Analog multiplexer?)
   5. WR_ADDR increment set from internal/programmable delay [internal address clock
      - Increment value [3-bit? -- skip ROI?] from SCROD (?)
      - Needs reset
   6. h-GRAPH/TARGET7 extended dynamic range/linearity comparator modifications
   7. DONE signal to indicate when all conversions are complete (reduce deadtime)
   8. Charge pump prototype(?)

IRS3C = IRS3B + 2 small changes

(in fab – due imminently)

Example: linearity improvement



Exploit lessons learned from TARGET[i] series development, other ASICs

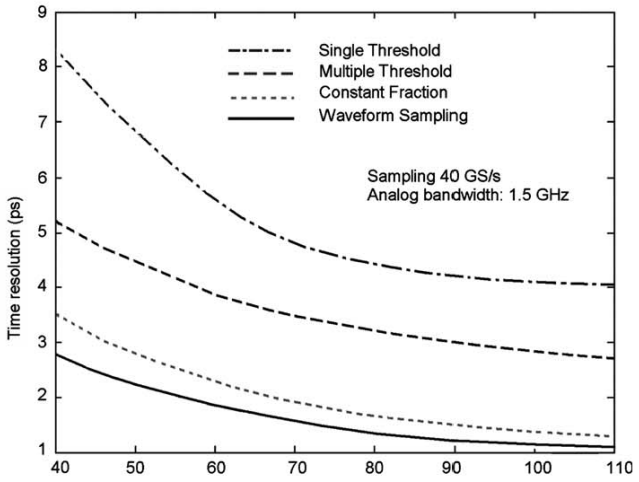
IRSX design review (September – if ready)

2X dynamic range,
Greatly improved linearity

Expectations – matched to measurements

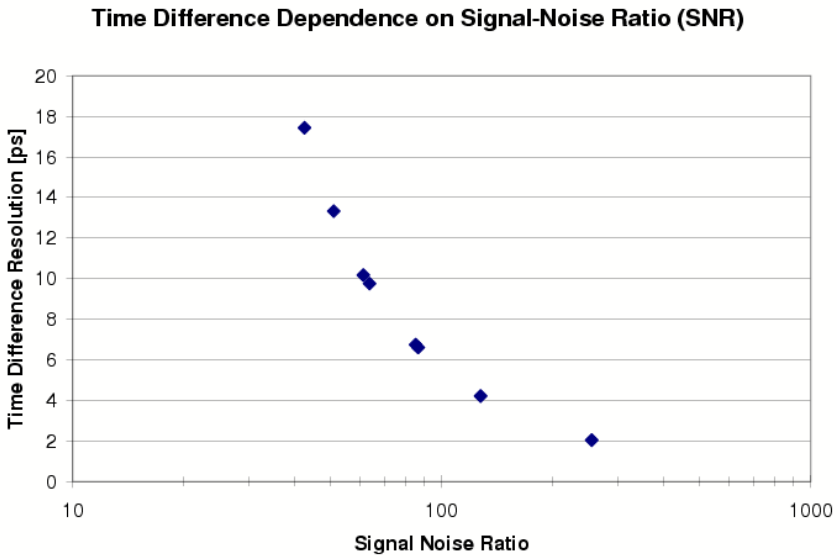
- Noise/amplitude
- Non-linearity
- Timebase non-uniformity

Simulation includes MCP response

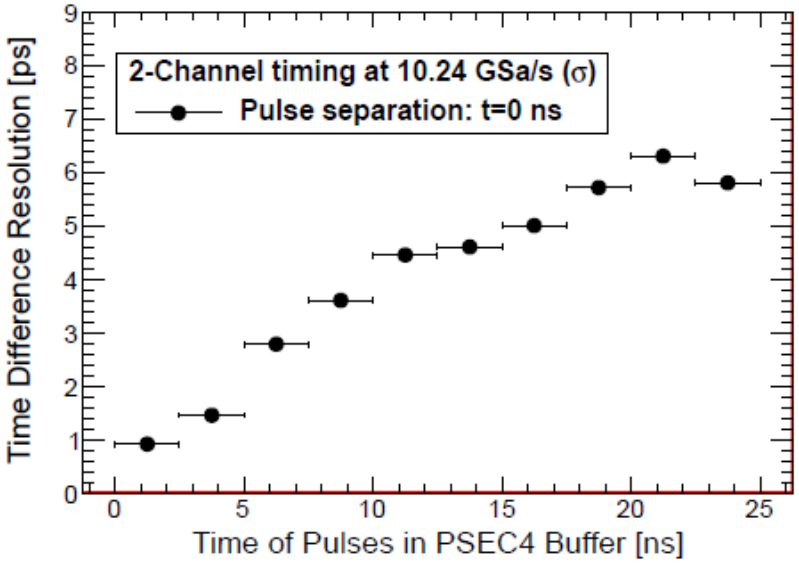


J-F Genat, G. Varner, F. Tang, H. Frisch
NIM A**607 (2009) 387-393**.

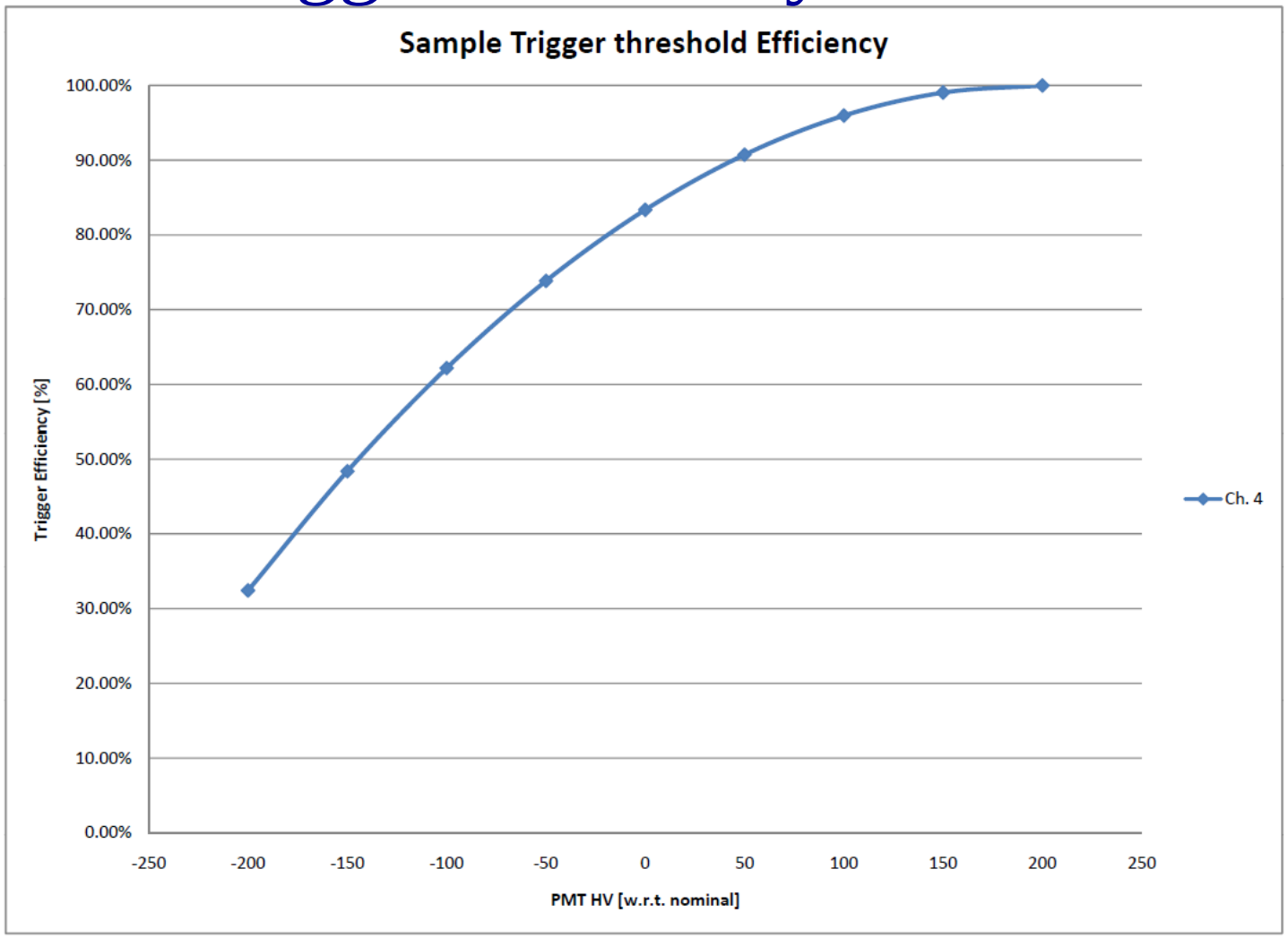
1GHz analog bandwidth, 5GSa/s



G. Varner and L. Ruckman
NIM A**602 (2009) 438-445**.



Trigger Efficiency estimate



Simple estimate based upon trigger threshold dependence

Use as cross-check for detailed fit estimate, though robust (insensitive to laser coupling/optical fiber alignment)