PIXRO1 Chip

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Outline

- Background Introduction
- 4 Schemes
- Scheme1 Circuit Design & Results
- Schedule
Overview of Belle DAQ system
Readout Subsystem

- CAP3: 21mm*3mm, ~115,000 pixels
- 16 pairs of Channels, two time sampling/ pair channel
- Data Rate Criteria

10cm 32 channels 100MSa/s 30m 1.6GSa/s (6 Bits Resolution)
A Close Look at Readout Board

The diagram shows the components of a readout board, including:

- **CAP 3 Pixel Sensor**
- **Diff Amp**
- **Analog Process**
- **Laser Drive**
- **Laser**
- **PIXRO1 Chip**
- **Clock Multi**
- **FPGA Controller**
- **DMUX**
- **Front-end Amplifier**
- **Photodiode**
- **Signal Fiber**
- **Back-end Electronics**
- **Power Source**

The flow of signals is as follows:

2. The output from the Diff Amp goes to the Analog Process, then to the Laser Drive, and finally to the Laser.
3. Control signals (m bits) flow from the FPGA Controller to the DMUX, then to the Front-end Amplifier, and finally to the Photodiode.
4. The Signal Fiber connects the Laser to the Back-end Electronics.
5. The Power source supplies power to the system.
PIXRO1 Chip

- Differential twice sampling signal
- Pipeline data
- Convert from parallel signal into series signal
- Drive Laser
- IBM 0.5µm SiGe BiCMOS 5HP
  - Compatible with CMOS design, RAM
  - BJT (HBT) offers fast speed, MUX
- Four schemes proposed
  - Advantages vs. Disadvantages
  - Theorem vs. Application
Scheme 1: High-speed Analog MUX

Sample and Hold

Diff Amp

32 Channels

AMUX

Laser Driver
Scheme 2: High-speed Analog RAM with Selection

Diagram:

- PIXEL
- Analog RAM
- Laser Driver
- To Laser
- Address
Scheme 3: Conversion and Compression Digital Transfer

First Configuration

32 channels

Control Signals

Memory

ADC Module

MUX

Laser Driver

To Laser
Scheme 3: Conversion and Compression Digital Transfer (Cont.)

- Second Configuration

32 channels

Control Signals

ADCG

MUX

RAM

RAM (Threshold)

Laser Driver

To Laser
Scheme 4: Digital Pulse Width Modulation

32 channels

Sample and Hold Cells

Control Signals

Input (Voltage)

Reference Clock

Output (time)

Analog MUX

V-t Modulator

Laser Driver

To Laser

09/17/2004

Belle Project, ID meeting
Scheme 1 Circuit Design

CMOS

Sample and Hold

Diff Amp

32 Channels

BJT

AMUX

Laser Driver

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Scheme 1 Circuit Design (Cont.)

- Sample and Hold Circuit

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Simulation Result

- $T=0.7\text{ns (143MSa/s)}$
Simulation Result (Cont.)

<table>
<thead>
<tr>
<th>in (V)</th>
<th>out (V)</th>
<th>t_settle (ns)</th>
<th>diff(V)</th>
<th>error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.9</td>
<td>0.88</td>
<td>0.13</td>
<td>-0.02</td>
<td>-2.22222</td>
</tr>
<tr>
<td>1</td>
<td>0.983</td>
<td>0.14</td>
<td>-0.017</td>
<td>-1.7</td>
</tr>
<tr>
<td>1.1</td>
<td>1.086</td>
<td>0.08</td>
<td>-0.014</td>
<td>-1.27273</td>
</tr>
<tr>
<td>1.2</td>
<td>1.189</td>
<td>0.06</td>
<td>-0.011</td>
<td>-0.91667</td>
</tr>
<tr>
<td>1.3</td>
<td>1.292</td>
<td>0.09</td>
<td>-0.008</td>
<td>-0.61538</td>
</tr>
<tr>
<td>1.4</td>
<td>1.396</td>
<td>0.06</td>
<td>-0.004</td>
<td>-0.28571</td>
</tr>
<tr>
<td>1.5</td>
<td>1.499</td>
<td>0.02</td>
<td>-0.001</td>
<td>-0.06667</td>
</tr>
<tr>
<td>1.6</td>
<td>1.603</td>
<td>0.02</td>
<td>0.003</td>
<td>0.1875</td>
</tr>
<tr>
<td>1.7</td>
<td>1.707</td>
<td>0.08</td>
<td>0.007</td>
<td>0.411765</td>
</tr>
<tr>
<td>1.8</td>
<td>1.81</td>
<td>0.11</td>
<td>0.01</td>
<td>0.555556</td>
</tr>
<tr>
<td>1.9</td>
<td>1.913</td>
<td>0.13</td>
<td>0.013</td>
<td>0.684211</td>
</tr>
<tr>
<td>2</td>
<td>2.014</td>
<td>0.16</td>
<td>0.014</td>
<td>0.7</td>
</tr>
<tr>
<td>2.1</td>
<td>2.113</td>
<td>0.16</td>
<td>0.013</td>
<td>0.619048</td>
</tr>
<tr>
<td>2.2</td>
<td>2.208</td>
<td>0.18</td>
<td>0.008</td>
<td>0.363636</td>
</tr>
<tr>
<td>2.3</td>
<td>2.301</td>
<td>0.14</td>
<td>0.001</td>
<td>0.043478</td>
</tr>
<tr>
<td>2.4</td>
<td>2.397</td>
<td>0.16</td>
<td>-0.003</td>
<td>-0.125</td>
</tr>
<tr>
<td>2.5</td>
<td>2.496</td>
<td>0.18</td>
<td>-0.004</td>
<td>-0.16</td>
</tr>
</tbody>
</table>

- **Linear**
- **Fast settle time**
- **After calibration, should achieve 10 bit resolution**

![Sample Hold Circuit Graph]

Vin (V) | Vout (V)
-------|----------
0       | 0.00     
1       | 0.18     
2       | 0.36     
3       | 0.55     
4       | 0.72     
5       | 0.89     
6       | 1.07     
7       | 1.25     
8       | 1.43     
9       | 1.60     
10      | 1.78     
11      | 1.95     
12      | 2.13     
13      | 2.30     
14      | 2.48     
15      | 2.65     
16      | 2.83     
17      | 3.00     

09/17/2004  Belle Project, ID meeting
Schedule and Plan

- PIXRO1 IBM SiGe BiCMOS 0.5µm 5HP
  - Process Submission Deadline: Oct. 25
  - Scheme1 AMUX: Sep. 20

- CAP3 TSMC CMOS 0.25µm
  - Process Submission Deadline: Oct. 18