Towards a Detector Upgrade with Monolithic Active Pixel Sensors

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Detector must tolerate increased hit density and large radiation doses.

- Occupancy
  Current robustness is marginal. At 20x background, even with segmentation (“striplet”) and shorter shaping/pipelined readout – a concern

- Improvement
  One of the few areas in which the detector can be improved

March 1997, Varner & Sahu: Belle Note #226
  • Simplistic evaluation of the raw contributions to vertexing
  • Argued for improvement

Recent advances in deep sub-micron MAPS look promising for S-Belle vertexing.
Cont. Acq. Pixels (CAP) 1/2 Prototypes

- TSMC 0.35μm Process

- CAP1: simple 3-transistor cell

- CAP2: 8x mini-pipeline in each cell

Column Ctrl Logic

Pixel size: 22.5 μm X 22.5 μm
Pixel array: 6 Kpixels

Sample of CAP1/CAP2 tested: all detectors (>15) function.
Correlated Double Sampling (CDS)

Frame 1 - Frame 2 =

- Leakage current Correction

~fA leakage current (typ)
~18fA for hottest pixel shown

Hit candidate!

8ms integration

Can readout/process @ 20Hz ~ 16% live time (CAP1!)
June 2004 Test Beam/π2-area

π2 area

B-Board / DAQ

CAP targets!

4 F2s / Pixel Sensor
Initial “by eye”

Layer-by-layer correlations

~1mm x 3mm “rice grain”

And after only 4 iterations…
Improved Alignment

Det.3 vs. Det.1
Det.3 vs. Det.2
Det.3 vs. Det.4

In X

In Y

“online” plot
Hits! alignment proof
Resolution: GEANT Expectation

In our case: measurement of intrinsic resolution degrades mainly because of distances between pixel detectors (constraints from Front-End board design)

No IR smearing
UL on Resolution

Current Residuals, @ 4GeV:
- 11µm in x plane
- 14µm in y plane
Collected Charge vs. Cluster Size

... still June 2004 beam test data...

Of interest:
- 50% of the charge is in the peak pixel.
- 90% in the 4 mains.

Studied with a data sample of ~1800 4GeV pion tracks.

(MPV of landau fit)
Hyp: charge entirely collected in 3X3 pixel array.
Of interest:
- SNR peak signal between 16 and 20.
Four Critical R&D Items

1. Readout Speed
   1. Elsewhere: STAR phase 1, LC, RAL efforts
   2. Super-B: CAP2, syst. archi., next main R&D topic

2. Radiation Hardness
   1. Elsewhere: TESLA, STAR $10^{12}$ n$_{eq}$, >100kRad ionizing
   2. Super-B: low E e$^{-}$/γ CAP -- results shown next

3. Thin Detector – LBNL

4. Full-sized detector - LEPSI
1. Increased readout speed: CAP2

Technical implementation:
1) A 8-fold mini-pipeline sits in each pixel.
2) Mechanism to write to and read from the appropriate buffer.

15µs operation of CAP2:
Current status:

1) Noise higher than what is observed with CAP1/F2/B2 (~30/~35e- vs. 16e-). Related to digital activity? → Shield?
2) Leakage current under control.
3) Mini-pipeline output level dispersion rather large. Not a dramatic problem, but can improved (by design). → Modification in pipeline design?
4) Still more work to be done on CAP2 testing.
2. Irrad: leakage currents

0.35mm CMOS APS Leakage Current

- **Belle CAP1 Prototype**

**Leakage Current [fA]**

- **Eid et al.**
- **no anneal**
- **60 hr 60C**
- **60hr/60C+2mo/20C**

Proper annealing is still to be completed for 3Mrad prototype.

Wait eagerly new irrad data to come.
Present R&D items / plans (1)

- Compact packaging for next beam test:
  - Expect a better upper limit on intrinsic resolution

Highlights: - <0.3cm between CAPS.
  - eases alignment.

Status: PCB of D-Boards designed & ordered from vendor. Back these next days.
Present R&D items / plans (1)

3mm spacing between detectors, 300 μm Si.

@ 4GeV, 5-7μm (as in June beam test configuration) → 4μm

Effects of multiple scattering and of distances become negligible!

When could the next beam test be scheduled?
Present R&D items / plans (2)

- **New CAP prototype designs:**
  - **CAP3: “prototype iteration”**
    - **Array might be larger.**
    - **Go from 0.35 μm to 0.25 μm process.**
      - From 4 to 5 metal layers: better shielding!?
      - Increased radiation-hardness(?)
      - More pipeline if possible.
      - Technical change in pipeline: less dispersion.
      - Differential reads!? (might be tricky to implement)
  - **CAP4: “full-size detector”**
    - Still in decision process: should we go directly to a CAP4 like full size design?
      - **Interests:** experience with full-size MAPS, realistic constraints on system architecture, neat.
      - **Disadvantages:** risky as it costs ¥¥¥ / $$$ (CAP4 ~7.5X more expensive).

⏰ Beware, need to submit the design at a specific time
Present R&D items / plans (3)

- **System architecture:**
  - A topic we are now actively investigating:
    - Four system architectures considered at present time, number might increase:
      a) High speed analog buffering.
      b) High speed analog buffering with on-chip data reduction.
      c) ADC on Front-End board and (sparsified) digital data transfer.
      d) Digital pulse width modulation.

    → **Estimate data volumes vs. system architecture.**
    → **Link to FINESSE Board.**

⏰ More on this topic at HL06 WS / next BGM.
Summary & Conclusion

• **Quite successful beam test in June:**
  • Experience gained / Demonstrate beam test operation.
  • UL on intrinsic resolution: 11µm.
  • Charge spread: 90% of charge contained in 4 pixels.
  
  We look forward to the next beam test opportunity.

• **CAP2 and next iterations:**
  • Works alright, more work to be done → improvements.

• **Further Radiation Damage Studies:**
  • Still a hot topic, we wait for new data points.
  • Demonstrate operation with highly irradiated detectors.

• **Investigate now various system architecture**
  
  Report on that topic: HL06 WS and next BGM.
  Have started a Belle Note, could be the basis for a future PVD 1.0 Technical Design Report